Implementation of Soft Switched Low Stress ZVT PWM Converter for Renewable Energy Applications

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Abstract

This paper presents an improved soft switching technique zero voltage transition technique (ZVT-buck). For high frequency DC-DC converter switching losses and stresses are the main concern. One solution to this problem is replacing the switch with of a standard SMPS topology (buck, boost etc) with a resonant switch. This resonant switch topology operates under ZVS or ZCS to minimize the losses, stresses, noise, EMI and heating of the device. The proposed ZVT buck converter is compared with the ZVS buck converter. The ZVT PWM buck converter produces the less switching losses and stresses than the ZVS PWM buck converter. Also a closed loop approach designed for both the ZVS and ZVT techniques. All the above stated switching techniques are simulated using the MATLAB simulink at a frequency of 10 kHz.

Index Terms: *ZVT, ZVS, ZCS and PWM DC-DC converter.*

I.INTRODUCTION

Nowadays power demand is more than our generation it becomes a serious emerging problem. Two major technologies will play important roles to solve that problem. One is the change the electrical power production from conventional, fossil based energy sources to renewable energy sources. Another is to use high efficient power electronics in power generation, power transmission/distribution and end-user application. So for residential and industrial applications we are focusing more on the renewable energy (RE), this RE is converted as the useful DC/AC by the power electronics converters by many conversion stages. In conversion stages, switching loss and switching stress occurs due to the high frequency, di/dt and dv/dt operation, it significantly reduces the efficiency. Pulse Width Modulated (PWM) dc/dc converters are vastly used in industry because of their high-power capability and fast transient response. To reduce the volume and the weight of these converters, higher switching frequency operation is preferred. In high power frequency requirements, power semiconductor switches are subjected to high switching stresses and switching losses, which limits the operating switching frequency. Generally, a snubber circuit reduces the switching losses and stresses, but increases the total power loss in the converter. Recently, a number of soft-switching PWM techniques were proposed aimed at combining desirable features of both the conventional PWM and resonant techniques. Among them, the zero-voltage-transition (ZVT) PWM technique is deemed desirable since it implements zero-voltage switching (ZVS) for all semiconductor devices without increasing voltage and current stresses. This technique minimizes both the switching losses and conduction losses and is particularly attractive for high-frequency operation where power MOSFET's are used as power switches.

Ilse Cervantes and Sergio Perez-Teniers [1] have discussed about the QRC (Quasi Resonant Converters) used to illustrate procedure of ensuring soft-switching conditions using control actions. The proposed strategy is a pulse-width controller that has the advantage of being easy to operate along with any output-voltage regulator that modifies the switching frequency. The pulse width controller has shown to be useful to improve operation of the converters leading to a more efficient transferring of energy to the output and reducing conduction losses.

Mario Lucio da Silva Martins [2] Discussed about the complete analysis for ZVT PWM converters with an auxiliary resonant circuit converters with an resonant auxiliary circuit (ZVT-RAC). The analysis is based on a common circuit topology with this generic topology; the analysis can be easily generalized for any ZVT PWM with an RAC converter.

Bhajana V.V. Subrahmanya Kumar [3] and S Rama Reddy conducted an exhaustive comparative

analysis between a conventional ZVS converter and the ZVS-ZCS bidirectional DC-DC Converters.

Milan M.Jovanovic [4] has summarized the basic properties of resonant, quasi-resonant, multi-resonant and soft-switching PWM techniques. In addition, the merits and limitations of each technique have been discussed.

Hiroshi Nakajima and Haruhiko Matsushita [5] proposed a "variable capacitance device." Its capacitance can be varied by an Independent dc control voltage. And it was confirmed that the Schwarz circuit and the buck-type resonant converter can be regulated under the fixed switching frequency by applying "variable capacitance device" to the capacitor of the LC resonant tank.

M. L. Martins, J. L. Russi and [6] H. L. Hey presents a classification methodology of the ZVT soft transition technique, which is based on different ways of implementation of the auxiliary circuit voltage source. The merits and limitations of each class are presented and their key features and characteristics are discussed.

II.PROPOSED ZVT BUCK CONVERTER

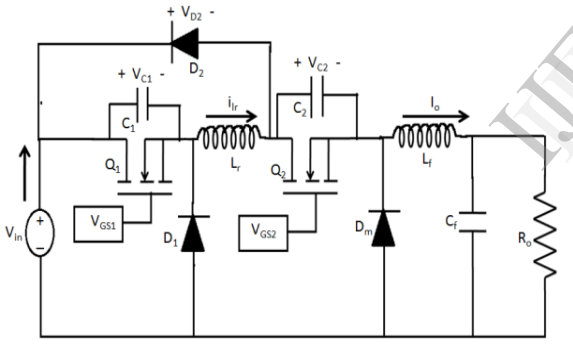


Fig.2. 1 Circuit Diagram

The proposed ZVT soft-switching buck converter (Fig. 1) has two additional diodes D1 and D2, an auxiliary power switch Q2, a resonant capacitor C2, and an inductor Lr in addition to those in a traditional ZVS buck converter. These two clamp diodes are used to extend the resonance time on the main switch and overcome the weakness of excessively short resonance time in conventional ZVS and ZCS converters.

The ZVT–PWM approach uses a shunt resonant branch to generate soft switching. During switching transition, the shunt resonant tank creates a partial resonance for obtaining ZVS. When the switching transition is completed, the shunt resonant tank is disabled such that the operation of the ZVT–PWM converter resembles that of a conventional PWM converter. Thus, the ZVT–PWM converter can achieve soft switching without increasing the voltage stresses of active power switches.

Soft-switching power converters can be classified as ZVS/ zero-current-switching (ZCS) PWM power converters or ZVT/ZCT soft-switching power converters. The auxiliary switch forms a resonant loop, decreasing the voltage or current on the power switch to zero, which switches before the main power switch is switched to the conducting state. The ZVT/ZCT soft-switching power converter decreases component stress and conduction losses by reducing the voltage/current and minimizes switching losses.

III. MODES OF OPERATION

A. Mode 1 Lr-C1 resonant stage (0 ≤ t ≤ t0)

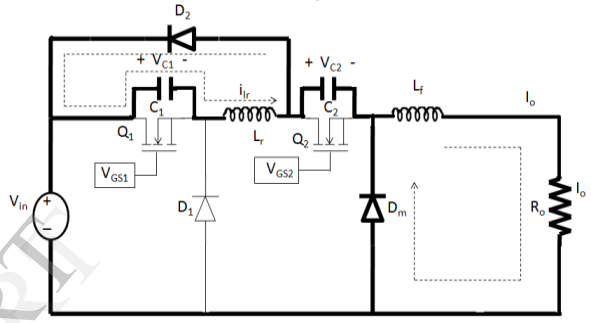


Fig 3.1 Switching Stage Mode 1 (0 ≤ t ≤ t0)

Power switch Q2 is assumed to be cut off, and power switch Q1 is initially switched from the ON state to the cutoff state. Diode D1 is still cut off; D2 and Dm are maintained as turned on due to the initial value of the capacitor voltage VC1.In this initial stage, the capacitor voltage VC2 is fixed at Vin, and Lr– C1 forms a serial resonant circuit.

The circuit equations are

$$L_r \frac{dil_r(t)}{dt} = -V_{c1}(t) \quad (3.1)$$

$$C_1 \frac{dV_{c1}(t)}{dt} = -ILr(t) \quad (3.2)$$

$$V_{c2}(0) = V_{in} \quad (3.3)$$

The solution to the circuit equations is determined by initial conditions

ILr (0) =Io (3.4)
VC1 (0) =0 (3.5)
VC2 (0) = Vin (3.6)
ILr (t) =Io cos (ω1t) ` (3.7)
VC1 (t) =IoZ1sin (ω1t) (3.8)
VC2 (t) =Vin (3.9)

At the input voltage and prevents the terminal voltage of power switch Q1 from exceeding Vin.

Where $Z_1 = \sqrt{L_r/C_1}$; $\omega_1 = \frac{1}{\sqrt{L_r C_1}}$

The duration in Mode I can be determined from boundary condition VC1 (t0) = Vin

$$T_a = \frac{1}{\omega 1(\sin^{-1}\alpha)} \qquad (3.10)$$

Where $\alpha = \frac{V_{in}}{I_0 Z_1}$

When capacitor voltage VC1 is increased to Vin, diode D1 is conducting mode under forward bias and enters Mode 2 VC1 is then clamped.

B. Mode 2 Inductor Lr in discharging state (t0 ≤ t ≤ t1)

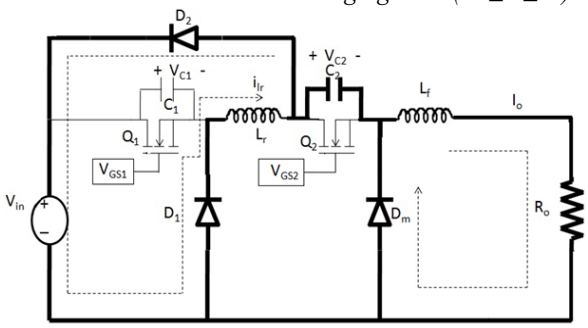


Fig 3.2 Switching Stage Mode 2 (t0 ≤ t ≤ t1)

Power switches Q1 and Q2 are both maintained at cutoff, diodes Dm and D2 keep conducting, and diode D1 is switched on Voltages VC1 and VC2 remain at Vin, causing the transient to stop, and diodes D1 and D2 remain conducting. The terminal voltage across the resonant inductor becomes Vin. Hence, the inductor current ILr linearly decreases to zero prior to Multi resonance to prevent ILr from surging, thereby overcoming the short comings associated with large voltage/current in a resonant converter. Therefore, diodes D1 and D2 are clamp diodes. The circuit equations with initial values are given as follows:

$$L_r \frac{diLr(t)}{dt} = -V_{in} \qquad (3.11)$$

$$ILr((t0) = Io\sqrt{(1-\alpha^2)} \qquad (3.12)$$

$$VC1\ (t0) = Vin \qquad (3.13)$$

$$VC2\ (t0) = Vin \qquad (3.14)$$

$$ILr((t) = Io\sqrt{(1-\alpha^2)} - \frac{V_{in}}{L_r}t \qquad (3.15)$$

$$VC1\ (t) = VC2\ (t) = Vin \qquad (3.16)$$

The solutions are obtained using (3.13) and (3.14) and the waveform is that with period Tb (figure 3.9**).** The time interval of Mode II can be determined from boundary condition ILr (T_b) = 0.

$$T_b = t_1 - t_0 = \frac{L_f I_0 \sqrt{1-\alpha 2}}{V_{in}} \qquad (3.17)$$

When IL_r equals zero, Mode 3 is entered.

C. Mode 3 Three components in Multi Resonant Stage (t1 ≤t ≤ t2)

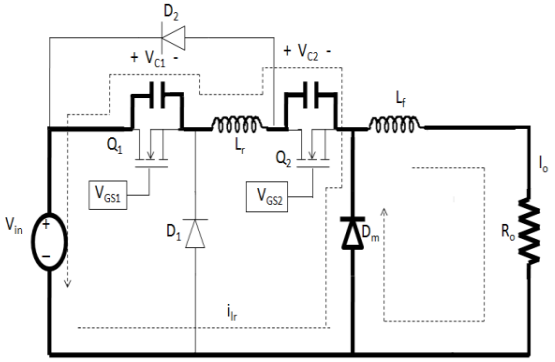


Fig 3.3 Switching Stage Mode 3 (t1 ≤ t ≤ t2)

Power switches Q1 and Q2 in this stage remain in the cutoff state, and the output current still flows through Dm, which is still conducting. Diodes D1 and D2 are cut off, as ILr cannot flow in reverse through D1 and D2 because the inductor current flowing through Lr is negative. Fig. 3.4 presents the equivalent circuit corresponding to Mode III. Components C1, Lr, and C2 begin resonating; the circuit equations are specified as follows:

$$L_r \frac{diLr(t)}{dt} = -V_{in} - V_{c1}(t) - V_{c2}(t) \qquad (3.18)$$

$$ILr\ (t1) = 0 \qquad (3.19)$$

$$C_1 \frac{dVc1(t)}{dt} = ILr(t) \qquad (3.20)$$

$$V_{C1}\ (t) = V_{in} \qquad (3.21)$$

$$C_2 \frac{dVc2(t)}{dt} = ILr(t) \qquad (3.22)$$

$$V_{C2}\ (t) = V_{in} \qquad (3.23)$$

The solutions are determined as follows:

$$I_{Lr}(t) = \frac{V_{in}}{Z_r}\sin\omega_r t \qquad (3.24)$$

$$V_{c1}(t) = \frac{V_{in}}{C_1 + C_2}[C_1 + C_2 \cos\omega_r t] \qquad (3.25)$$

$$V_{c2}(t) = \frac{V_{in}}{C_1 + C_2}[C_2 + C_1 \cos\omega_r t] \qquad (3.26)$$

Where $\omega_r = \frac{1}{\sqrt{L_r C_r}}$

The time duration of Mode III can be determined from boundary conditions

$$I\ Lr\ (t2) = VC1\ (t2) = VC2\ (t2) = 0 \qquad (3.27)$$

$$Tc = t_2 - t_1 = \frac{\pi}{\omega_r} \qquad (3.28)$$

At this moment, I Lr flows in reverse, and VC1 and VC2 decline slowly until all three simultaneously equal zero and then enter Mode IV. The large current in the ZVT converter is unique during this stage. Current iDm in this stage slightly exceeds the output current

$$|iDm,max| = Io + Vin/Zr \approx Io. \qquad (3.29)$$

D. Mode 4 Inductor Lr in charging state ($t_2 \le t \le t_3$)

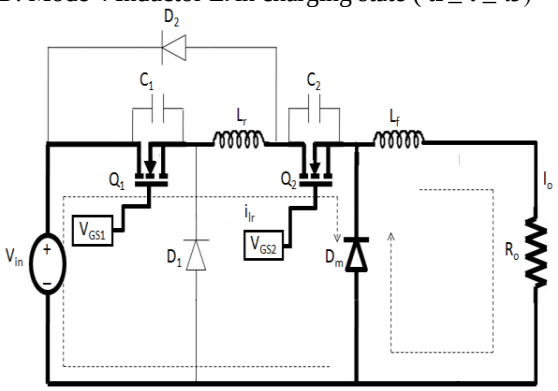


Fig 3.4 Switching Stage Mode 4 ($t_2 \le t \le t_3$)

The ZVS occurs when power switches Q1 and Q2 in the additional drive circuit is simultaneously conducting at zero voltage. Therefore, diode Dm is conducting; diodes D1 and D2 remain in their former state, since I Lr cannot suddenly increase [Figure 3.5]. Inductor current I Lr linearly increases, as the terminal voltage across the inductor is Vin. The circuit equation and initial condition are given as follows:

$$L_r \frac{di_{Lr}(t)}{dt} = V_{in} \quad (3.30)$$

$$I_{Lr}(t2) = 0 \quad (3.31)$$

$$VC1\ (t2) = 0 \quad (3.32)$$

$$VC2\ (t2) = 0. \quad (3.33)$$

The solutions are determined as follows:

$$I_{Lr}(t) = \frac{V_{in}}{L_r} t \quad (3.34)$$

$$VC1\ (t) = VC2\ (t) = 0 \quad (3.35)$$

The period of Mode IV can be determined from boundary condition I Lr (Td) = 0

$$T_d = t_3 - t_2 = \frac{L_r I_0}{V_{in}} \quad (3.36)$$

When inductor current I Lr linearly increases to I0, the diode current IDm = i0 – iLr = 0, diode Dm is cut off, and Mode 5 is entered.

E. Mode 5 Conduction Rate Control Stage ($t3 \le t \le t4$)

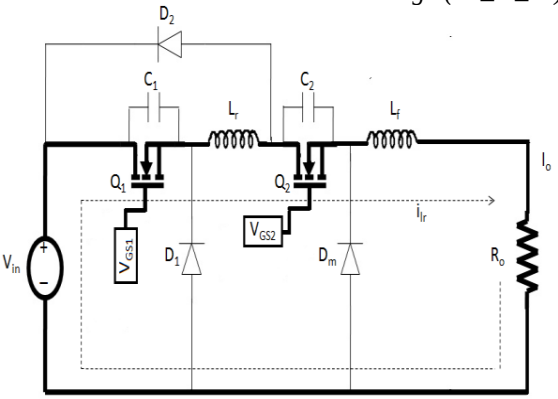


Fig 3.5 Switching Stage Mode 5 ($t3 \le t \le t4$)

Diode Dm is switched to cutoff, and diodes D1 and D2 remain cut off [Figure 3.6]. These states remain until power switch Q2 is switched to the cutoff state using the drive circuit.

The circuit equation and initial conditions are given as follows:

$$I\ Lr\ (t3) = I0 \quad (3.37)$$

$$VC1\ (t2) = VC2\ (t3) = 0. \quad (3.38)$$

This stage is exactly the conduction period of the ZVT soft switching buck converter. The output voltage can be regulated by controlling the time interval of this stage

$$Te = t4 - t3 = DTs. \quad (3.39)$$

When power switch Q2 is turned off, Mode 6 is entered.

F. Mode 6 Capacitor C2 in charging state ($t4 \le t \le t5$)

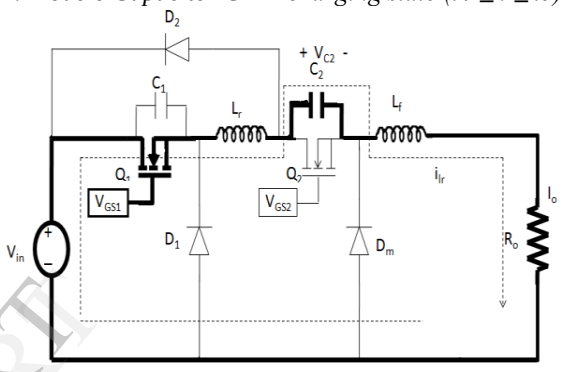


Fig 3.6 Switching Stage Mode 6 ($t4 \le t \le t5$)

Power switch Q1 remains turned on during this stage, power switch Q2 is cut off under the zero voltage switching condition, and diodes Dm, D1, and D2 are maintained in their original cutoff states [Figure 3.7]. The voltage VC2 (t) linearly increases as capacitor C2 is charged by a constant inductor current I0.

The circuit equations and initial conditions are described as follows:

$$ILr\ (t4) = Io \quad (3.40)$$

$$VC1\ (t4) = 0 \quad (3.41)$$

$$C_2 \frac{dV_{c2}(t)}{dt} = ILr(t) \quad (3.42)$$

$$VC2\ (t4) = 0. \quad (3.43)$$

The solutions are determined as follows:

$$I\ Lr\ (t) = Io \quad (3.44)$$

$$VC1\ (t) = 0 \quad (3.45)$$

$$VC2\ (t) = (I0/\ C2)\ t. \quad (3.46)$$

The time duration of this stage can be derived using the following and boundary condition

$$VC2\ (tf) = V_{in}$$

$$T_f = \frac{C_2}{I_0} V_{in} \quad (3.47)$$

When voltage VC2 linearly increases to Vin, Mode 7 is entered.

G. Mode 7 Flywheel Stage (t5 ≤ t ≤ t6)

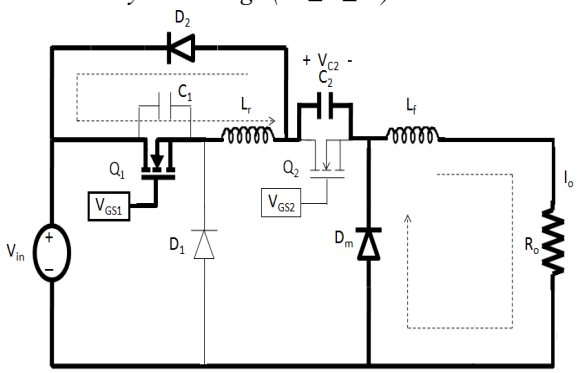


Fig 3.7 Switching Stage 7 (t5 ≤ t ≤ t6)

Power switches Q1 and Q2 and diode D1 maintain their earlier states at this stage. Diode Dm begins to conduct current I0 when the voltage of VC2 linearly increases to Vin. Diode D2 begins conducting at the same time and forms a current loop of I Lr. Therefore, VC2 and ILr are clamped at Vin and I0, respectively [Figure (3.8)]. Voltages VC1 and VC2 and current I Lr again enter the steady State, in which they maintain constant values associated with the flywheel stage of the ZVT soft-switching buck converter. The waveforms of the various voltages in the Tg stage figure 3.9 can be expressed as follows

$$I\,Lr\,(t) = Io \qquad (3.48)$$

$$VC1\,(t) = 0 \qquad (3.49)$$

$$VC2\,(t) = Vin. \qquad (3.50)$$

The duration of this stage is calculated by

$$Tg = Ts - Ta - Tb - Tc - Td - Te - Tf.$$

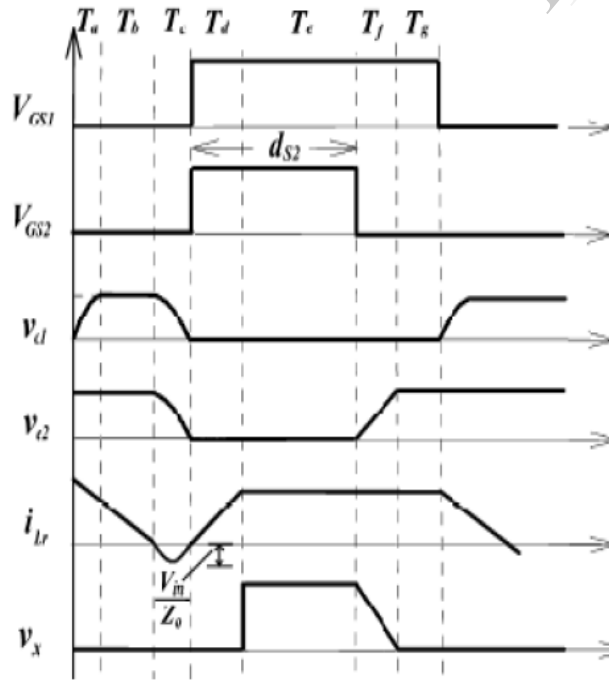


Fig 3.8 Timing Sequence and Waveform Diagram

A complete period is finished when power switch Q_1 is again turned off by the periodic signal. The next period is begin as shown in figure 3.8

IV.SIMULATION RESULTS

For conventional ZVS Resonant Buck

The inductor L_r and C_f forms the resonance circuit.

$$\omega = \frac{1}{\sqrt{L_r C_f}};$$

Let C_f = 1μF. Duty cycle D=0.6

$\omega = 2\pi f$.

f=10 kHz

L_r=0.2533mH.

C_1=1μF.

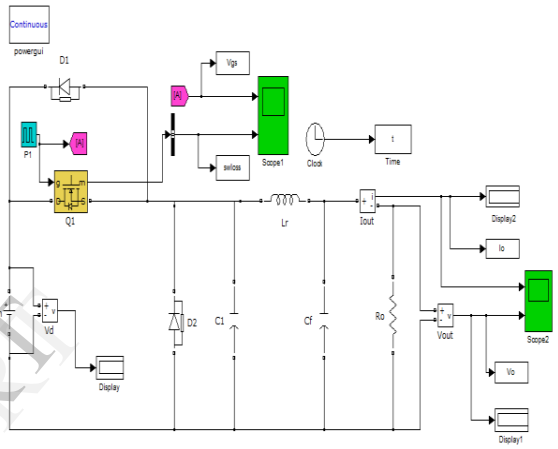


Fig 4.1 Simulation circuit of a ZVS resonant Buck Converter

The proposed converter is simulated in MATLAB SIMUINK with 10 kHz as the switching frequency and ZVS resonant buck converter is also simulated in the same switching frequency and results are compared. Figure 4.1 shows the circuit for ZVS resonant buck converter.

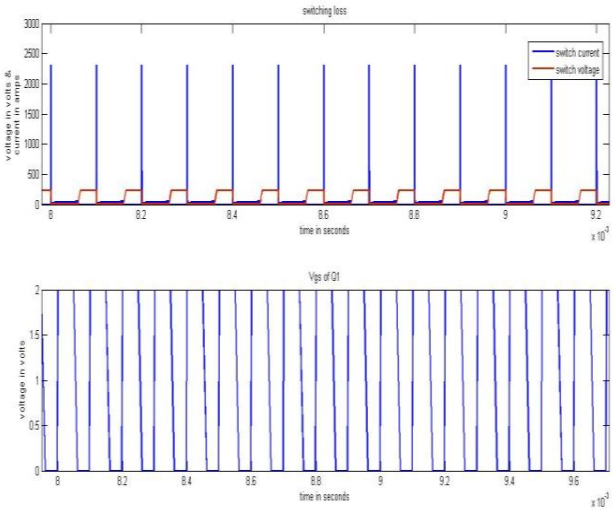


Fig 4.2 switching loss and control gate signal

Fig 4.2 shows the switching loss (overlap of current and voltage) and the gate signal for the Q1 of the ZVS resonant buck converter.

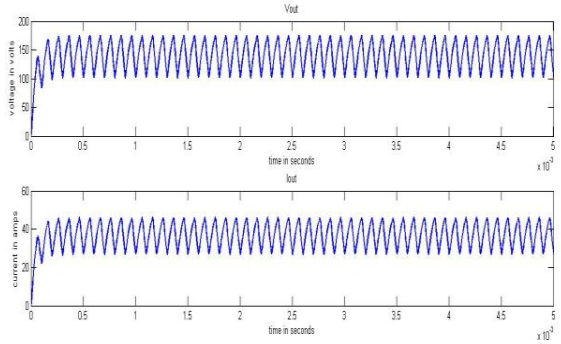


Fig 4.3 Output Voltage and Output load Current

Fig 4.3 shows the output voltage and current values of the conventional ZVS buck converter.

For ZVT PWM Buck Converter:

The inductor L_r C_2 and L_f C_f forms the resonance circuit. Duty cycle D=0.6

$$\omega = \frac{1}{\sqrt{L_r C_f}};$$

Let C_f = 1µF. C_2=100 µF

ω =2πf.

f=10 kHz

L_f=0.2533mH L_r=2.533µH

C_1=1µF.

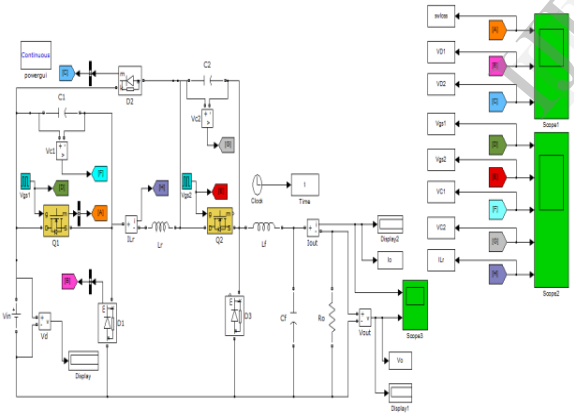


Fig 4.4 Simulation Circuit of a ZVT PWM Buck Converter

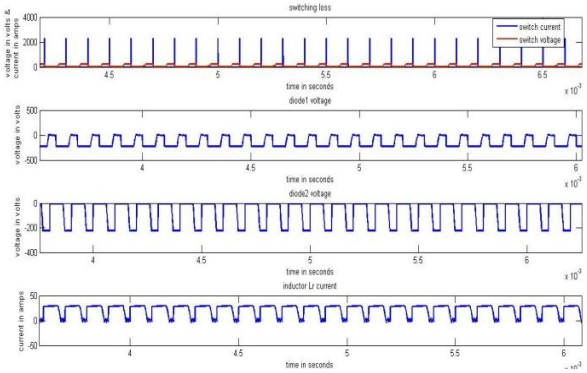


Fig 4.5 Switching loss, Diode voltage and Inductor current

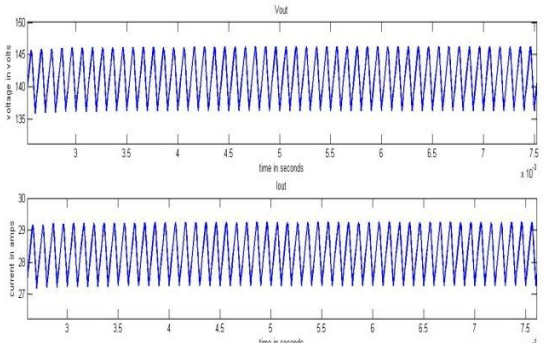


Fig 4.6 Output Voltage and Output load Current

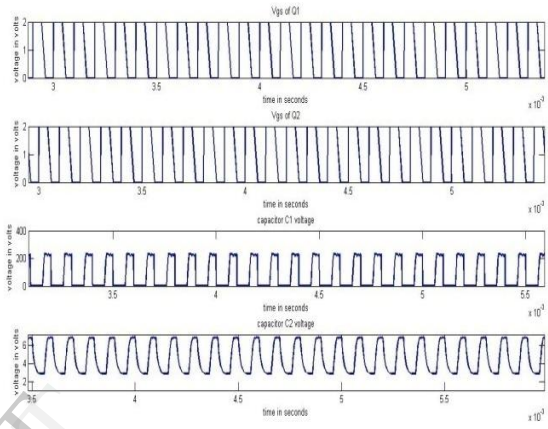


Fig 4.7 Gate Pulse and Capacitor Voltage

Fig 4.4 shows the simulation circuit of the proposed ZVT PWM buck converter, simulated at the frequency rate of 10 kHz with the duty cycle ratio of D=0.6.

Fig 4.5 shows the switching loss, diode D1, D2 voltage and the inductor Lr current. Fig 4.6 is the output voltage and current of the proposed converter and Fig 4.7 indicates the pulse rates of the Q1 and Q2, capacitor VC1 and VC2 voltage levels.

The switching losses in ZVT PWM converter is considerably reduced compare to the ZVS resonant converter. To know it clearly only one cycle is compared between the ZVS and ZVT converter for same operating conditions and same time period range. The overlap between the voltage and current determines the loss amount. Our aim is to make the overlap as much as low.

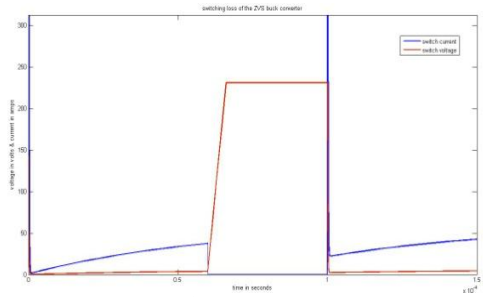


Fig 4.8 Switching loss of the ZVS resonant buck converter

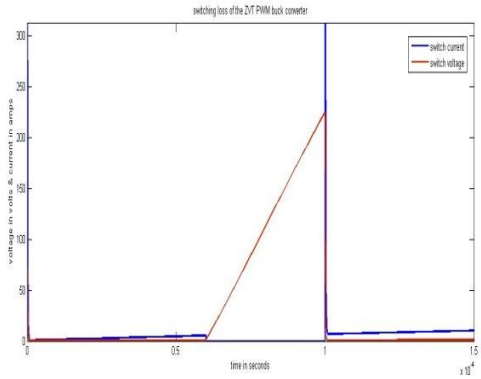


Fig 4.9 Switching loss of the ZVT PWM buck converter

Fig 4.8 shows switching loss ZVS resonant buck converter and Fig 4.9 shows the switching loss of the ZVT PWM buck converter. From these two results the loss in the proposed converter is less and the stress is gradual rise i.e the voltage rise in ZVT PWM buck converter, but in ZVS resonant buck sudden increase of the voltage rise. Also the current almost reaches to zero in the proposed converter but not in the case of ZVS resonant converter.

V.CALCULATION OF THE SWITCHING LOSS

The average switching power loss Ps can be approximated to

$$P_s=1/2\ V_d I_o f_s (t_{c\ (on)} + t_{c\ (off)})$$

V_d = Input voltage applied

I_o = Output load current

f_s = Switching frequency

$t_{c\ (on)}$ = On time duration of MOSFET

$t_{c\ (off))}$ = Off time duration of MOSFET.

Table: 5.1 ZVS resonant buck result values

$t_{c\ (on)}$=0; $t_{c\ (off)}$=0.0000003 sec; V_d=230V

Pulse Width (Ton) (%)	O/P voltage (Vo) (Volts)	O/P Load current (Io) (Amps)	Switching Loss (P_s) (Watts)	Efficiency (η) (%)
10	15.33	3.066	1.0570	6.67
20	23.71	4.742	1.6359	10.31
30	35.66	7.132	2.4605	15.50
40	51.24	10.25	3.5362	22.27
50	71.00	14.20	4.8990	30.86
60	95.82	19.16	6.6102	41.67
70	126.70	25.34	8.7423	55.08
80	164.20	32.84	11.3298	71.39
90	295.10	41.03	14.1553	89.17

Table 5.1 shows the ZVS buck converter resultant values for the different pulse width values.

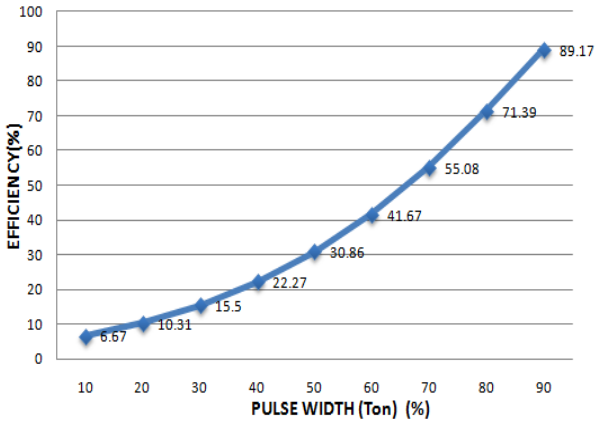


Fig 5.1 Pulse width vs Efficiency plot

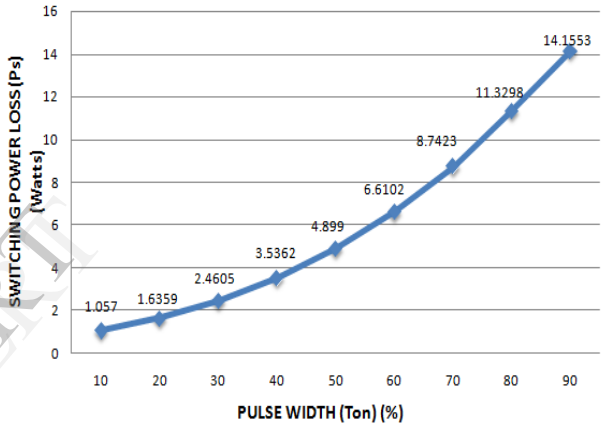


Fig 5.2 Pulse width vs switching power loss plot

Similarly for the proposed ZVT PWM converter the switching power loss can be calculated.

Table: 5.2 ZVT PWM resonant buck result values

$t_{c\ (on)}$=0; $t_{c\ (off)}$=0.0000001 sec; V_d=230V

Pulse Width (Ton) (%)	O/P voltage (Vo) (Volts)	O/P Load current (Io) (Amps)	Switching Loss (P_s) (Watts)	Efficiency (η) (%)
10	41.53	8.30	0.9551	18.05
20	55.31	11.06	1.2719	24.04
30	70.60	14.12	1.6238	30.59
40	87.06	17.41	2.0021	37.85
50	104.30	20.87	2.4000	45.34
60	122.30	24.47	2.8140	53.17
70	140.90	28.18	3.2407	61.26
80	159.90	31.98	3.6777	69.52
90	180.00	39.93	4.1319	78.26

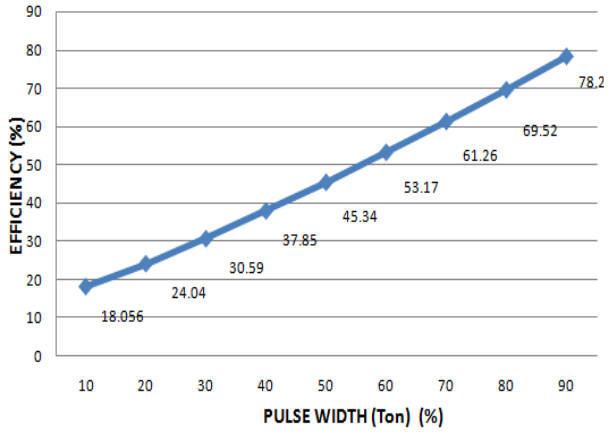


Fig 5.3 Pulse width vs Efficiency plot

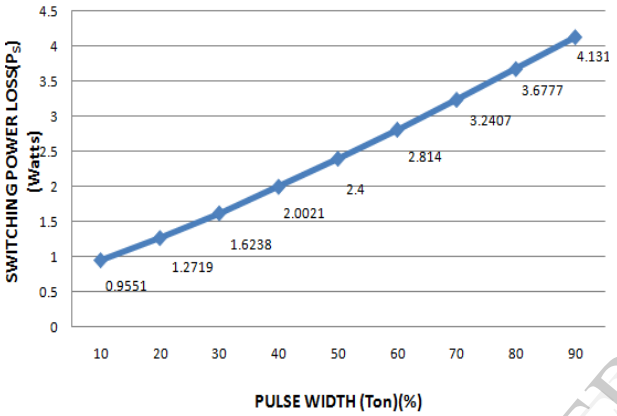


Fig 5.4 Pulse width vs switching power loss plot

Fig 5.3 and 5.4 shows the Pulse width vs Efficiency and Pulse width vs switching power loss graphs.

From the Fig 5.1 and 5.3 can conclude that ZVT PWM buck converter contains less power loss compared to the ZVS resonant buck converter, and from fig 5.2 and 5.4 efficiency also improved in ZVT PWM buck converter.

VI.CLOSED LOOP CONTROL

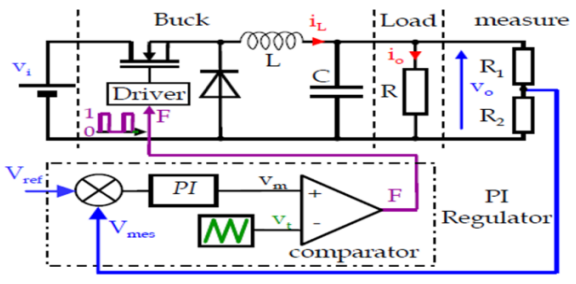


Fig 6.1 Schematic of closed loop control

Fig 6.1 illustrates closed loop structures that consist of a PI regulator and a driver circuit.

The PWM generator acting as the driver circuit can be designed in number of ways one of the simple techniques is given here.

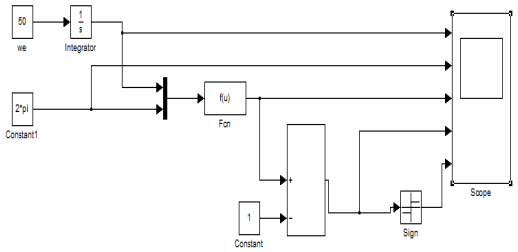


Fig 6.2 Simulation circuit of a PWM generator

This PWM generator produces triggering signals for the power switch, is decided by the Carrier frequency and PI regulator output value.

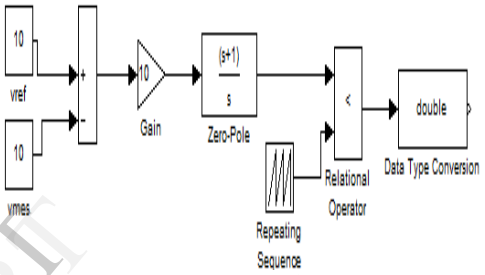


Fig 6.3 Schematic of a PI controller

Fig 6.3 shows the schematic model of a PI regulator with zero pole structure with relational operator condition, the repeating sequence value fixed at the rate of a 10 voltage. Whenever the zero pole block value voltage amount is less than the repeating sequence the output of the relational operator is one and is converted in the data format at data type conversion block.

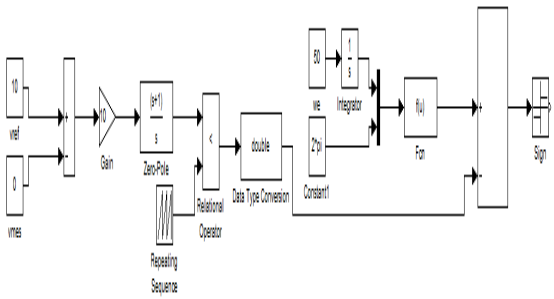


Fig 6.4 Simulink Closed Loop Structure

Fig 6.4 gives the complete closed loop structure integrated with PWM generator and the PI regulator. For simplicity purpose here after PWM block created as asubsystem2 and PI regulator block created as the subsystem 3.

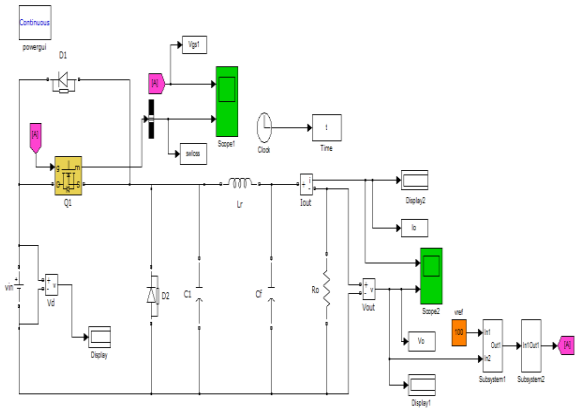


Fig 6.5 Simulation circuit of closed loop ZVS resonant buck converter

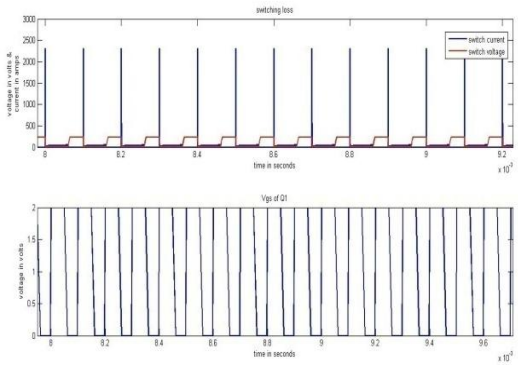


Fig 6.6 Closed loop results for switching loss and Vgs of Q1 switch of the ZVS resonant buck converter

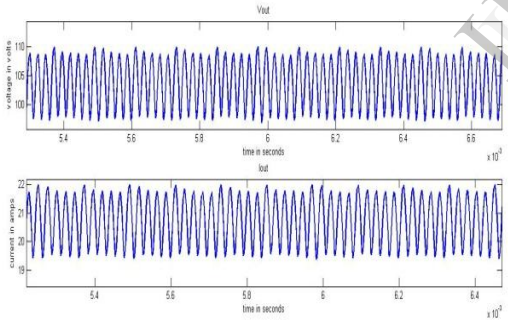


Fig 6.7 Closed loop results for output voltage and output load current of the ZVS resonant buck converter

Fig 6.5 shows the closed loop simulink model of the conventional ZVS resonant buck converter, in that the reference voltage is fixed at the value of a 100 voltage. Also the output voltage reaches closer to the 100 voltage, the switching loss and automatically generated gate pulse for Q1 is shown in fig 6.6.Fig 6.7 shows the output voltage and output current of the closed loop ZVS resonant buck converter, the output voltage is closer to the reference value what is fixed in the simulation.

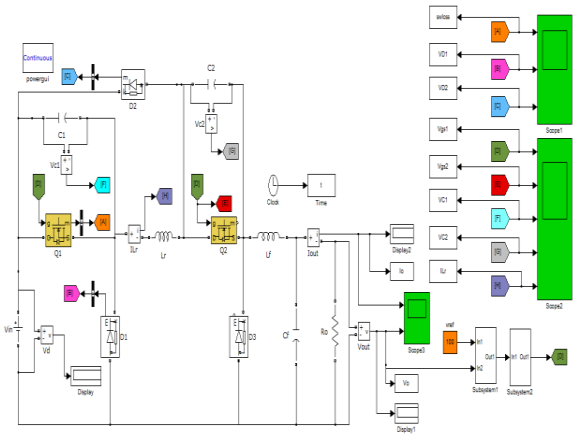


Fig 6.8 Simulation circuit of closed loop ZVT PWM resonant buck converter

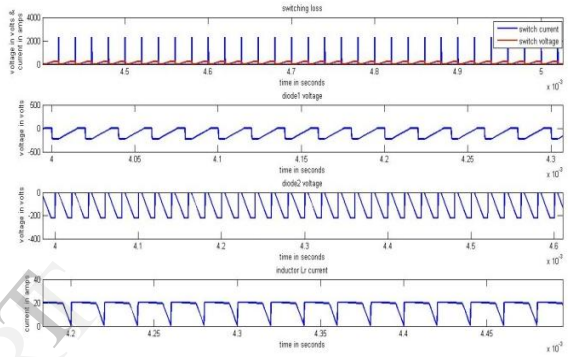
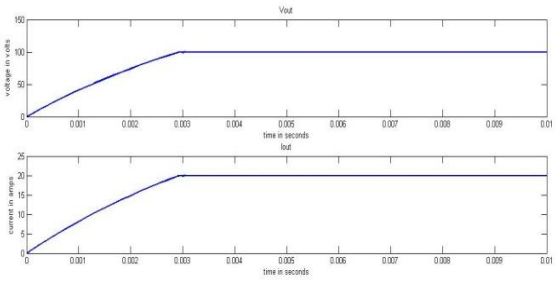


Fig 6.9 Closed loop results for switching loss and diode voltage VD1, VD2 and inductor current ILr of the ZVT PWM resonant buck converter



6.10 Closed loop results for output voltage and output load current Of the ZVT PWM resonant buck converter

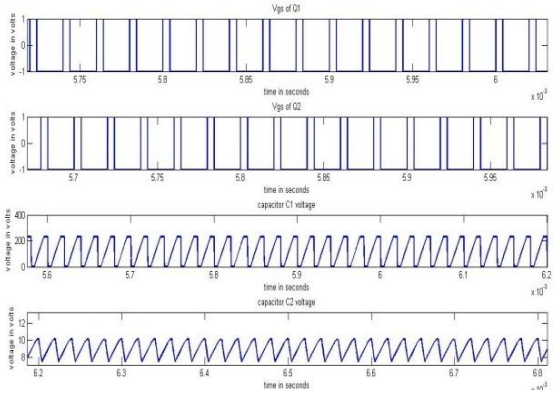


Fig 6.11 Closed loop results for Vgs of Q1, Q2 and capacitor voltage VC1, VC2 of the ZVT PWM resonant buck converter

Fig 6.8 shows the closed loop simulink model of the proposed ZVT PWM resonant buck converter. Reference voltage is fixed in the rate of a 100 voltage in the ZVT PWM buck converter. Fig 6.9 shows the switching losses, diode voltage1, diode voltage2 and inductor current ILr. The switching losses in ZVT PWM converter is much reduced than the ZVS resonant buck converter. Fig 6.10 shows the output voltage and output load current result, the voltage and current, is closer to the reference value than the ZVS resonant buck converter. Fig 6.11 shows the gate triggering pulses for the switch Q1, Q2 and capacitor voltage VC1, VC2.the gate pulses for the Q1 and Q2 is automatically generated to achieve the reference voltage result. The voltage is very closer to reference voltage also the switching losses are reduced and increased efficiency in the proposed converter but not in the case of previous ZVS resonant buck converter.

VII. CONCLUSION

A Soft switched low-stress ZVT-PWM buck converter is designed, according to the test result the primary switch and the auxiliary switch are turned on and turned off, respectively at zero voltage. Furthermore all components are operated under soft switching to decrease the high voltage/current stresses caused by the input voltage of the resonant capacitor and hence decreasing power dissipation from power switches by extending the resonant time of the main switch. The result are then compared with the switching losses of a ZVS resonant buck converter and is found that the switching losses in ZVT-PWM buck converter are lesser than the ZVS resonant buck converter and also the closed loop was designed for the ZVS and ZVT PWM buck converter..

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