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Improve Efficiency Doherty Power Amplifier (DPA) by Using Stacked Field Effect Transistor (FET) Cells at 28GHz Frequency

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***Abstract*—The DPA is thought to be a promising solution in the design of Ka-band power amplifiers ranging from 26.5-40 GHz for the significant advantages it has due to low-cost production and easy maintenance and installation within radio transmission units, In addition to its effective role in both efficiency and output power with reasonable gain values .This work explains how to design stacked FET DPA and Study the effect of standard parameters on stacked FET topology to operate Doherty, which are: gate capacity and stacked transistor bias voltage, where these two parameters determine the output power of the amplifier, the power added efficiency (PAE) and the flatness of the power gain. Stacked transistor circuits can be found in many forms and used for various applications such as 5G communications applications, Doherty's symmetrical power amplifier model is designed in this work using GaAs technology to work at 28GHz.The simulation results showed a gain of up to 11.6db and output power of about 30dbm with a 66% PAE max and a 35% PAE at 6-dB Back-Off from PSat.**

***Keywords*—5G; Efficiency; Ka-band; Stacked-FETs topology; Doherty power amplifier (DPA).**

I. INTRODUCTION

The Ka-band, especially the 28 GHz frequency, is the main evolving frequency for the next generation of wireless communications. Thus, in systems with very high peak-to-average power ratio (PAPR), such as 5G systems, amplification is a primary problem for low-efficiency amplifiers driven by high-PAPR signals in systems with a very high peak-to-average power ratio (PAPR). Doherty architecture, which uses a multi-transistor approach, is a solution to this problem and plays a role in improving the efficiency of the back-off output power.

The equity of semiconductor technology used in the manufacture of 5G potential transistors plays a significant role in determining the output power of amplifiers using gallium arsenic (GaAs) technology for two main reasons, as illustrated in Figure (1)[1]. GaAs technology is the most appropriate in terms of output efficiency and power provided by the design at the transistor level, with an operating frequency of 28 GHz.

However, the output power is limited by the low breakdown voltage of GaAs and stacked FETs have been proposed as one of the most effective solutions to this problem. Therefore, emphasis is placed on the analysis of the Stacked-FET topology when used in Doherty's amplifiers to achieve appropriate output power, high efficiency, and the greatest gain. This study also included the design of a Doherty amplifier using (stacked FET) transistors, focusing on the capacity of the gate capacitor in a common gate (CG) architecture, as indicated in [2]. This capacitor helps mitigate the effect of the voltage swing between the drain and gate in the stacked transistors of the transistor cell (TC). This voltage swing is one of the main challenges in stacked-FET to pologies.

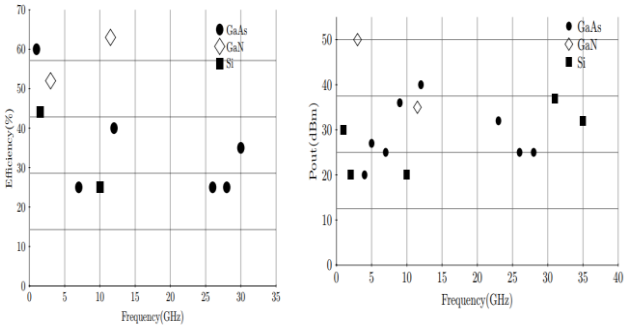

Fig 1: Limited performance of RFPA amplifier transistors using semiconductor technology [1].

II. COMPREHENSIVE THEORETICAL BASIS

*A.*Relevant Literature

We found designs for RFPA amplifiers based on stacked-FET topology and using (GaAs) technology in the literature [3.4.5.6] and based on GaN technology in the literature [7.8]. Doherty's two-stage amplifier was introduced using a stacked-FET topology [9]. This research proves, for the first time, the importance of two critical parameters in the Stacked-FET topology that must be designed specifically for Doherty's architecture, including the gate voltage and stacked transistor bias voltage (Stacked-FET). These parameters are determined by the output power of the DPA, power added efficiency (PAE), and linear gain of the resulting power.

Moreover, an article [9] presented a dual-driving topology input signal to enhance the gain of the amplifier without reduction (PAE) through a proposed bias network to address the high leakage current of the gate in enhancement mode (E-mode).

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B.Stacked-FET topology concept

Stacked transistor amplifiers are defined as balanced cascades. If an equal number of transistors are stacked, the breakdown voltage available for each transistor increases by an amount equal to N. Owing to this configuration, the voltage swing levels of each transistor were integrated into the stack. In the stack, this combination increases the overall voltage signal level in the stack to N times higher than the voltage swing when using a single transistor. All transistors in the stack have the same DC supply and RF drain current, which provide an ideal state (the ideal case corresponds to the complete stability of the circuit without loss of amplification phases), where the output power is greater than the output power when only one transistor is used.

Stacked transistor circuits can exist in many forms and can be used for many applications, such as 5G communication applications, as reported in [9]. Both the gate bias voltage and the bias voltage were used to determine the performance of the amplifier. In short, "Stacked-FET" is a useful solution in Radio Frequency (RF) amplifier applications where the level of voltage swing can exceed the value of the transistor breakdown voltage, requiring the use of more than one transistor to offset this increase in the level of voltage swing, i.e., keeping the RF amplifier circuit within the safety and immunity requirements of combustion or thermal damage.

C.Stacked-FET topology in RF power amplifiers

The concept of a Stacked-FET topology is based on the use of many transistors rather than one in the amplifier; therefore, we have what is called a transistor cell (TC), which is composed of several transistors connected in a specific stack architecture, therefore, a conventional power amplifier can be converted into another form based on the stacked-FET topology as shown in Fig.2.

In this study, we are not concerned with analyzing the working principle of stacked-FET topology, but directly applying it as an engineering principle in TC transistors to be applicable in a Doherty amplifier rather than using a single transistor in both the main amplifier and the auxiliary amplifier, and then simulating the performance as a possible solution in designing "Doherty" amplifiers in 5G applications, which work on millimeter-wave frequencies; we followed [9] in the strategy of Doherty amplifier circuit design, including operating frequency 28 GHz but with different semiconductor technology, where we used GaAs technology rather than GaN technology used in [9].

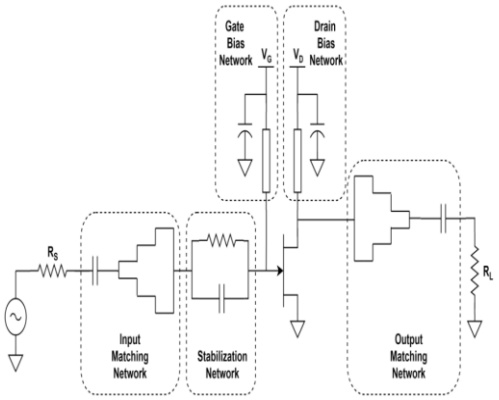

Fig. 2: A general principle of RFPA amplifier based on Stacked-FET topology

To simplify the simulation model and achieve our goals for studying performance, we depend on Fig. (3) [3] to design the TC of a Doherty amplifier. This is similar to the TC architecture reported in previous studies [6.9.10]. especially, the authors in [6.10] explain in detail the hypothesis of multiplication optimum impedance value, we depend on this principle In the load pull process in the stack output where we use a basic assumption in our design of a Doherty amplifier based on the Stacked-FET topology which is demonstrated by considering the optimum impedance value that the TC should see at its output in the stack will be equal to N times to value of the ideal impedance If the load pull procedure is with a single FET transistor.

Fig. (3) is a special case of Fig. 24.3 [3], from which we constructed a TC for both the main and auxiliary Doherty amplifier based on the Stacked-FET topology. In Fig. 3, the box blocks IMN, SN, and BN represent the input matching network (IMN) at the TC cell input, stability network (SN), and bias network (BN) of the gate transistor, respectively, and are used to determine the operating class of the main or auxiliary amplifier when using the TC adopted in the Doherty architecture. In the simulation, the resistance Rgbais (the load resistance of the supply voltage that supplies the stacking transistors with a supply separate from the DC bias in the conventional amplifier configuration) and capacitor CgX, N were set by tuning for the optimum performance in terms of efficiency, output power, and gain.

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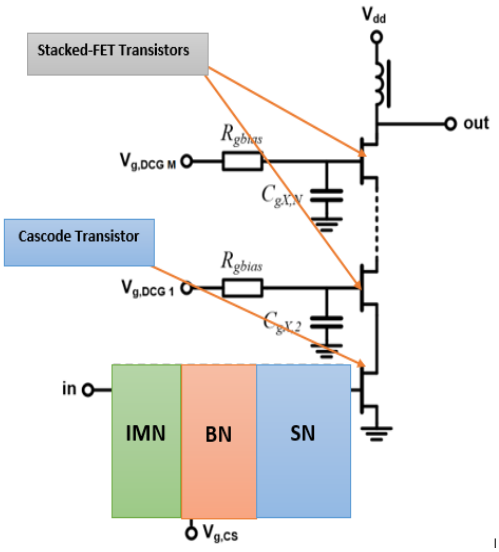

Fig. 3: TC configuration in this work to form an amplifier stage based on Stacked-FET [3].

III. METHOD

A.Determine optimal impedance on the output of Stacked-FET topology

The value of the optimal impedance of the TC output that is designed based on stacked-FET topology can be determined to be double the optimal impedance value that is shown on the Cascode transistor output, as explained in Fig. (5), which is considered to be N= 2. Therefore, to determine the optimal impedance value of the TC cell output, we first need to determine the optimal impedance in the TC cell of the Cascode transistor output, as long as the TC cell forms the primary transistor in both the main and auxiliary amplifiers in Doherty amplifier based on the Stacked-FET topology, the optimal impedance can be determined through pull-load technology.

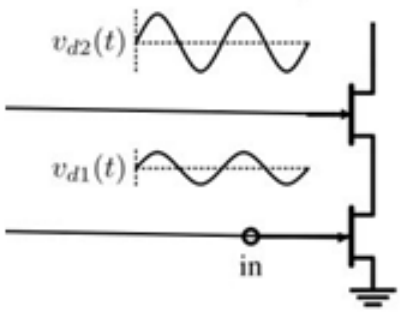

Fig. 4: The relationship between the optimal impedance of a Stacked-FET topological cell (N = 2) with the optimal Cascode output impedance.

B.Units Design of a stable Cascode transistor in stacked-FET topological cell.

The necessary and sufficient condition for the unconditional stability of the RFPA amplifier is the use of the μ parameter test, which is expressed by the swing presented in Eq.1:

Eq.1

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{12}S_{21}|} > 1;\ \Delta = S_{11}S_{22} - S_{12}S_{21}.$$

The μ parameter must be larger than one so that the amplifier is stable at a basic operation frequency of 28 GHz. Based on the challenge of stacking-FET-amplified stability, it is necessary to add a stability network that consists of a resistance and capacitor that is connected as branches and positioned at the Cascode transistor input in the TC cell, as shown in Fig. (5), which is compatible with the adopted design in Fig. (3).

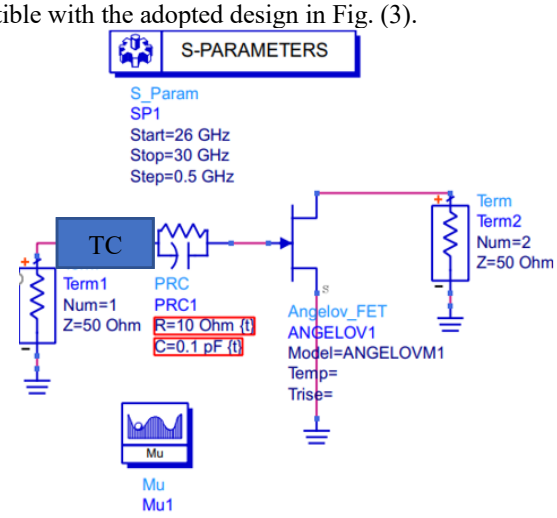

Fig. 5: Unconditional Stability Test Circuit for Cascode transistor to achieve Stacked-FET topology

The values of the parallel RC (PRC) connected at the transistor gate based on the Tune Parameter tool were tuned, as shown in Fig. (6).

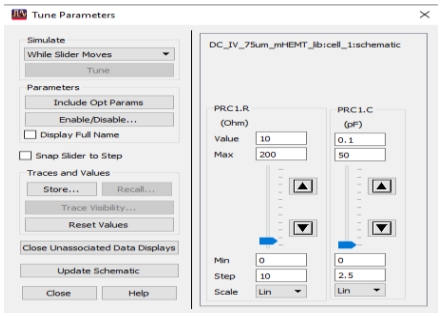

Fig. (6): Tuning the RC circuit based on the Tune Parameters tool.

Fig. (7) shows the results of the μ test at frequencies from (26-30GHz), where the division of axis Mu1 created by the Advanced Design System (ADS) program is (1.48713527124_1.48713527308) with a step equal to 〖8.715×10〗^(-12), which is the reason for physically showing the same number of 1.4871353 on the axis Mu1. Fig. (8) shows that the value of μ from Eq.1 is approximately 1.5, which means that it is larger than 1, which will achieve the unconditional stability of the transistor by the existence of parallel RC on the gate input of the cascade transistor based on the adopted configuration Stacked-FET topology.

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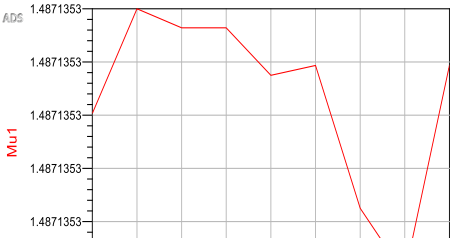

Fig. (7): the results of the unconditional stability test for the presence of the parallel RC with Cascode transistor from Stacked-FET topology.

C. DC Bias Transistor of Stacked-FET DPA amplifier

relating to DC bias, we assume in this study the following: gate bias voltage Vg, AB = -1.5 V and drain bias voltage Vd, AB = 24 V (for the main amplifier (class AB) in a Stacked-FET DPA), and gate bias voltage Vg, C = -2.6 V, and drain bias voltage is Vd, C = 24 V (for auxiliary amplifier (class C) in the Stacked-FET amplifier). As shown in Table 1.

Table I:DC Bias

Class of operation	**Main stage**	**auxiliary stage**
V_{DS}	24	24
V_{GS}	-1.5V	-2.6V

D. The final DPA amplifier circuit based on Stacked-FET topology

Figure (8) shows the final Doherty amplifier circuit based on the Stacked-FET topology, including the output power combining network, phase compensation network, Wilkinson power divider with a load of 50Ω, and a 28 GHz sine wave source, including input power in the range of -5 dBm to 23 dBm.

Figure 9 shows the final traditional Doherty circuit design with which we compared the performance of the Stacked-FET DPA.

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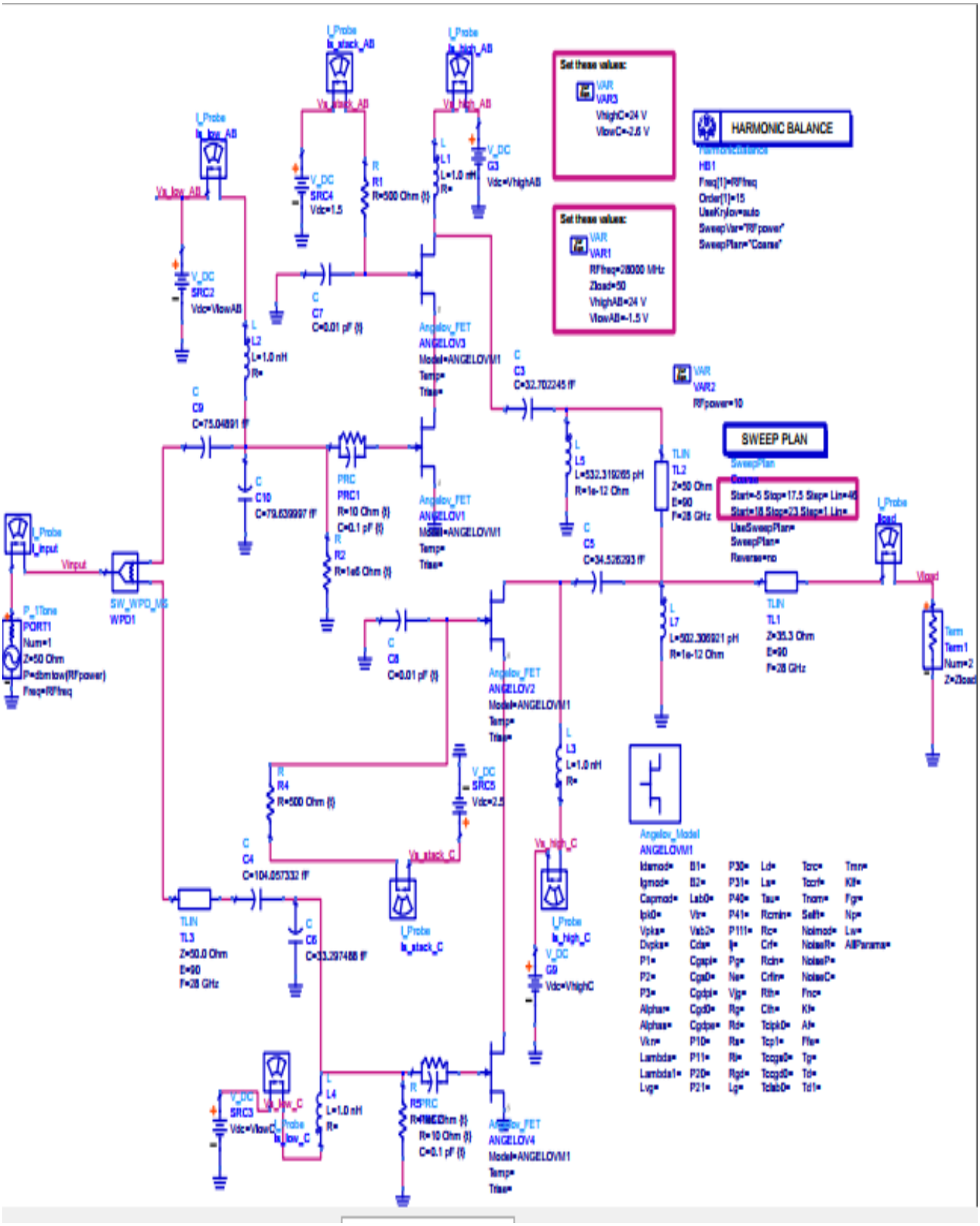

Fig. (8): the proposed circuit of the final Stacked-FET

Doherty amplifier.

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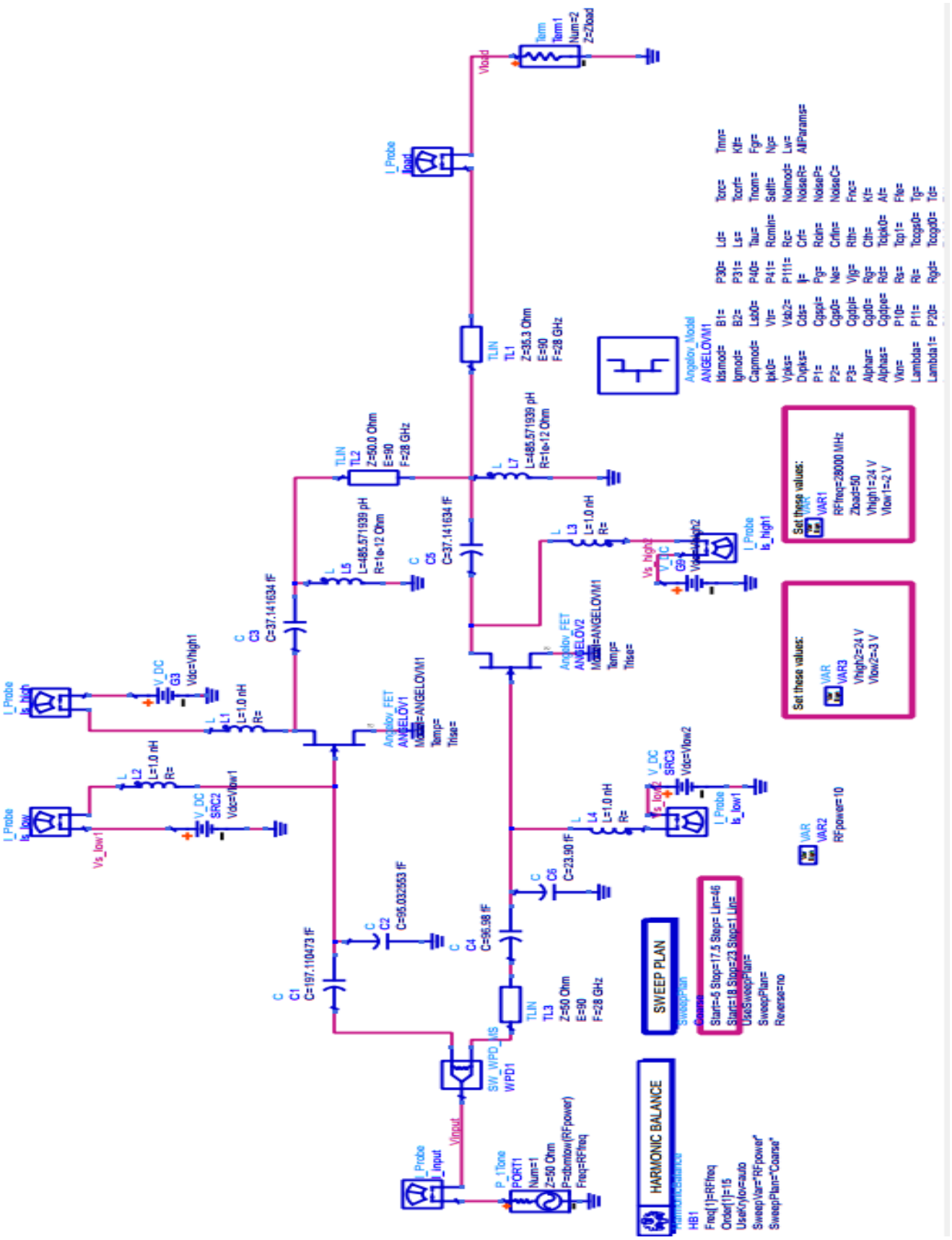

Fig. (9): the simulation of a traditional DPA amplifier circuit based on AB/C-Doherty standard.

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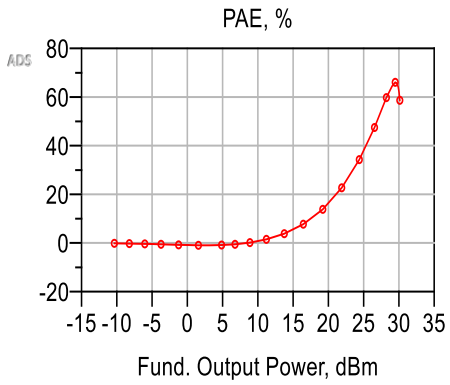
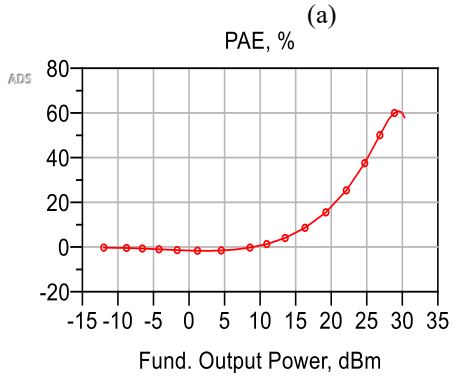
IV. RESULTS AND DISCUSSION

A.Efficiency and Power Output

Figures (10. a) and (10. b) present the comparison of the simulated PAE between a DPA amplifier based on Stacked-FET topology and a traditional one, it can be seen that Stacked-FET topology obtains 66% maximum PAE at an output power of 29 dBm, while we obtained 60% maximum PAE at output power of 29 dBm in traditional desigin, that is mean improvement of 6% is obtained in the Stacked-FET design. Similarly, at output power back-off (OPBO=6 dB) we got an improvement of 20% of PAE in the Stacked-FET design, which proves the role of the Stacked-FET topology in improving the power output compared with the traditional Doherty amplifier in Figure (13. b).



(a)

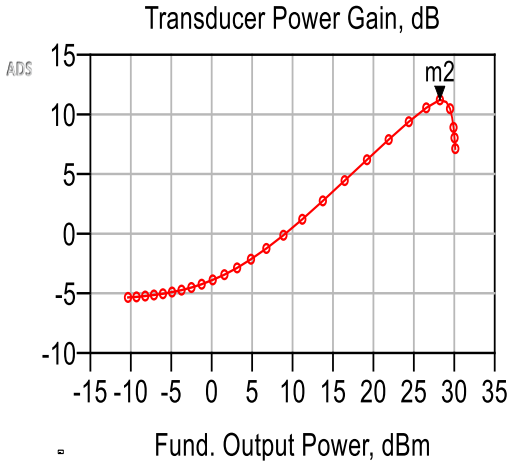


(b)

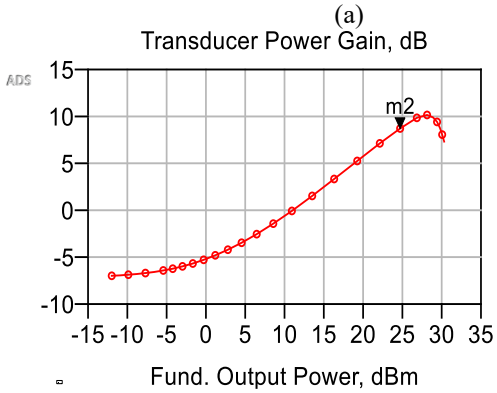
Fig. (10): (a) Efficiency bending PAE Stacked-FET DPA amplifier. (B) Efficiency bending PAE traditional DPA amplifier.

B.Gain

Figures (11. a) and (11. b) present a comparison of the simulated gain between the stacked-FET DPA amplifier and the traditional one. It can be observed that the Stacked-FET topology obtains a maximum gain of 11.6 dB, whereas it obtains a maximum gain of 10 dB in the traditional design, that is, a mean improvement of 2 dB is obtained in the Stacked-FET design. No improvement was observed in the back-off output power (OPBO=6 dB).



(a)

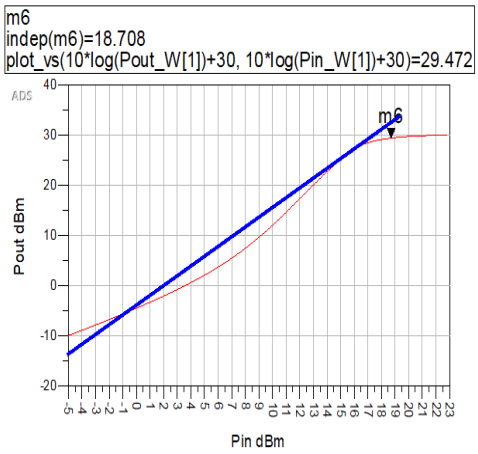


(b)

Fig. (11): (a) Gain of Stacked-FET amplifier. (b) Gain of traditional DPA amplifier.

C. Power Compression point at – 1dB

The linearity of the Stacked-FET DPA was slightly improved compared with that of the traditional DPA amplifier. Fig. 12(a) shows the curve of the output power change concerning the input power. When comparing this Fig. to Fig.12(b), we notice that the straightness of the curve for the Stacked-FET DPA before the power compression point at 1 dB is better than that of traditional Doherty. However, the power boost is clearly shown in Fig. 15(a), where the output power has moved to 29.5 dB at the 1 dB power compression point, which is approximately 1 dB better than that of a conventional DPA amplifier.



(a)

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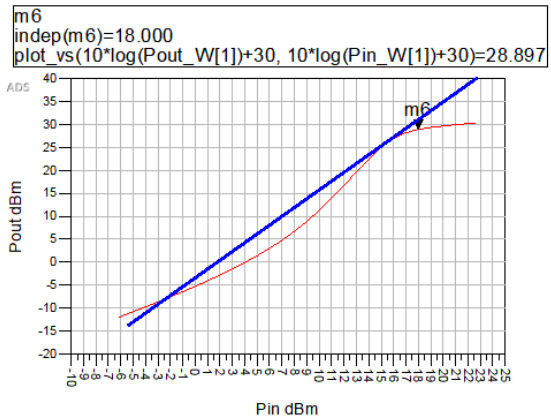
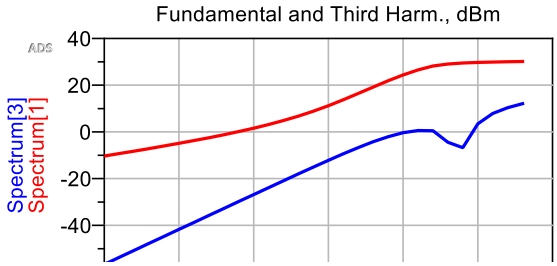


(b)

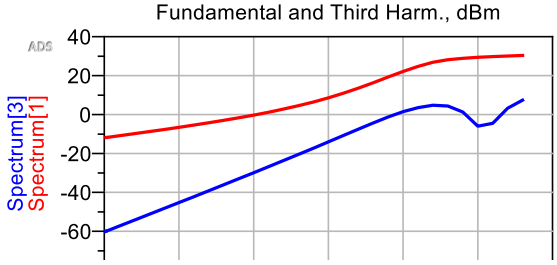
Fig. 12: (a) the output power variation depending on Stack-FET DPA amplifier input power. (b) the variation of output power depending on traditional DPA amplifier input power.

*D.*Harmonic Distortion

Fig. 13(a) shows the fundamental and third harmonic spectrum for the proposed stacked- FET topology (fundamental harmonic at 28GHz and third harmonic at 3*28GHz), it can be observed here improvement in linearity more clearly than Fig. 12(a)
There is a clear improvement in the power level difference between the third harmonic and fundamental harmonic corresponding to the operating frequency of the amplifier. Moreover, the power curve of the third-harmonic spectrum does not begin to exceed 0 dBm until the RF power exceeds 20 dBm, which is a clear improvement in linearity compared to Fig. 13(b) for a traditional Doherty amplifier.



(a)

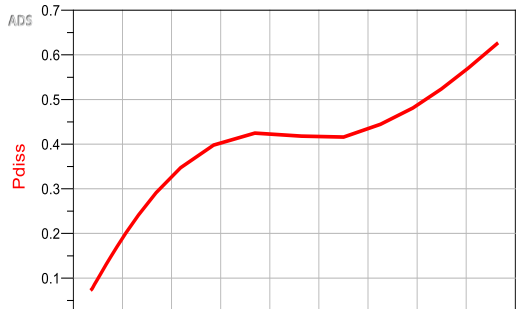


(b)

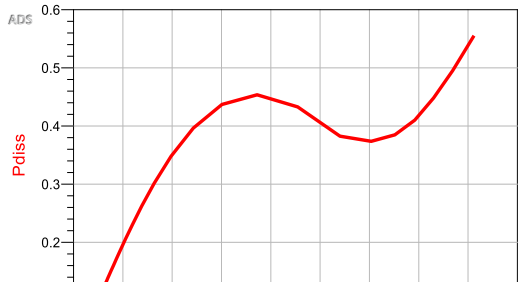
Fig. 13: Power spectrum of fundamental and third harmonics depending on RF power of (a) Stacked-FET DPA amplifier, (b) Traditional amplifier.

*E.*Power Dissipated

The Stacked-FET DPA amplifier offers lower power dissipation in the form of heat compared to a conventional Doherty amplifier, as shown in Fig. 14(a) when compared to Fig. 14(b), where the power dissipated at the maximum input power level is 0.55 W and is therefore Relatively much lower than its value in a traditional Doherty amplifier, exceeding 0.63 watts. This is advantageous for using the Stacked-FET topology in a Doherty power amplifier.



(a)



(b)

Fig.14: Dissipated power in the amplifier depending on total input power. (a) Stacked-FET DPA amplifier. (b) Traditional Doherty amplifier.

*F.*Summary of results of Doherty's amplifier performance based on Stacked-FET

Table (2) shows a comparison of the performance of each of the traditional Doherty amplifiers and the Doherty amplifier based on the Stacked-FET topology in terms of efficiency, output power, and immunity to distortions (degree of linearity).

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Table II: COMPACTION RESULT IN STACKED-FET DPA WITH TRADITIONAL DPA

	PAE (%)	**POUT (dBm)**	**Gain(dB)**	**Linearity**	**PDiss(watt)**
Stacked-FET DPA	66	>30	11.22	Good	0.55
Traditional DPA	60	~30	10	Bad	0.63

V. CONCLUSION

In this study, we reviewed the results of the study and simulation of the RF amplification solution using the Doherty architecture with ADS program, where the main amplifier is biased class AB, while the auxiliary amplifier is biased class C, and considering that the DPA amplifier studied here is of the symmetrical type, that is, using the same transistor device in both configurations for the main and auxiliary amplifier.

We found that a Doherty amplifier solution based on Stacked-FETs topologies significantly enhances both efficiency and output power. However, linearity must be improved because the performance in terms of linearity and gain remains similar to that of a traditional Doherty amplifier.

In any case, the solution of the Doherty amplifier according to the Stacked-FETs topology provides the requirements for efficiency and output power in the cells of the base stations of the 5G network, such as femto and microcells, where it is possible to reach a maximum PAE of 66% and an output power of 30 dBm and gain of up to 12 dB at an operating frequency of 28 GHz.

Table III: Comparison with related studies

reference	Center Freq (GHz)	Power (dbm)	Gain (dB)	Peak PAE (%)	Peak at 6dB PBO (%)	Chip size (mm^2)	Technology
11	28	26	12	40	29	2.86	0.15 µm GaAs
12	28	28.5	14.4	37	27	4.93	0.15 µm GaAs
13	33	26	5.5	39	19	3.4	0.15 µm GaAs
14	26.4	25.1	10.3	38	27	25	0.15 µm GaAs
This work	**28**	**30**	**11.6**	**66**	**35**	**----**	**0.75-µm GaAs**

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