Improvement of Design Issues in Sequential Logic Circuit with Different CMOS Design Techniques

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Abstract

This paper present the low power high performance D flip flop using with gate diffusion input (GDI) technique. Here we also implemented D flip flop using different CMOS logic design such as transmission gate, pass transistor logic (PTL) and gate diffusion input (GDI) logic and shown the comparable study on these CMOS design techniques. These different CMOS logic design techniques are also compared with respect to the layout area, number of transistors, delay, and power consumption. All the result of this paper is verified on 'cadence virtuoso tool' using specter at 45nm technology with supply voltage 0.7V.

Keywords

CMOS logic style; Pass transistor logic; transmission gate; Gate Diffusion input(GDI)

1. Introduction

Historically, speed was the performance metric parameter used by the VLSI designers. Integrated chips such as digital processors, microprocessors, DSPs (Digital Signal Processors), ASICs (Application Specific ICs), etc. thus used high gain in terms of performance and silicon area. A small area and high performance are the main important factors which affect gain highly [1], [2] With the continuously increasing chips' complexity and number of transistors in a chip, power consumption is growing as well. Higher power consumption, raises chips' temperature and directly affect battery life in portable devices as it causes more current to be withdrawn from the power supply. High temperature afflicts circuit operation and reliability so requires more complicated cooling and packaging techniques [3] [4]. The wide use of sequential logic and memory storage systems in modern electronics results in the implementation of low power and high speed design of basic memory elements. One of the most important basic memory elements is the D flip-flop (DFF) [5]. Hence novel architectures such as CMOS Transmission Gate (TG), Pass-Transistor Logic (PTL), Complementary Pass-transistor Logic (CPL) [6] and Gate Diffusion Input (GDI) [7] are proposed to meet the requirements. Each design style of the proposed CMOS logics has its fair advantages and disadvantages. Transmission gate is one of the most important structures in CMOS integrated circuits, supporting a logic reduction, switch function and efficient layout [8]. Gate Diffusion Input is a low power design that reduces transistor count. But the main problem with the GDI is that it requires twin well CMOS or silicon on insulator (SOI) process for fabrication [9]. Thus GDI chips are costlier comparatively. These logics along with their Hybrids are thus used to design D flip flop circuit [10].

2. CMOS Design Implementation of D Flip-Flops

Three different designs of D flip-flops in CMOS logic are presented in this section. Here the proposed D flip-flop is combines a pair of master and slave D latch.

2.1 Design D Flip Flop based on Pass Transistor Technique

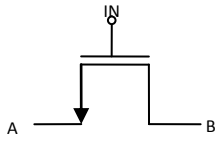

Figure.1 Basic NMOS Pass Transistor logic

It has been demonstrated that CMOS pass-transistor based logic can often result in high-speed and high-density circuits. It reduces the count of transistors used to create different logic gates, by eliminating extra transistors. Transistors are used as switches to pass logic levels between nodes of a circuit, rather than as switches connected on to provide voltages.

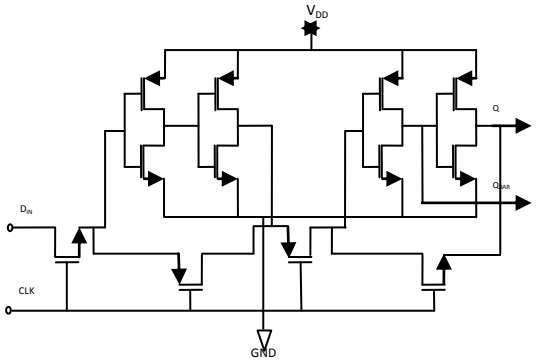

Figure.2 D flip-flop using Pass transistors

This reduces the amount of active devices, but has the disadvantage that the distinction of the voltage between high and low logic levels decreases at each stage [11]. Each of the switches can be implemented either by a single NMOS transistor Fig.1 shows the basic symbol of pass transistors. In Fig.2 uses pass transistors logic (PTL) and inverters for the master-slave latches [12]. The two chained inverters are in memory state when the PMOS loop transistor is on, that is when clk= 0. Other two chain inverters on the right hand side acts in the opposite way. The flip-flop changes its state during the falling edge of the clock.

2.2 Design D Flip Flop based on Transmission Gate Technique

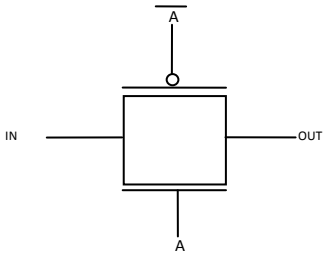

Figure.3 Basic symbol of Transmission gate

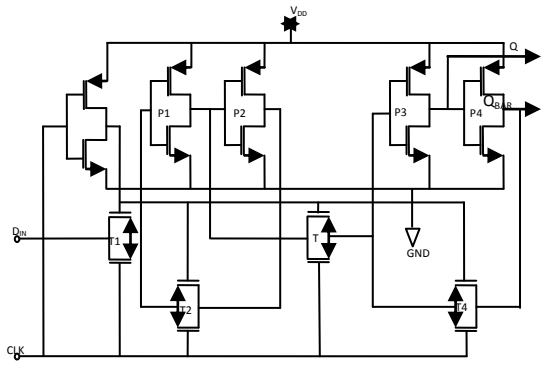

Figure.4 D flip-flop using transmission gates

A transmission gate is one of the most important structures in CMOS integrated circuits, supporting a switch function, logic reduction, and efficient layout. This solid-state switch is comprised of a PMOS transistor and NMOS transistor [13]. Each Transistor turn on or off alternately with alternate biasing of the control gates. The Fig.3 shows the basic symbol of transmission gate. Fig.4 shows the D flip flop using transmission gate and inverters [14]. At the negative edge of the clock, transmission gates T1 and T4 are ON and transmission gates T2 and T3 are OFF. During now the slave maintains a loop through two inverters P3, P4 and T4. This time previous triggered value from Din is keep within the slave. At the same time master latches next state however as T3 is OFF it's not passed to slave. During the positive clock edge T2 and T3 are turned ON and the new latched value passes to slave through the loop of two inverters P1, P2 and T2.

2.3 Design D Flip Flop based on GDI Technique

The GDI cell shown in Fig.5 was proposed by Morgenshtein et. al. [15]. It's a genius design which is very flexible for digital circuits. This technique optimizes the power dissipation and also reduces transistor count. The advantage of GDI technique two-transistor implementation of advanced logic functions and in-cell swing restoration under certain operational conditions, are unique within existing low-power design techniques. Fig.6 represents the master-slave connection of two GDI D-latches. During this the body gates are responsible for the state of the circuit. These gates are verified by the clock (clk) signal and make two different paths. One for transparent state of the latch ,when the clock is low and the signals are propagating through PMOS transistors .The other one is for the holding state of the latch ,when the clock signal is high and internal values are maintained due to conduction of the NMOS transistors[16]. The inverters are responsible for maintaining the complementary values of the internal signals and the circuit outputs.

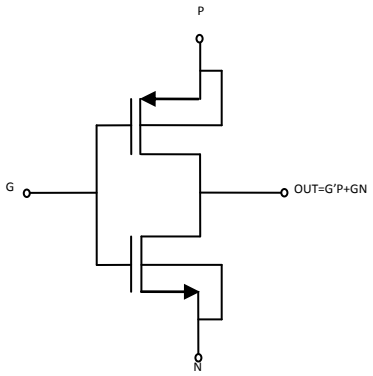

Figure.5 Basic GDI cell

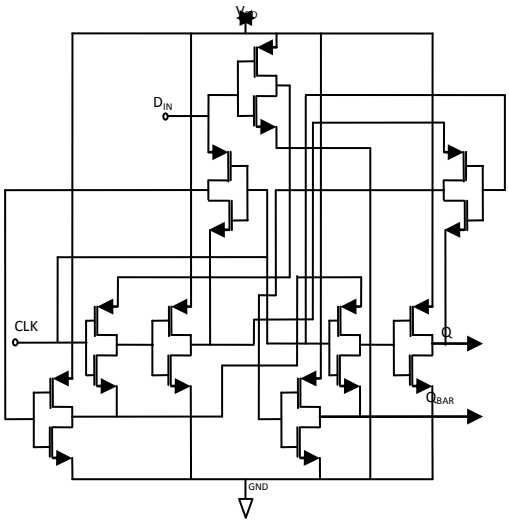

Figure.6 D flip-flop using GDI gates

3. SIMULATION AND RESULTS

In this section, the performance of the three different designs of D flip-flops have been implemented and simulated on cadence virtuoso tool on 45nm CMOS Technology. The table shows the result of three different design style of CMOS technology and also shows the comparison between them. These comparisons are based on Delay, number of transistor count, average power and leakage power of the different design style. Table 1 show the simulation result of the PTL, Transmission Gate, and GDI CMOS design.

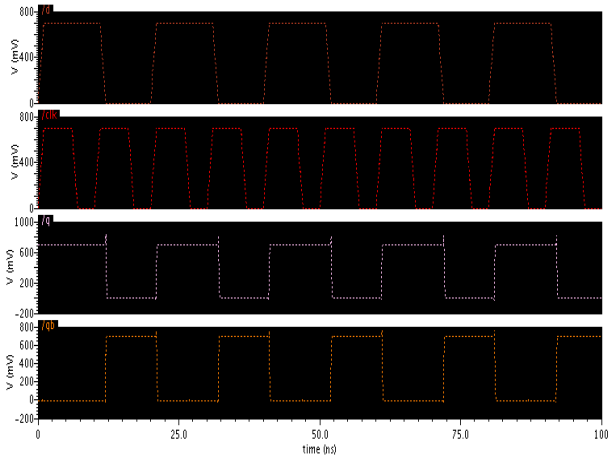

Figure.7 Input Output waveform of D Flip Flop

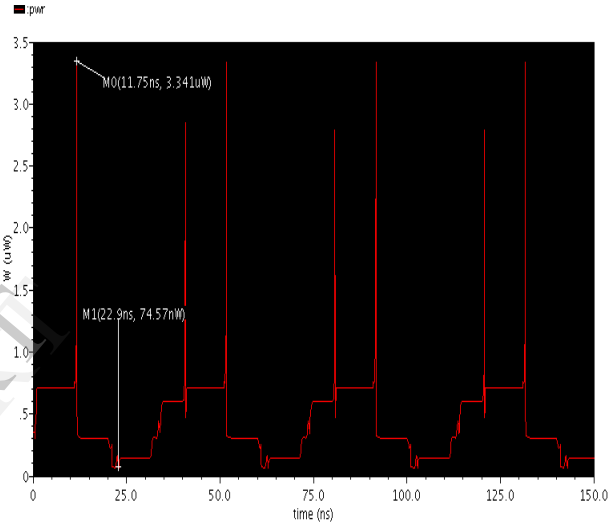

Figure.8 Active Power of PTL Based D Flip-Flop

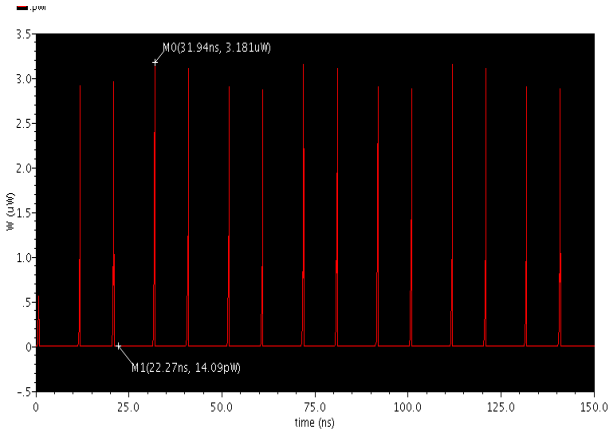

Figure.9 Active Power of Transmission Gate Based D Flip-Flop

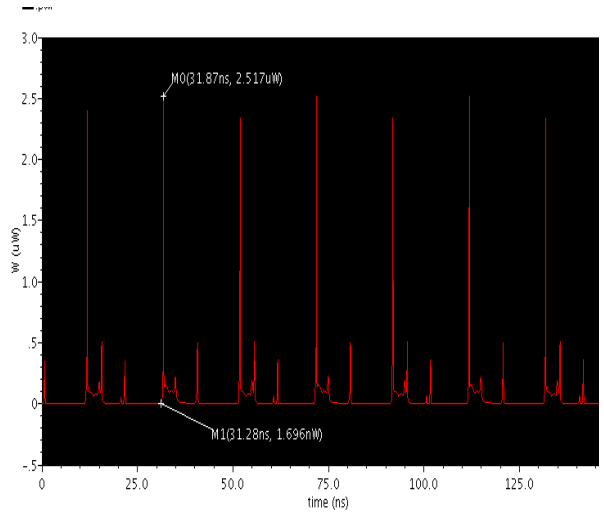

Figure.10 Active Power of GDI Based D Flip-Flop.

Table 1 Comparison result of proposed CMOS techniques

DFF Design using	Comparison result of proposed CMOS techniques			
	No. Of Transistor count	Delay	Avg. Power	Leakage Power
PASS Transistors logic	12	21.93ns	426.0nw	297.1nw
Transmission Gate	18	20.51ps	41.55nw	13.87pw
Gate Diffusion Input (GDI)	18	14.68ns	37.56nw	10.1pw

4. Conclusion

In this paper three CMOS implementations of DFFs using pass transistors, transmission gates and GDI gates are proposed. This paper also describes the comparative analysis on pass transistor logic, transmission gate and gate diffusion technique. As observed from the discussion about the D Flip Flop that various designs have their own advantage and disadvantage in terms of area, delay and power consumption. Here the pass transistor logic based DFF required minimum transistor (12) as compared to other CMOS structure .the design of DFF with transmission gate give the minimum delay (20.51ps) with respect to PTL and GDI based technique. The minimum average power is used in GDI based DFF approximate 37.56nw which is used to design low power circuits. All the parameters studied and verified on 'cadence virtuoso tool' using specter simulator at 45nm CMOS technology with 0 .7v.

5. Acknowledgment

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6. References

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