

Integrated EPON-LTE Network DBA Algorithm's Real Time Performance Analysis Using Network Processors

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Abstract

A new scheme in converged Ethernet Passive Optical Networks (EPON) and Long Term Evolution (LTE) networks is proposed for bandwidth allocation to the end user services. A mapping mechanism between the LTE bearers and EPON queues is established as a means to enhance the algorithm to support Quality of Service (QoS). OPNET simulation results reveal that the devised scheme excels in throughput and other QoS services, such as jitter, delay than the traditional one. However, commercial deployment of the algorithm requires evaluation of the performance of the algorithm in a LTE switch to verify its hardware compatibility. This paper focuses on implementing and testing the performance of the CDA (Centralized DBA) algorithm in a LTE switch using the Intel's IXP 2400 Network Processor. The performance of the algorithm is further compared with the conventional process in terms of machine clock cycles.

1. Introduction

With the emergence of bandwidth-intensive applications, broadband access is becoming increasingly important for the Internet and these are best offered by fixed fiber links with high data rates. Among the different network access solutions available, EPON is a cheap solution (95% of already existing local networks use Ethernet based communication, overlapping of Ethernet equipment with fiber infrastructure and void of maintenance cost)

and offers extremely high bandwidth in addition to possessing reliability and network availability [1]. However, they are still very costly for deployment to each home, and provide little flexibility and no mobility. Broadband wireless access networks like GSM, WiFi, WiMAX and LTE provide high-capacity bandwidth links, coverage and QoS support [2]. However, wireless networks generally suffer from a limited wireless spectrum, and when many users are to share the bandwidth it limits the bandwidth assigned to each user. This necessitates the development of an efficient "last-mile" access network that provides high bandwidth with QoS support, mobility and cost-effective access [3].

Integrating both wireless and optical access network technologies is essential in the evolution of a new generation wired-wireless access to combine mobility with high speeds, which would see the integration of the latest advances in optics and electronics. One major challenge associated with the integration process is the proper selection of a DBA algorithm since DBA is solely responsible for effective allocation of resources in the system. Also, QoS guaranteeing is a critical issue in such a converged network. The wireless technology focused in this work is LTE and EPON is chosen for the optical part of the network. Researchers worldwide have proposed lot of complex and diverse DBA algorithms and Interleaved Polling with Adaptive Cycle Time (IPACT) [4] is considered to be one of the most efficient. Most of the proposed DBA algorithms are centralized [5] - [7]. SLA between the OLT and ONUs

determine fairness, which means terms of SLA should be satisfied in allocating bandwidth to a ONU in a cycle ensuring any ONU is not affected by any other overloading ONU. Earlier works by researchers mostly enforced fairness based on the ONU's current request. Hence an attempt is made in this research work to fine tune the DBA process in a different perspective and also enforce QoS in the EPON-LTE convergence. Though EPON and LTE represent fixed PON and 4G mobile access technologies in our work, the proposed algorithm is also applicable to other PON and 4G access networks such as GPON and WiMAX.

To realize the algorithm in commercial switches, it has to be implemented in processor and checked for its compatibility in hardware architecture. For the same, the number of clock cycles consumed for the execution of the algorithm is calculated to determine the speed of the algorithm. Real time service assurance of LTE necessitates that the algorithm be tested in a processor before implementing it for commercial practice. To realize the same, this paper focuses on implementing and testing the performance of the CDA algorithm in a LTE switch using the Intel's IXP 2400 Network Processor.

With the supporting factors of high performance, flexibility and fast time to market, Network Processor is the best option for implementing the network equipments and it also provides the correct balance of hardware and software [8] – [11]. Network processor is similar to a CPU in that it is an integrated circuit optimized for the networking application domain and is basically a software programmable device. Agere, AMD, Cavium, EZchip, Hifn, Intel, Mindspeed, Motorola, Xelerated, Ubicom [12] – [16] are some of the key players in the market. Among the different network processors available in the market, Intel IXP2400 network processor's flexibility and performance makes it highly desirable solution for services like Gateways, QoS enforcement, Service Level Agreements (SLAs) realization [12]. Most of the packet processing is handled by the Microengines (MEs) and IXP2400 has 8 MEs connected in two clusters of 4 MEs. All the MEs run synchronously each being its own processor.

The following sections in the paper include a detailed explanation about the implementation of the algorithm in network processors and the results of the process along with a summary.

2. Architecture of the scheme

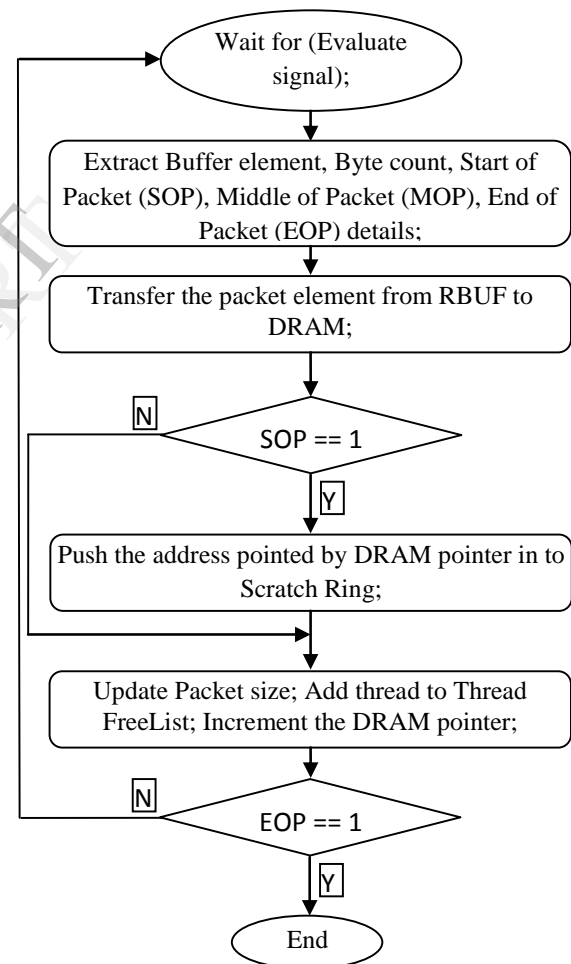
This section explains the CDA algorithm along with its implementation in the processor. There is no functional difference in the operation of the ONUs between the conventional scheme and the CDA

algorithm. Still, to record the performance of the system the ONU processing system is implemented in the network processor and the machine cycles required to execute the algorithm are estimated. Three MEs are required to construct a ONU hardware. The first ME receives the packets, the second ME performs the bandwidth estimation and the third ME is used to transmit the packets. Description of the OLT's functionality follows the ONU's construction.

2.1. ME 0:0 – Reception

ME 0:0 is used to receive the packets for the ONU. The first ME receives all the incoming packets which are then stored in memory for further processing.

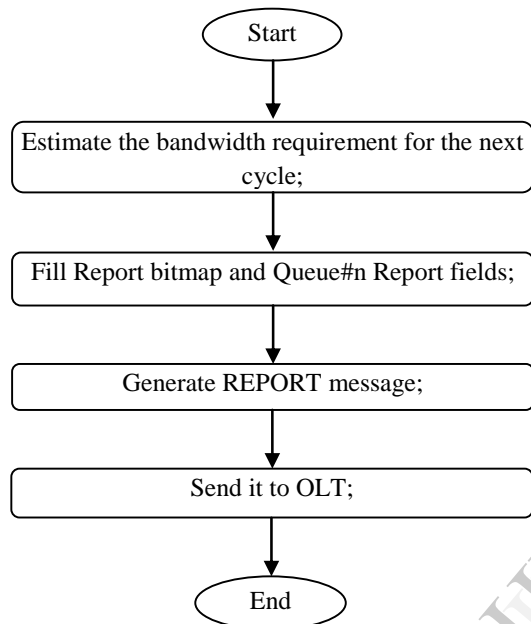
Flowchart for Packet Reception Functionality:



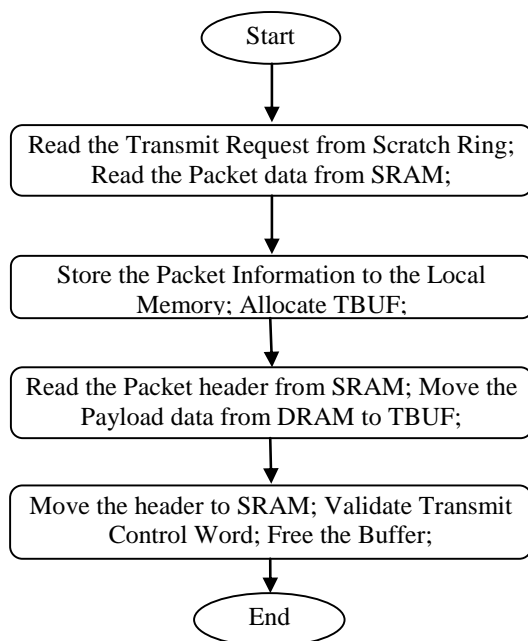
2.2. ME 0:1 – ONU Processing

ME 0:1 reflects the functionality of the ONU. The ONU estimates the bandwidth requirement for the next cycle and generates the REPORT message filling the Report bitmap and Queue#n Report fields of the REPORT message. Then, the ONU sends the request message to the OLT.

Flowchart for ONU processing:



2.3. ME 0:2 – Transmission



ME 0:2 is used by ONU for packet transmission.

Implementation of the conventional and proposed OLT models using network processor is now discussed. The implementation requires four MEs. ME 0:0 receives the packets from the ONU. ME 0:1 classifies the packet. ME 0:2 run the conventional and proposed OLT algorithms and forward the packets to the ME 0:3 for transmission. The receiving process carried out by ME 0:0 is similar to the ONU model as explained in the previous section and the transmission process carried out ME 0:3 is similar to the process handled by ME 0:2 in the ONU model.

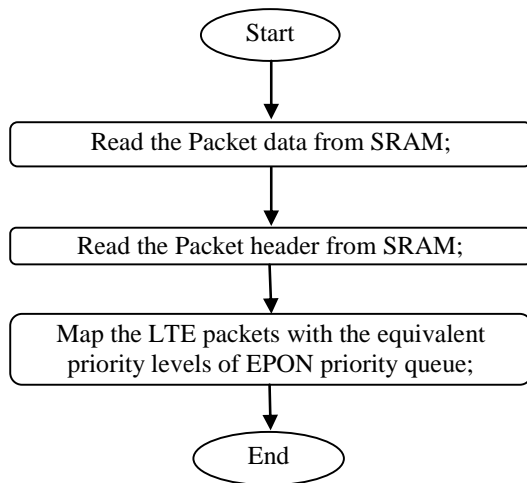
2.4. ME 0:1 – Classification

In order to improve the CDA algorithm, the QoS mapping between EPON 802.1p priority queues and the LTE connections is done. The second ME 0:1 reflect the functionality of the QoS guarantor. EPON supports eight priority levels with the QoS for the service represented by the numbered priority queue in the 802.1P nomenclature. QoS in LTE is determined by QoS Class Identifier (QCI), Allocation and Retention Policy. The 9 QCI values define eight characteristics for IP packets ranging from VOIP call to email and chat. The mapping between the EPON priority queue and LTE flows provides equivalent QoS levels at both ends as detailed in Table 1.

TABLE I
EPON - LTE QoS mapping mechanism

Priority	LTE services	EPON traffic types
0	IMS Signaling	Background
1	VOIP Call	Best Effort
2	Video Call	Excellent Effort
3	Online Gaming	Critical applications
4	Video Streaming	Video
5	Video (buffered streaming)	Voice
6	Voice, video, interactive gaming	Internetwork Control
7	TCP-based (e.g. WWW, e-mail), FTP, P2P, etc.,	Network Control

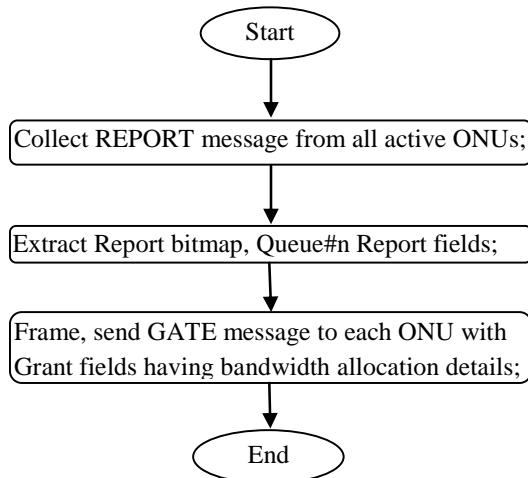
Flowchart for QoS mapping:



2.5. ME 0:2 – OLT processing

Conventional OLT: ME 0:2 depict the functionality of the conventional OLT. OLT receives the REPORT message from all active ONUs. For each REPORT message extracts the Report bitmap and Queue#n Report fields from each REPORT message and calculates the ONU's requested bandwidth. OLT calculates the available and allotted bandwidth to each ONU and then sends a GATE message to each ONU with these details.

Flowchart for Conventional OLT processing:



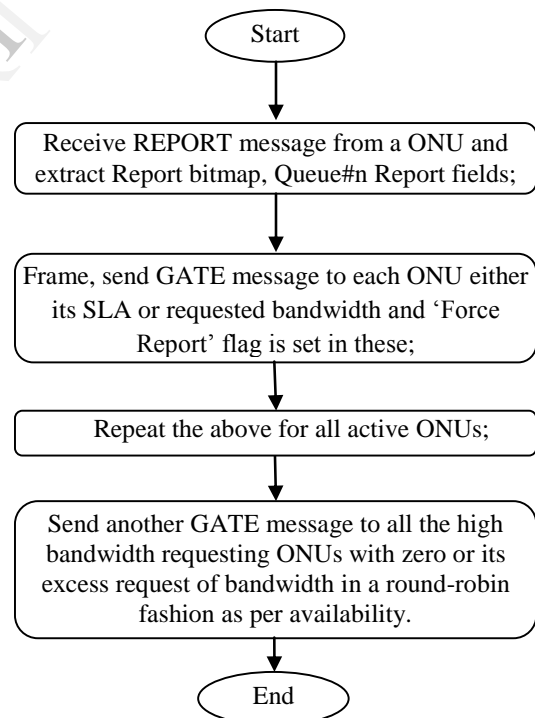
After evaluating the performance of the conventional algorithm, the CDA algorithm is then implemented.

Proposed OLT Processing: ME 0:2 reflect the functionality of the proposed OLT. The OLT is

designed to be configured with the SLA values of the ONUs. OLT on receiving a request from the ONU, grants immediately either its SLA or requested bandwidth based on whether the request is higher or lower than the SLA value without waiting for request messages from rest of the active ONUs. For ONUs with request higher than its SLA agreement, the first set of GATE message do not generate a REPORT message in response by resetting the 'Force Report' flag in the GATE message. Whereas, for ONUs with request lower than or equal to its SLA agreement, a single GATE message is sent and the allocation meets its request. This GATE message generates a REPORT message in response to continue with the transmission process for the next cycle.

If more bandwidth is available, the OLT then sends another GATE message to all the high bandwidth requesting ONUs with its excess request of bandwidth in a round-robin fashion. The second GATE message unlike the first informs the ONU to respond back with a REPORT message to continue with the transmission process for the next cycle.

Flowchart for proposed OLT processing:



After implementing the algorithm, the performance of the same in the ME is evaluated.

3. Results and Discussions

The conventional and proposed architecture are implemented in IXP2400 network processor which is configured to work as a LTE switch and studied for their performance.

Since there is no difference in configuration for the ONU system between the conventional and proposed CDA schemes, the performance study of the MEs in the ONU configuration is studied for better understanding of the system. Reception implementation is done in ME 0:0 for both ONU and OLT configuration. Initially, ME 0:0 is free but the execution of the ME increases as the packets are received and transferred to the next ME for further operation as detailed in figure 1. When there are no more packets to receive, this ME becomes completely free. ME 0:1 implements the functionality of the ONU. Speed of execution is initially low but gets increased as packets are received and the REPORT messages are generated containing the bandwidth request details for each request. When there are no more packets to receive, the consumption becomes gradually lower. ME 0:2 transmit the packets from the ONU to the OLT. Initially, the speed of execution for ME 0:2 is very low because packets reach ME0:2 only after they are received and processed by ME 0:0 and ME 0:1. The speed of execution increases after this initial slowness when more packets reach ME0:2 scheduled for transmission after ME 0:1 finishes processing of the packet.

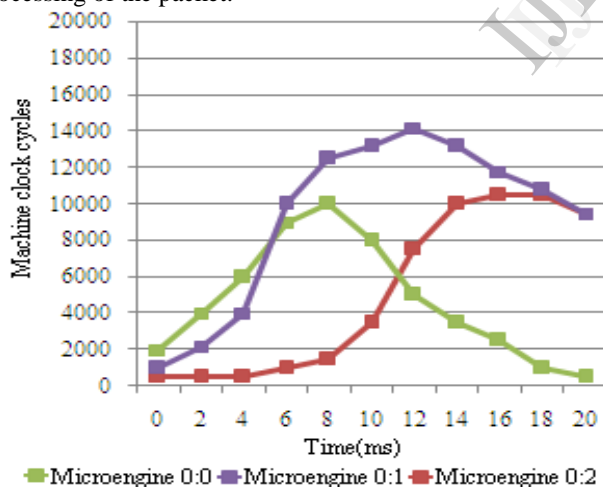


Figure 1: Machine clock cycles for ONU algorithm

Performance of the OLT configuration is the critical factor in deciding the realization of the algorithm. Performance study of the MEs in the OLT configuration is depicted in figure 2. Since ME 0:0 is similar in both ONU and OLT model and ME 0:3 in OLT is similar to the process handled by ME 0:2 in the ONU model, we'll concentrate on the functionalities of

ME 0:1 and ME 0:2. Packet classification functionality is implemented in ME 0:1 which classifies the packets based on the Type of Service. ME 0:1 is initially free but when the packets are transferred from the ME 0:0 for classification it increases gradually. Conventional and proposed OLT functionality are implemented in

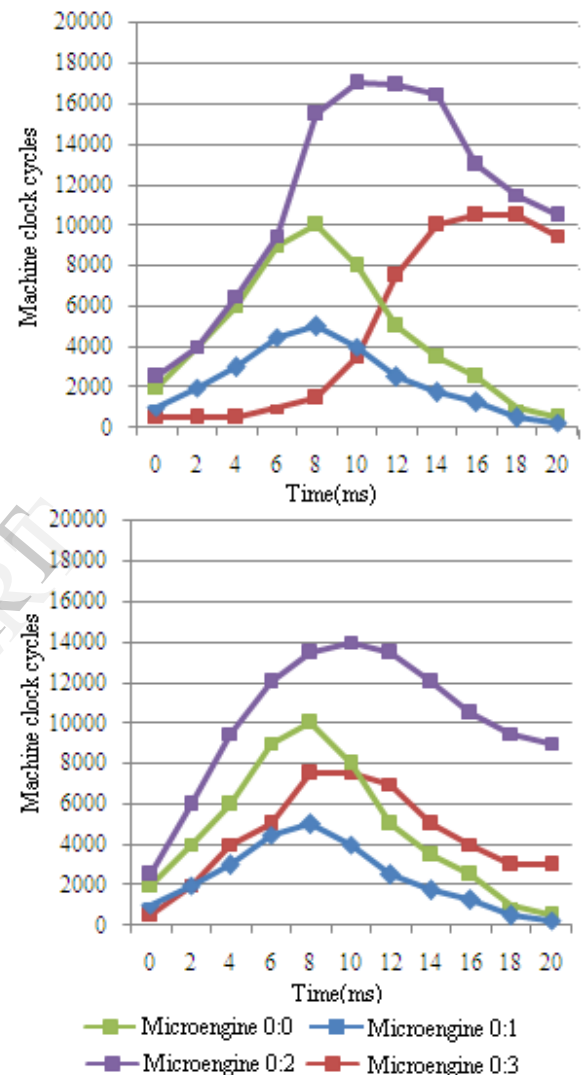


Figure 2: Machine clock cycles for Conventional (top) and Proposed (bottom) OLT algorithm

ME 0:2. Machine clock cycle consumption by ME 0:1 in the conventional mode gradually increases when the packets are processed after reception and when packets from all ONUs are received it becomes high, since the bandwidth allocation calculation is done only after receiving from all the ONUs. In the proposed mode, the utilization of the machine clock cycle is higher than the conventional mode in the start since the OLT now sends a GATE message to every request immediately.

But the utilization remains stable and lower than the conventional mode after receiving request from all ONUs since the OLT now does the second round of bandwidth allocation which involves lesser processing than conventional mode. The observation from the clock cycles indicates that the processor requires around 17000 cycles to execute the conventional OLT algorithm at the peak and 14000 cycles to execute the proposed OLT algorithm at the peak. The peak utilization of the machine cycles in the CDA algorithm is lower than the conventional mode and hence becomes a proof for the suitability of the algorithm for commercial deployment in a LTE switch.

4. Conclusion

Most of the bandwidth allocation proposals excel in a synthetic network setup, but when it comes to real time setup they fail to perform since the synthetic setup do not consider all the practical factors in a network. Any bandwidth allocation algorithm for the network should be compatible in a hardware switch without which it is not feasible to deploy the algorithm commercially and hence evaluating the performance of the algorithm in a hardware switch becomes highly important. In this work, we have demonstrated the suitability of the CDA algorithm to deploy commercially by evaluating the performance of the algorithm in a switch. It would be worthwhile to see how the algorithm performs in real time setup.

References

- [1] Kramer, and Glen, *Ethernet Passive Optical Networks*, McGraw-Hill Communications Engineering, 2005.
- [2] <http://www.3gpp.org/>.
- [3] IEEE 802.3ah, *Ethernet in the First Mile Task Force*, <http://www.ieee802.org/3/efm/index.html>.
- [4] G. Kramer, B. Mukherjee, and G. Pesavento, "Interleaved polling with adaptive cycle time (IPACT): a dynamic bandwidth distribution scheme in an optical access network", *Photonic Network Communication*, Jan. 2002, Vol. 4, pp. 89–107.
- [5] J. Zheng, and H. T. Mouftah, "A survey of dynamic bandwidth allocation algorithms for Ethernet Passive Optical Networks", *Optical Switching Networking*, July 2009, Vol. 6, pp. 151-162.
- [6] G. Kramer, *On Configuring Logical Links in EPON*, whitepaper : <http://www.ieee-communities.org/epon/>.
- [7] S. Choi, and J. Park, "SLA-aware dynamic bandwidth allocation for QoS in EPONs", *IEEE/OSA Journal of Optical Communications and Networking*, 2010, Vol. 2, n. 9, pp.773 - 781.
- [8] Douglas E. Comer, *Network System Design and Network Processors*, Pearson Edition.
- [9] T. Wolf, and M.A. Franklin, "Performance models for network processor design", *IEEE Transactions on Parallel and Distributed Systems*, June 2006, vol.17, no.6, pp.548-561.

- [10] Min Li, Biao Ma, and Wei-wei Zhang, "Research and Implement of the Key Technology for IP QoS Based on Network Processor", *Proceedings of the International Symposium on Computer Network and Multimedia Technology*, CNMT 2009, China, Jan 18-20, pp.1-4.
- [11] XuXiaobo, ZhengKangfeng, Yang Yixian, and XuGuoai, "A model for real-time simulation of large-scale networks based on network processor", *Proceedings of 2nd IEEE International Conference on Broadband Network & Multimedia Technology*, IC-BNMT '09, China, 18-20 Oct,pp.237-241.
- [12] "Intel® IXP2400 Network Processor: Flexible, High-Performance Solution for Access and Edge Applications", white paper, Intel.
- [13] J. Allen et al., "IBM PowerNP Network Processor: Hardware, Software, and Applications," *IBM J. Research and Development*, vol. 47, nos. 2/3, pp. 177-194.
- [14] AMCC, *NP7510 10 Gbps Network Processor*, 2003, <http://www.amcc.com>.
- [15] EZchip Technologies Ltd., *NP-1 10-Gigabit 7-Layer Network Processor*, http://www.ezchip.com/html/pr_np-1.html.
- [16] Intel Corp., *Intel Network Processor*, <http://developer.intel.com/design/network/products/npfamily..>