Interface Trap Analysis of HIGH-K MOSCAP Using T-CAD

Barnana Dutta
Assistant Professor (EXTC)
Atharva College Of Engg.
Mumbai,India

Shilpa Jaiswal
Assistant Professor (EXTC)
Atharva College Of Engg
Mumbai,India

Sweta Jha
Assistant Professor (EXTC)
Atharva College Of Engg
Mumbai,India

Divya Sharma
Assistant Professor(EXTC)
Atharva College Of Engg
Mumbai,India

Manoj Mishra
Assistant Professor (EXTC)
Atharva College Of Engg
Mumbai,India

Abstract- Considerable challenges are encountered with polysilicon gate as the channel length and gate-oxide thickness is aggressively reduced in case of CMOS devices when scaled into submicron regime. Metal gates and alternative gate dielectrics with high permittivity shows promising results to overcome the limitations like high gate resistance, high gate tunneling leakage current and boron penetration into the channel region. Therefore, there is immense interest in electrical characterization of a metal-oxide-semiconductor (MOS) capacitor structure with high-K dielectrics. Here capacitance-Voltage (C-V) characteristics of metal-oxide-semiconductor (MOS) capacitor is plotted for high-k dielectric materials such as, Aluminum Oxide (Al2O3), Hafnium Oxide (HfO2), Titanium Oxide (TiO2), Yttrium Oxide (Y2O3) as oxide material, Si as substrate and compared it with conventional SiO2 based MOS device. The MOSCAP structure was simulated to obtain the C-V characteristics using TCAD. From the results various parameters such as threshold voltage, flat band voltage, interface trap density etc. were calculated. The simulation results were then verified with the reported experimental values.

Key words: Al2O3, HfO2, TiO2, Y2O3

I. INTRODUCTION

Considerable challenges are encountered when bulk CMOS devices are scaled into the sub-45nm regime for higher integrated circuit (IC) density and performance. The problems of polysilicon gate depletion, high gate resistance, high gate tunneling leakage current, and boron penetration into the channel region become more severe as the channel length and gate-oxide thickness are aggressively reduced. Therefore, there is immense interest in metal gates and alternative gate dielectrics with high permittivity K [1]. To date, Hf- and Zr- based high-κ gate dielectric materials are the most common studied by academia and industry. Other alternative high-k dielectrics available for submicron MOSFET are Al_2O_3, TiO_2, Y_2O_3 and HfO_2. In this paper these above dielectrcs are used as insulator in MOS instead of SiO_2 due to their wide bandgap,

high decomposition temperature, and low electrical, but high thermal conductivity[3]. This will in fact enhance the lifetime, stability, reliability and signal to noise ratio of such devices. The high-κ/metal gate combination is also important for enabling future high-performance and low gate leakage emerging nano electronic transistors built upon non-silicon high-mobility materials, e.g. Ge, carbon nano tubes, and III-V substrates. The aim of this paper is to study the capacitance- voltage characteristics of Al/high delectric/Silicon structure, measure the interface trap charges and the very cause of leakage current are brought into focus.

## II. MODEL DETAIL

A. Properties Of high K dielectrics

With the scaling of the MOS-device ultra-thin SiO_2 suffers some unsolvable issues. Therefore, it is necessary to replace the SiO_2 with a thicker layer of higher dielectric constant. For high-k dielectric the K value should be greater than 10 where as 25-30 is preferable. However there is a trade off between high K value and band offset. The energy band gap and band offsets of some dielectric are summarized in table I.

TABLE- I: Electrical Properties of High K dielectrics

Gate Dielectric Material	Dielectric Constant (k)	Energy Band Gap Eg (eV)	Conduction Band Offset ΔEC (eV)	Valence Band Offset ΔEC (eV)
SiO2	3.9	9	3.5	4.4
Al2O3	8	8.8	3.7	4.7
Y2O3	13	6	2.3	2.6
HfO2	25	6	1.5	3.4
TiO2	80	3.5	1.1	1.3

Special Issue - 2017

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
ICIATE - 2017 Conference Proceedings

B. Preparation

In the present work, simulation was carried out on Al/Gate Oxide/Silicon MIS structure using atlas version 5.10.0.R TCAD of SILVACO. The structure of MOS capacitor is with an area of $3.976 \times 10^{-4}\ \mu m^2$. Here the insulator part is selected to be of thickness $0.225\mu m$. The semiconductor is 280um thick p-type silicon, uniformly doped with $5 \times 10^{14}\ cm^{-3}$ acceptors. In our structure the bulk dimension is very large. Here Aluminum is used for forming gate and substrate contact of area $3.1459 \times 10^{-8}\ \mu m$ as shown in fig.1 below. While simulation material properties of gate oxide at room temperature like band gap, permittivity, etc. has been declared from [15] so as to include it into the material library. Appropriate models were declared such as cvt and srh to take care the physics [15]. The CV curve was obtained and analyzed by applying a small AC voltage with different frequencies from 10Hz – 1MHz in steps.
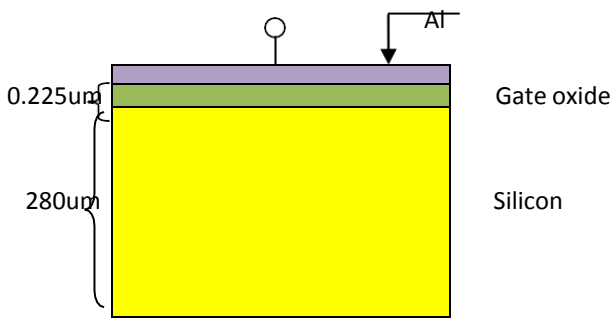
(Fig .1. MIS structure of Al/Oxide/Si)

(▮ Conductor, ▮ Insulator, ▮ substrate)

III. RESULT AND DISCUSSION

A. High Frequency CV Plots:

The bulk of the MOS capacitor structure is consisting of both majority charge carrier and minority charge carrier. With external applied voltage the majority carriers can respond immediately but for minority carriers the response time is more. If the applied potential changes so quickly that the polarity across the MOS gate changes before the minority carriers could respond to the applied field, the applied field is said to have a high frequency [7]. Here with negative gate bias, p-type „Si‟ is in accumulation and we measure simply the capacitance of the parallel plate capacitor with various dielectric layers as dielectric. As gate voltage is more positive then the flat band voltage (Vfb), a depletion layer is formed in the semiconductor. This creates a capacitor in series with the oxide capacitor and produces a drop in total capacitance. When the gate voltage exceeds the threshold voltage a layer of

inversion charge is formed, and if the gate voltage is slowly increased further, the inversion layer increases till charge to balance of the gate but for the measurement of positive charge the depletion layer doesn‟t widen further. Since the depletion region width is reached maximum, the total capacitance pegged to minimum. The structure is simulated at relatively high signal frequency i.e. 1MHz.Fig.3 (a). As shown in Fig. the HF-CV characteristics of MOS capacitors with tox= 0.225um were measured for a small signal frequency, f = 1MHz, and at a slow DC sweep rate, 1 V/s.

As there is no charge is generated in ideal condition, the capacitance value is decrease in a rapid rate compare to the SiO_2. Hence the high frequency capacitance value is less in this case.
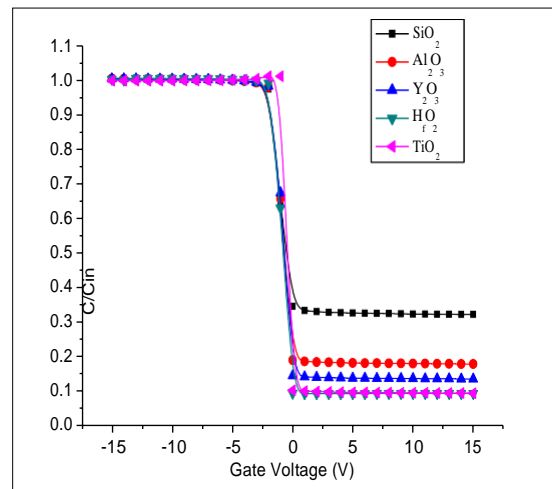

Fig .3(a) High frequency curve of Al/Oxide/Si simulated with various high k dielectrics in SILVACO.

B. Interface Tarp Density (Dit)

The interface states are located at or very close to the semiconductor/oxide interface with energy distributed along the band gap of the semiconductor. Electrons or holes get trapped in these states and act like charges at the interface. It is due to the incompletely oxidized „Si‟ atom with unsatisfied dangling bond located in the oxide. The charge associated with Dit may be positive, neutral or negative or in fact may change during normal device operation because of capture of electron or holes. Interface trap charges also known as interface trap or interface state Fig.3(b) [8].When a voltage is applied the interface trap levels move up or down with the valance and conductance band, while Fermi level remain fixed. An interface trap is considered as a donor if it can become neutral or positive by donating an electron. An acceptor interface trap can become neutral or negative by accepting an electron [9].

Special Issue - 2017

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
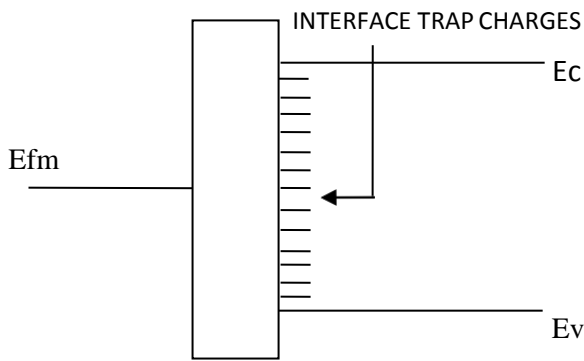**ICIATE - 2017 Conference Proceedings**

Fig.3(b). Energy-band diagram of a MOS structure, depicting the distribution of interface states along the band gap of the semiconductor at the semiconductor /oxide interface.
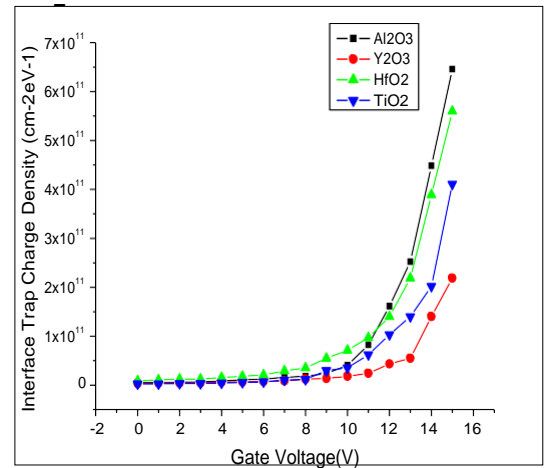
In order to evaluate the interface trap density Dit, we can use either capacitance measurement or the conductance measurement. Here the Dit is determined in the room temperature 1 MHz C-V curves with the standard high frequency capacitance method. Using the relation between depletion region capacitance, insulating capacitance and the slope of a surface potential (Φs) and C curve $\frac{d\Phi s}{dV}$ we can calculate the interface charge density Dit. Here the structure is simulated at gate voltage 0V to +15V Fig.3(c). As the DC voltage increases the Dit increases, and at higher voltage there is hardly any changes in interface trap charge density.
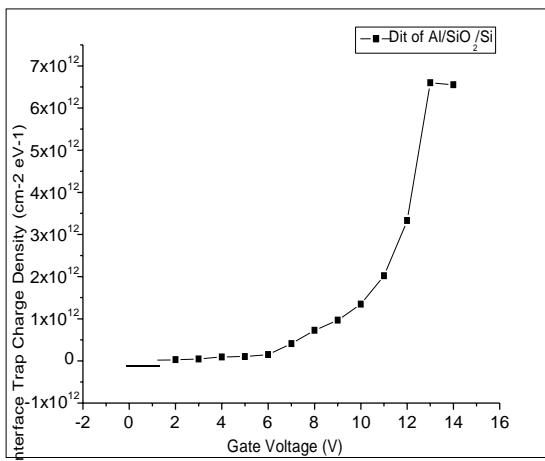

Fig .3 (c) Interface state densities versus the stress voltage for Al/SiO$_2$/Si structure. [7]

Again the reduction of depletion region capacitance reduce the interface electronic state density, which indicates the reduction of interface trap charge density and presence of dangling bond

Fig .3(d) Simulated result of Interface Trap Charge Density using varrious dielectrics.

gradually increases in ideal condition compare to the experimental condition near the interface. The capacitance value is minimum in this case. So the Dit values of the mos capacitor using varrious dielectrics are given in table-II.

TABLE – II Simulated result of Dit using various dielectrics at room temperature.

Dielectrics	Dit(cm-2 eV-1)
SiO$_2$	6.4×10^{11}
Al$_2$O$_3$	4.48×10^{11}
Y$_2$O$_3$	3.89×10^{11}
HfO$_2$	2.19×10^{11}
TiO$_2$	2.02×10^{11}

IV. TEMPERATURE DEPENDENT CHARGE BEHAVIOR

It is obtained by correlating the effect of temperature on the charges present at interface and in insulator (gate oxide) deposited on silicon substrate. Figure below shows the attained result of an analysis made by using capacitance-voltage (C-V) techniques at different measured temperatures [6].The shift in the C-V curves towards positive voltage with increase in temperature, which indicates diminish in the positive insulator charges (sum of the fixed insulator charges, mobile ionic charges, and the trapped charges in the insulator). Theoretically at room temperature (25°C), the minority carriers do not follow the high frequency (1 MHz) signal, but at higher temperature the deviation was clearly visible towards the higher positive voltage range of the C-V curve. But here in ideal case as there is no charge is generated in device, such effects are rare to be noticed. In ideal condition the interface trap charge density measured in

25°C is more than the interface trap charge density measured in 100°C, (Table III). The dielectric constant measured from the highest capacitance (Cox) at accumulation region.
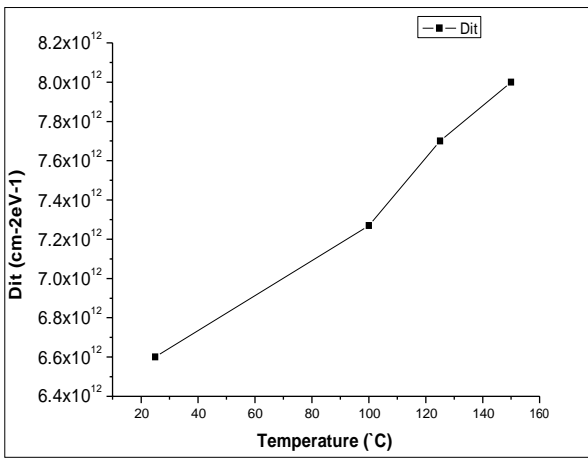

Fig.4 (a) Simulated result of Interface Trap Charge Density using Al/SiO$_2$/Si Structure.
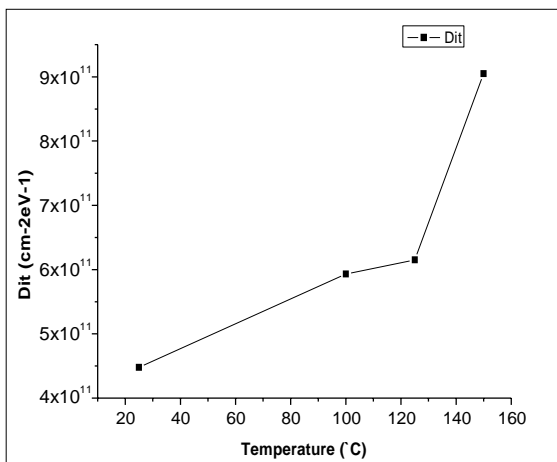

Fig.4 (b) Simulated result of Interface Trap Charge Density using Al/Al$_2$O$_3$/Si Structure.
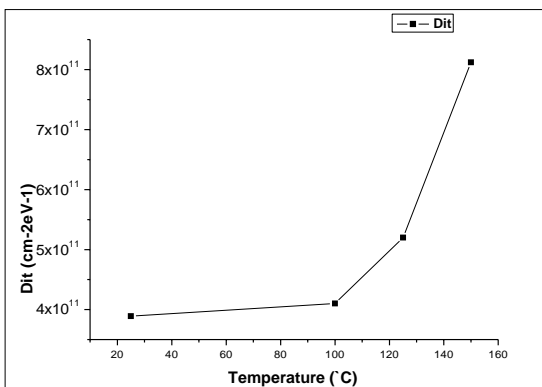

Fig.4 (c) Simulated result of Interface Trap Charge Density using Al/Y$_2$O$_3$/Si Structure.
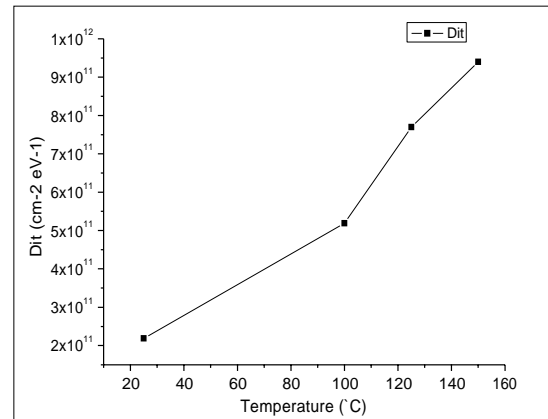

Fig.4 (d) Simulated result of Interface Trap Charge Density using Al/HfO$_2$/Si Structure.
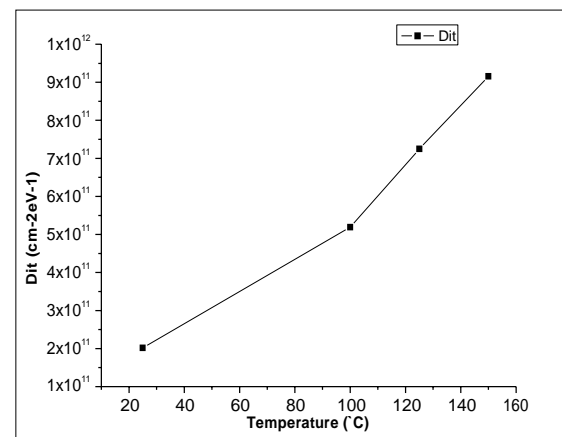

Fig.4 (e) Simulated result of Interface Trap Charge Density using Al/TiO$_2$/Si Structure.

It is observed from the stretched out of CV curve that Dit increases with increasing temperature from 25°C to 150°C as shown in table-III [fig no.4(a),(b),(c),(d),(e)]. This may be due to the generation of thermally induced defects. It is also reported that the higher temperature produces more defects due to dislocations near the valance and conduction band.

TABLE III: Measured Dit of varrious dielectrics films at different temperature.

Temp (°C)	Al$_2$O$_3$ (Dit x10^{11})	Y$_2$O$_3$ (Dit x10^{11})	HfO$_2$ (Dit x10^{11})	TiO$_2$ (Dit x10^{11})
100	5.9	4.1	5.1	5.1
125	6.15	5.2	7.7	7.2
150	9.05	8.12	9.4	9.1

Special Issue - 2017

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
ICIATE - 2017 Conference Proceedings

V. TEMPERATURE DEPENDENT OTHER ELECTRICAL PROPERTIES

As the temperature decreases Device performance improves and as temperature Increases, the device performance degrades. As the Temp decreases Vth increases. The threshold voltage increases at low temperature due to the increase in Fermi potential ϕf, depletion charge [16].

TABLE-IV: Measured Vth of various dielectrics at different temperature.

Temp (°C)	SiO2	Al2O3	Y2O3	HfO2	TiO2
25	0.19	0.16	0.16	0.16	0.16
100	-0.04	-0.04	-0.08	-0.04	-0.03
125	-0.11	-0.13	-0.16	-0.12	-0.12
150	-0.19	-0.19	-0.20	-0.20	-0.20

A flat band voltage that is different from zero will cause dielectrics are there whose permittivity is higher than AlN. For e.g. HFO 2 , Al 2 O 3 , ZrO 2. So a better result can be obtained from these above dielectrics by considering the discussed parameters. We have already discussed here the behavior of the different electrical parameter at high temperature. Now we can expect a better understanding of the mechanism of this material at the influence of the lower temperature.

TABLE-V: Measured Vfb of various dielectrics at different temperature.

Temp (°C)	SiO2	Al2O3	Y2O3	HfO2	TiO2
25	-0.35	-0.35	-0.35	-0.37	-0.37
100	-0.43	-0.43	-0.44	-0.43	-0.42
125	-0.44	-0.44	-0.44	-0.46	-0.45
150	-0.46	-0.46	-0.48	-0.48	-0.49

.

VI. CONCLUSION

After modeling the material, the simulated data for Capacitance- Voltage, interface trap charge density, and other electrical parameters with respect to the temperature have been validated with that of the reported ones. And from that were reached at the conclusion that because of the high permittivity, thermal stability of AlN, the discussed parameters are expected to improve considerably at high temperature, than the SiO2. We studied the various parameters taking AlN as a dielectric.

REFERENCE

[1] Y.-C. Yeo, Q. Lu, P. Ranade, H. Takeuchi, K. J. Yang, I. Polishchuk, T.-J. King, C. Hu, S. C. Song, H. F. Luan, and D.-L. Kwong, "Dual-metal gate CMOS technology with ultra-thin silicon nitride gate dielectric," *IEEE Electron Device Lett.*, vol. 22, pp. 227–229, May 2001.

[2] F. Englemark, G. Fuctnes, I.V. Katardjiev, A. Harsta, U. Smit, S. Berg, J. Vac. Sci. Technol. A 18 (4) (2000) 1609.

[3] [J.A. Ruffner, P.G. Clem, B.A. Tuttle, D. Dimos, D.M. Gonzales, Thin Solid Films 354 (1999) 256.

[4] Z.R. Song, Y.H. Yu, D.S. Shen, S.C. Zou, Z.H. Zheng, E.Z. Luo, Z. Xie, Mater. Lett. 57 (2003) 4643.

[5] T. Adam, J. Kolodzey, M.W. Tsao, J.F. Rabolt, „The electrical properties of MIS capacitors with ALN gate dielectrics", *applied surface science,* 175-176(2001),2000, p. 428-435.

[6] J. P. Kar, G. Bose, S. Tuli, 12 th International workshop on The Physics of Semiconductor Devices (IWPSD-2003), Dec.16-20, 2003, I. I. T. Madras, p. 283.

[7] Jyoti P. Kar, G. Bose*, S. Tuli "Effect of annealing on DC sputtered aluminum nitride films" Centre for Applied Research in Electronics, I.I.T. Delhi, Surface & Coatings Technology 198 (2005) 64 – 67.

[8] Niladri Pratap Maity, A. K. Pandeya and Reshmi Maity, Capacitance-Voltage Analysis for Al2O3 based High-K Dielectric MOS Devices, IJCSI International Journal of Computer Science Issues, Vol. 9, Issue 5, No 2, and September 2012.

[9] Wei-Chieh Kao, IMPACT OF INTERFACE STATES ON SUB-THRESHOLD RESPONSE OF III-V MOSFETs, MOS HEMTs And TUNNEL FETs, The Pennsylvania State University ,The Graduate School, College of Engineering, august 2010.

[10] S. M. Sze "Physics of Semiconductor Devices" 2 nd ed.,1991.

[11] J. P. Kar, G. Bose*, S. Tuli, DC STRESS EFFECT ON CHARGE DISTRIBUTION IN SPUTTERED AlN FILMS, Journal of Electron Devices, Vol. 2, 2003, pp. 57-61.

[12] Jyoti P. Kar, G. Bose*, S. Tuli, "Correlation of electrical and morphological properties of sputtered aluminum nitride films with deposition temperature" Centre for Applied Research in Electronics, I.I.T. Delhi, Surface & Coatings Technology, Current Applied Physics 6 (2006) 873–876.

[13] C.C. Tin, Y. Song, T. I. Smith, V. Madangarli, T. S. Sudarshan, J. of Electronic Materials, 26(3) (1997) 212.

[14] M. P. Thompson, A. R. Drews, C. Huang, G. W. Auner, MRS Internet. J. Nitride Semicond. Res. 4S1 (1999) G3.7.

[15] ATLAS User's Manual, vols 1-2, SILVACO International,1998.

[16] Neha Goel, Ankit Tripathi, Temperature effects on Threshold Voltage and Mobility for Partially Depleted SOI MOSFET, nternational Journal of Computer Applications (0975 – 8887) Volume 42– No.21, March 2012.