INTERLEAVED HIGH STEP-UP SINGLE ENDED PRIMARY INDUCTOR CONVERTER WITH BUILT-IN VOLTAGE DOUBLER CELL FOR DISTRIBUTED PV AND WIND GENERATION SYSTEM

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ABSTRACT- In this paper, the concept of built-in voltage doubler cell is derived to generate an improved interleaved high step-up converter for distributed photovoltaic and wind generation applications. The voltage doubler capacitors are charged and discharged alternatively to improve the voltage gain to improve the circuit performance. All these factors benefit the circuit performance improvements in the high step-up voltage applications. Thus the conventional system is modified with a SEPIC converter with a built in voltage doubler cell to improve the system voltage and increased stability. Simulation and analysis of the system has been done to study the performance of the high step up SEPIC converter with built in voltage doubler cell.

I INTRODUCTION

The renewable energy-based distributed generation systems are warmly welcomed and grown up rapidly in recent years, which are powered by multiple sources such as the fuel cells, photovoltaic (PV) panels, and batteries . Unfortunately, the output voltage of most PV panel is lower than 50 V and the PV series-connected configuration is the commonly employed solution to satisfy the second-stage grid-connected inverter applications. However, the PV light-to-electric energy conversion efficiency is degraded due to the panel mismatch and partial shading. It is reported that the PV panel parallel connected structure is more efficient than the series-connected configuration in the residential PV grid-connected system.

Meanwhile, only a low voltage is generated with parallel connected configuration, which is easily to satisfy the safety requirements in the home applications. Therefore, high step-up converters with nearly ten times voltage gain are required as the front-end stage to step the low voltage below 50 V up to about 400 V bus voltages.

Once a large number of PV panels are with parallel-connected configuration, these high step-up converters are expected to have the clear advantages of large voltage conversion ratio, high current conversion, and high efficiency. The conventional boost converters are not the preferable candidates in the high step-up conversion system because only the switch duty cycle can be adopted to regulate the voltage gain, which results in extremely narrow turn-off time, large peak current, and considerable conduction and switching losses. To improve the conversion efficiency and achieve large voltage conversion ratio, the switched capacitor-based converters are proposed in .

Unfortunately, the switched capacitor technique makes the switch suffer high transient current and large conduction losses. Furthermore, many switched capacitor cells are indispensable to obtain extremely high step-up conversion, which increases the circuit complexity. The coupled inductor-based converters are another solution to realize high step-up gain because the turn's ratio of the coupled inductor can be employed as another control freedom to extend the voltage gain. However, the input current ripple is relatively large by employing single-stage single-phase-coupled inductor-based converters, which shortens the usage life of the input electrolytic capacitor.

A family of interleaved high step-up boost converters with winding-cross-coupled inductors is proposed in . The active clamp or passive lossless clamp circuits are adopted to achieve soft-switching operation. Furthermore, some interleaved high step-up converters with simplified coupled inductors are introduced to derive more compact circuit structure . The built-in transformer concept is another excellent candidate applied in the high step-up applications by adjusting the turn's ratio of the built-in transformer.

The input current ripple is small due to the input inductors existed in these converters. A zero-voltage transition (ZVT) interleaved boost converter with three-winding built-in transformer is proposed in. By regulating the turn's ratio, the voltage gain is extended and the switch voltage stress is reduced. Furthermore, ZVS soft-switching performance is achieved for all switches. However, the voltage stress of the output diode is twice of the high output voltage. In this paper, the concept of built-in transformer voltage doubler cell is derived by investigating the detailed operation of the three-winding built-in transformer based converter in .

The additional voltage doubler capacitors can be charged or discharged alternatively to double the voltage gain. Both the switch duty cycle and the transformer turns ratio are employed as two controllable freedoms to lift the voltage ratio.

Compared with the original converter introduced in , due to the built-in transformer voltage doubler cell, the voltage stresses of the switches and the diodes can also be reduced, which makes the low voltage-rated power devices practicable to improve the circuit performance. These factors further improved the circuit performance in the high step-up and large current conversion system.

II CONVERTER PERFORMANCE ANALYSIS AND COMPARISON

In order to simplify the circuit performance analysis, the voltages on the clamp capacitors Cc 1 and Cc 2 , and the voltage doubler capacitors Cd 1 and Cd 2 are considered to be constant during the whole switching transition. The detailed circuit performance of the proposed converter is analyzed as follows.

Assuming the built-in transformer is well coupled and the leakage inductance is zero, from the steady analysis in previous section, it can be drawn that the input filter inductor is charged by the input voltage during the switch turn-on period and discharged by the voltage of the clamp capacitor voltage minus the input voltage during the switch turn-off period. By applying the voltage-second balance to the input filter inductor, it can be denoted as

$$VinDTs = (VCc - Vin)(1 - D)Ts \quad (1)$$

where Ts is the switching period, D is the duty cycle of the main switch, and VCc is the clamp capacitor voltage. Therefore, the clamp capacitor voltage can be represented as

$$VCc = VCc1 = VCc2 = Vin\ 1 - D. \quad (2)$$

Moreover, the primary voltage of the built-in transformer VLa is equal to that of the clamp capacitor Cc 2 in stage 4. The voltages on the secondary winding Lb and the third winding Lc are in the same value due to the same turns. Accordingly the output voltage Vout can be calculated as

$$Vout=2(N+1)Vin1–D. \quad (3)$$

Hence, the voltage gain can be represented as

$$M = Vout\ Vin = 2(N + 1)\ 1 – D. \quad (4)$$

The relationship between the voltage gain and the duty cycle in the conventional interleaved boost converter, the converter mentioned in the IEEE trasnsactions, and the improved converter is shown in Fig. It can be concluded that the voltage gain of the converter published in earlier paper is much higher than that of the conventional interleaved boost converter due to the built-in transformer. Because the voltage gain of the converter published in earlier paper is related not only to the duty cycle, but also to the turns ratio of the built-in transformer, the higher voltage gain can be obtained by regulating the turns ratio of the built-in transformer properly.

However, the voltage gain of the improved converter is twice that of the converter published in earlier paper due to the inserted voltage doubler besides the built-in transformer. So, the improved converter is more suitable for the high step-up and high output voltage applications.

In high step-up and high output voltage applications, the conduction losses and the switching losses are large with the conventional interleaved boost converter due to the large current ripple, the high switch voltage stress, and the serious diode reverse-recovery problem. Compared with the conventional interleaved boost converter, the extremely narrow turn-off time is extended, the switch voltage stress is reduced, and the switch current ripple is minimized to reduce the conduction losses due to the voltage gain extension by employing the built-in transformer voltage doubler cell.

Furthermore, by introducing the active clamp scheme, ZVS soft-switching performance is realized for both the main and the clamp switches during the whole switching transition. Because the diode reverse-recovery problem is alleviated by the leakage inductance of the built in transformer, the diode reverse-recovery losses are reduced. So, the proposed converter is suitable for high step-up, high efficiency, and high current conversion.

III EXPERIMENTAL VERIFICATIONS

The performance of the proposed converter is verified by the experimental results based on a laboratory prototype. The experimental results of the ZVS soft-switching performance of the main switch S1 and the clamp switch Sc 1. it is clear that the drain–source voltages Vds1 and Vdsc 1 have been decreased to zero before S1 and Sc 1 are turned ON, respectively. Thus, the switches S1 and Sc 1 are both turned ON at ZVS.

According to(b) and (d), it can be seen that the drain–source voltages Vds 1 and Vdsc 1 begin to increase after the gate voltages Vgs1 and Vgsc 1 decrease to below the threshold voltage of the switch. Then, switch S1 and Sc 1 are both turned OFF at ZVS. Therefore, ZVS soft-switching performance is achieved for both the main and clamp switches.

Furthermore, the drain–source voltages of S1 and Sc 1 are only about 100 V during the switch off period, which is far lower than the 380-V output voltage Therefore, the low-voltage-rated switch can be adopted to reduce the conduction losses for the proposed converter. The experimental results of the input inductor currents iL 1 and iL 2 , the clamp capacitor voltage vCc1, the main switch drain–source voltage vds1 are given.

Vin (Input Voltage)	40 V
Vout (Output Voltage)	380 V

Table 1 : The table shows Comparison of Improved Voltage Output of existing system.

Fs = 100 khz	L1,L2 =50 µH	LLK =1.9µH
Cc1,Cc2 = 4.7 µF	Cs1,Cs2 = 1.36 nF	Co = 470 µF
N= 14/14	D01, D02= MUR1560	S1,S2 = Main Switch

Table 2 - circuit parameters of the existing system.

For the input inductors and the built in transformer, the copper and core losses are both calculated. Besides the ignorable losses mentioned previously, the driver losses, the losses on the parasitic parameters of components, etc., are all ignored.

As a result, the calculated efficiency, 96.8%, is a little higher than the measured efficiency, 96%. In the total power losses, the ratios of each element power losses are also given in Table III. By analyzing the power losses distribution, it can be concluded that the major losses are in the main switches, the diodes, and the input inductors. The power losses in the clamp switches are small.The three windings are labeled in the photo. An EE55 core is employed for the 1-kW prototype.

IV SEPIC DOUBLER CELL TOPOLOGY

This paper introduces a quasi-resonant single-ended-primary inductor- converter (SEPIC) converter. The SEPIC converters are high efficiency systems. It also has the benefit of stepping up and stepping down conversion ability with excellent transient response.

In the SEPIC Converters no bulk inductor is used and the converter operates at fixed frequency and duty ratio. These attributes reduce passive component size, improve response speed. Furthermore, a new fixed-frequency ON/OFF control is introduced which provides good control.

The Rapid load disturbance rejection is enabled by the small passive component values and Limited slew rate of the output voltage, appropriate for applications such as adaptive bias power supplies. Above all Wide operating range, small size, and excellent transient response while maintaining good efficiency are the advantages of the SEPIC converters..

Vi = 40 V	L1 = 1500e-6 H	Ls = 1.5e-3 H
C1= 1500e-6 F	CO = 2200e-6 F	RL = 1000 Ω
D1 to D5=0.001 Ω	C1 to C6 = 470e-6F	Sc1,Sc2 = Switches

Table 3 - circuit parameters of the Proposed system.

The above table 4.3 shows the circuit parameters of the proposed system with RL load value 1000 Ω and an input voltage value of 40 V. The value of inductor L , capacitors C and switches are shown in table 4.3

V SIMULATION MODEL OF PROPOSED SYSTEM

The Mat lab Simulink model of the Proposed system is shown in figure 4.14, which employs an Interleaved High Step up SEPIC converter with built in Voltage Doubler cells, With an output voltage of about 980 V.

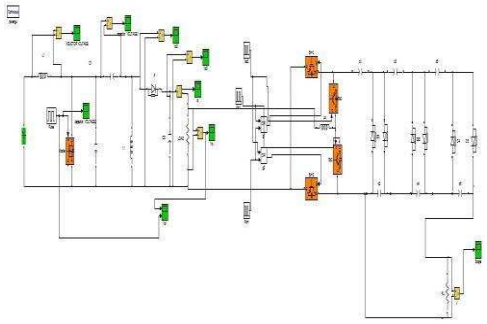

Fig1. Simulation model of Proposed System

VI SIMULATION OUTPUT OF THE PROPOSED SYSTEM

Figure shows the simulation input of the Proposed system. The input voltage of the Proposed system is 40V.

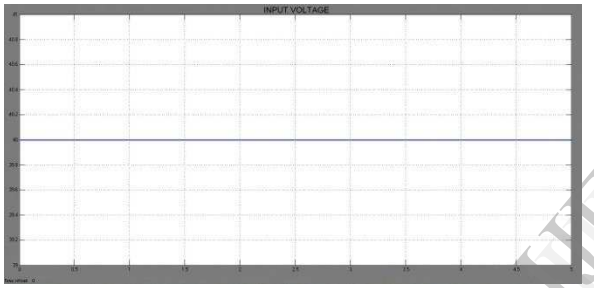

Fig 2. Simulation input of Proposed system

Figure shows the simulation of SEPIC initial output voltage of the Proposed system. The SEPIC initial output of the Proposed system is about 130 V

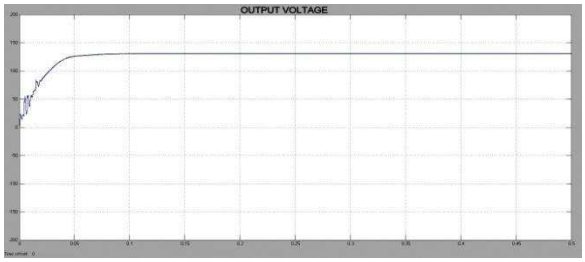

Fig 3. Simulation SEPIC initial output of Proposed System

Figure shows the simulation of SEPIC final output voltage of the Proposed system.

The SEPIC Final output of the Proposed system is about 1000 V.

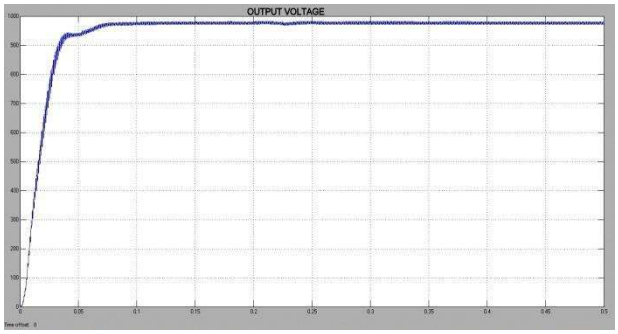

Fig 4. Simulation Final Output of Proposed System

VII INFERENCE

A SEPIC converter based integrated PV-WIND generation system has been modeled.

The system I/P voltage level was 40 V DC, which is fed from a distributed PV & WIND generation system.

The SEPIC converter output after conversion is 132V.

The final output of the system reaches a much improved voltage level of about 1000V, gives its place in embedded generation system.

Voltage spike problem has been eliminated with a damped SEPIC conversion stage and voltage doublers make the O/P voltage to reach the improved level

VIII CONCLUSION

An Advanced high step up SEPIC converter with voltage doubler cell has been introduced. The final output of the interleaved high step up Single ended primary inductor converter with voltage doubler cell system reaches a much improved voltage level of about 1000V, which gives its place in distributed wind and Photovoltaic generation systems. In the proposed system the built in transformer is eliminated with the voltage doubler cells efficiently, thus the cost of construction could e reduced. The Voltage spike problem in the interleaved high step up ZVT converter with build in transformer voltage doubler

cell has been eliminated with a damped SEPIC conversion stage and voltage doublers makes the O/P voltage to reach the improved level.

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