Investigation of Switching Angles Corresponding to the Elimination of Voltage Harmonics in Asymmetrical Seven Level Inverters

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Abstract - **This work discusses the investigation of notches corresponding to the elimination of voltage harmonics in single phase seven level asymmetrical inverter. The simulation is done using MATLAB-Simulink environment for modulation index m_a = 0.8 and for various modulation frequencies m_f. The reference is a stepped wave form and the carrier are triangular carrier are used for generation of pulse width modulation (PWM) in order to turn on the switches. Performance parameters are root mean square value of output voltage, DC component in output voltage, Average of output voltage, form factor, total harmonic distortion and crest factor are compared and analyzed for various carrier frequencies. It was found that the THD is better in few of the modulation index and eliminated in case of few cases**.

INTRODUCTION

Multilevel inverters plays an important role in the area of power electronics and power systems. The several output levels of the multilevel inverter aides them to be used in PV based plants. The carrier frequency f_c determines the number of pulses per half cycle. The modulation index (m_a) controls the output voltage. Tolbert et al [1] have derived a procedure to find all sets of switching angles for which the fundamental is produced while the 5th and 7th are eliminated. Sun and Yun [2] have proposed a hybrid PWM method for the new topology that has different cells working in different switching frequencies in order to achieve low switching losses. Palanivel and Dash [3] have developed various carrier based pulse width modulation techniques which can minimize the total harmonic distortion and enhance the output voltage for a five level inverter. Shanthi and Natarajan [4] presented the use of Control Freedom Degree (CFD) combination. The effectiveness of the Pulse Width Modulation (PWM) strategies developed using CFD are demonstrated by simulation. Du et al [5] discussed about the control of seven-level Hybrid Cascaded Multi Level Inverter (HCMLI) with fundamental frequency switching control and how its modulation index (m_a) range can be extended using triplen harmonic compensation. Xiao et al [6] have proposed a strategy to minimize harmonics and achieve zero error tracking. Tolbert et al [7] explored the benefits and discussed control schemes of the cascade inverter for use as an Electric Vehicle (EV) motor drive or a parallel Hybrid Electric Vehicle (HEV) drive and the diode-clamped inverter as a series HEV motor drive. Josh and Jerome [8]have stated that the power quality improvement can be achieved by reducing the harmonics at the output voltage of the inverter. Colak et al [9] have done intensive studies and have proposed carrier based sinusoidal space vector and sigma delta PWM methods in open loop control of inverters. Seyezhai and Mathur   [10] have reduced the switching losses and improved the power quality using variable frequency inverted sine PWM strategy. Lau et al [11] have found analytical solutions for determining the spectral characteristics of multicarrier based multilevel PWM pulses for the inverters. Carrier-based PWM modulation for reduction of THD and losses in multilevel inverters was studied by Barreto et al [12]. Yousef poor et al [13] have found an optimization algorithm to get a reduced THD. Batschauer et al [14] explored the hybrid multilevel inverter with half bridge circuit with unidirectional power flow. Cougo et al [15] have analysed and found that the Phase Disposition (PD) method is the best method to reduce the current imbalance in multilevel inverter. This paper investigates the switching angles for various switching frequencies of carrier PDPWM strategies using stepped reference for chosen single phase AMLI.

Several inverters are series connected, with different topologies and different input voltages. Hence they are said to be AMLIs. A seven level output voltage is achieved with two bridges in asymmetrical inverter whereas only five level output voltage will be achieved with two such bridges in case of conventional cascaded MLI. In AMLI more voltage levels can be achieved with lesser number switches. Figure1 shows the chosen asymmetrical single phase inverter. Each cell has two pairs of complementary switches S_{11} and S_{22} and S_{12} and S_{21}. The single phase asymmetrical seven level uses lesser number of switches and produces more output levels. The topology used in this paper is two cascaded H-bridges with eight switches. The modulation strategies used are the phase opposition disposition pulse width modulation with triangular carrier and stepped reference. The analysis is done for various carrier frequencies such that the angles are calculated for each carrier frequencies.

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The results are tabulated for mf various frequencies from 1203 hertz to 1224 hertz. The frequencies are so chosen that they suppress, recuse or eliminate the third order harmonics.
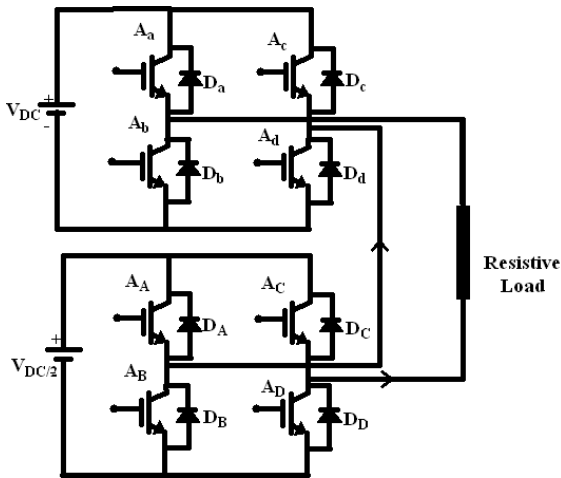

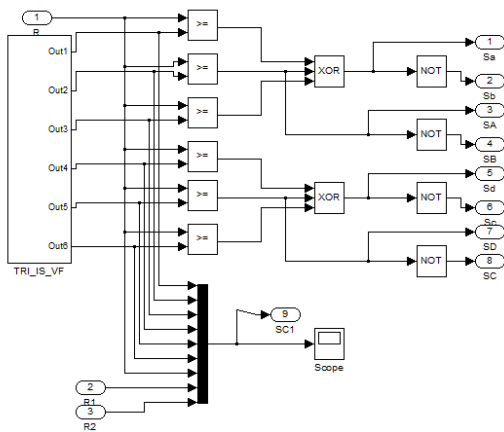Fig.1. Single phase asymmetrical cascaded seven level inverter

Simulation Results

Fig.2. Sample PWM generation logic developed using MATLAB-SIMULINK for bipolar VFPWM technique
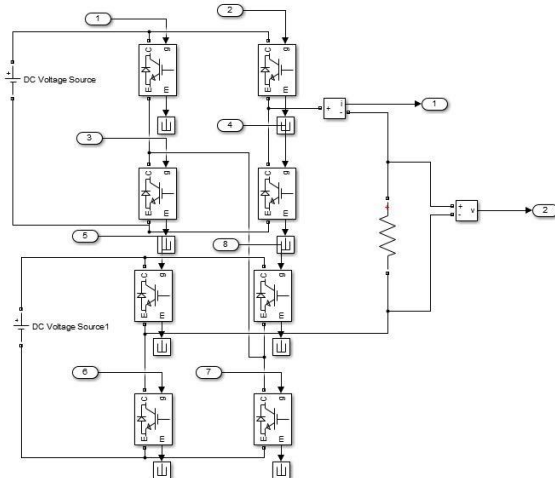
Fig.1. Single phase asymmetrical cascaded seven level inverter MATLAB simulation model

Table.1.
Fs=1203 and mf=24.06

m_a	DC	V_{peak}	V_{rms}	THD	FF
0.7	0.5893	104.6	73.96	26.06	177.4987
0.75	0.1165	111.9	79.13	26.67	960.515
0.8	0.3029	119.5	84.51	25.45	394.5196
0.85	0.131	127	89.83	24.5	969.4656
0.9	0.06986	134.5	95.09	23.7	1925.279
0.95	0.3259	141.8	100.3	21.86	435.1028
1	0.5391	149.1	105.4	19.02	276.5721

Table.2.
Fs=1206 and mf=24.12

m_a	DC	V_{peak}	V_{rms}	THD	FF
0.7	0.495	104.5	73.87	25.89	211.1111
0.75	0.2098	112.2	79.35	26.52	534.795
0.8	0.3262	119.7	84.61	25.34	366.9528
0.85	0.2796	127.2	89.97	24.38	454.9356
0.9	0.04655	134.4	95.05	23.68	2887.218
0.95	0.1164	141.4	100	21.89	1214.777
1	0.3514	148.9	105.3	19.16	423.7336

Table.3.
Fs=1209 and mf=24.18

m_a	DC	V_{peak}	V_{rms}	THD	FF
0.7	0.3534	104.2	73.65	25.65	2.95E+02
0.75	0.02331	112.4	79.48	26.42	4.82E+03
0.8	0.09315	120.1	84.91	25.29	1.29E+03
0.85	0.3027	127.2	89.96	24.19	4.20E+02
0.9	0.1164	134.2	94.88	23.46	1.15E+03
0.95	1.64E-07	141.2	99.85	21.83	8.59E+08
1	0.1171	148.4	105	19.15	1.27E+03

Table.4.
Fs=1212 and mf=24.24

m_a	DC	V_{peak}	V_{rms}	THD	FF
0.7	0.1649	104.1	73.64	25.5	6.31E+02
0.75	0.0233	112.5	79.53	26.43	4.83E+03
0.8	0.0466	120.4	85.13	25.19	2.58E+03
0.85	0.1397	127.6	90.22	23.95	9.13E+02
0.9	0.1164	134.2	94.92	23.26	1.15E+03
0.95	0.04653	141.4	99.75	21.65	3.04E+03
1	1.71E-07	148.3	104.9	18.91	8.69E+08

Table.5.
Fs=1215 and mf=24.3

m_a	DC	V_{peak}	V_{rms}	THD	FF
0.7	0.07065	104.2	73.65	25.54	1.47E+03
0.75	0.1398	112.6	78.6	26.24	8.05E+02
0.8	0.06989	120.5	85.23	25.04	1.72E+03
0.85	0.1398	112.6	79.6	26.24	8.05E+02
0.9	0.04653	134.3	94.96	23.05	2.89E+03
0.95	0.04651	141	99.72	21.51	3.03E+03
1	0.07025	148.3	104.9	18.86	2.11E+03

Table.6.
Fs=1218 and mf=24.36

m_a	DC	V_peak	V_rms	THD	FF
0.7	0.1884	104.2	73.65	25.54	5.53E+02
0.75	0.1164	112.5	97.54	26.16	9.66E+02
0.8	0.02328	120.7	85.35	24.81	5.18E+03
0.85	0.04655	127.9	90.44	23.69	2.75E+03
0.9	1.16E-07	134.6	95.19	22.99	1.16E+09
0.95	0.1163	141.2	99.86	21.39	1.21E+03
1	0.09367	148.2	104.8	18.8	1.58E+03

Table.7.
Fs=1221 and mf=24.42

m_a	DC	V_peak	V_rms	THD	FF
0.7	0.3768	104.2	73.69	25.77	2.77E+02
0.75	0.3491	112.2	79.35	26.31	3.21E+02
0.8	0.3259	120.4	85.1	24.79	3.69E+02
0.85	0.02327	127.6	90.23	23.74	5.48E+03
0.9	0.1163	134.5	95.11	23	1.16E+03
0.95	0.186	141.3	99.93	21.36	7.60E+02
1	0.1404	148.4	104.9	18.63	1.06E+03

Table.8.
Fs=1224 and mf=24.48

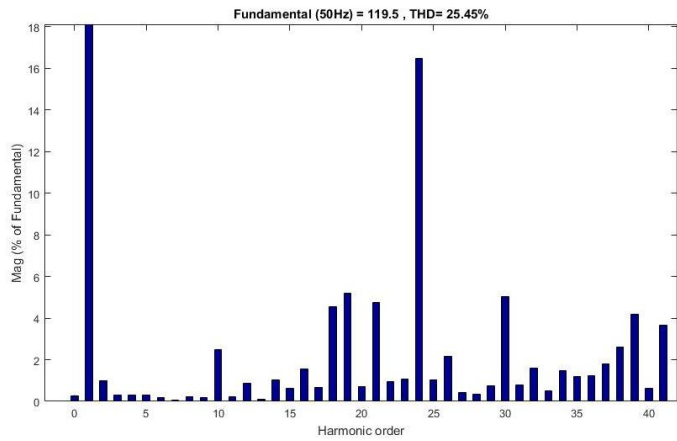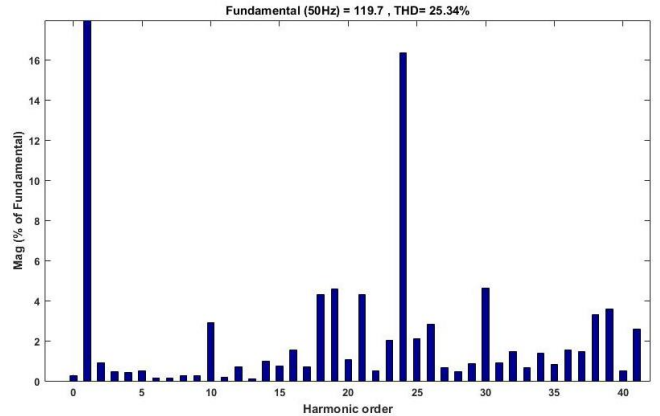| m_a	DC	V_peak	V_rms	THD	FF
0.7	0.04946	104.3	73.77	25.96	2.11E+03
0.75	0.5822	112	79.17	26.34	1.92E+02
0.8	0.5819	119.8	84.72	24.95	2.06E+02
0.85	0.09306	127.4	90.11	23.74	1.37E+03
0.9	0.04653	134.6	95.15	23.03	2.89E+03
0.95	0.3256	141.5	100	21.41	4.35E+02
1	0.2576	148.5	105	18.61	5.76E+02

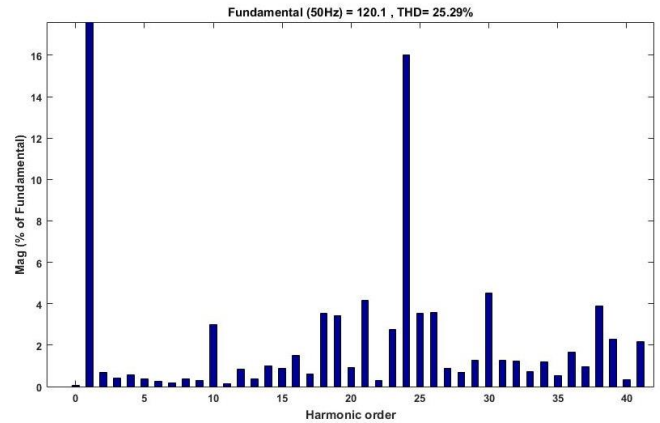Fig.2. THD for m_a=0.8, f_s=1206 and m_f=24.12

Fig.3. THD for m_a=0.8, f_s=1209 and m_f=24.18

Fig.4. THD for m_a= 0.8, f_s=1209 and m_f=24.24
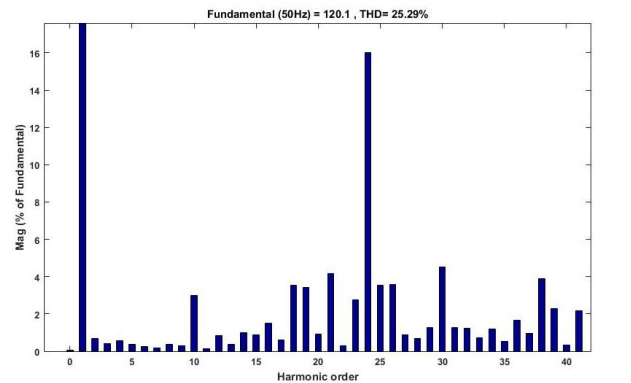

Fig.1. THD for m_a=0.8, f_s=1203 and m_f=24.06
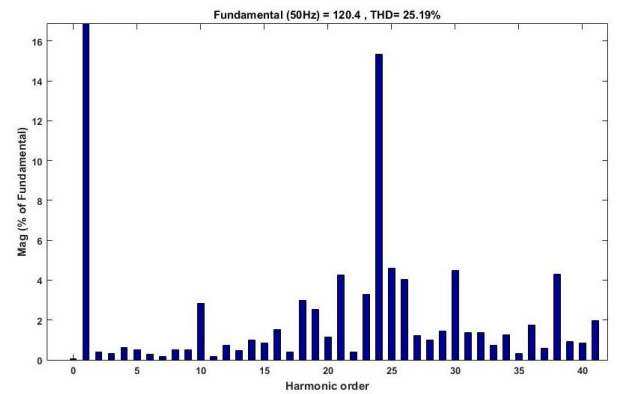

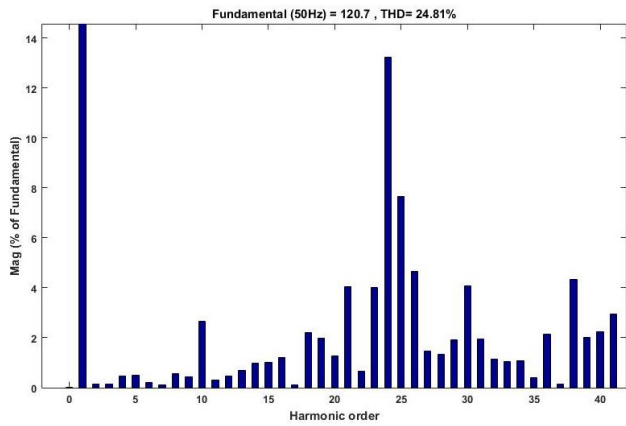Fig.5. THD for m_a= 0.8, f_s=1212 and m_f=24.24

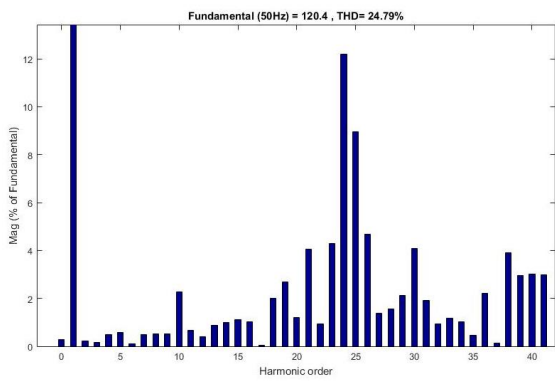Fig.6. THD for m_a= 0.8, f_s=1218 and m_f=24.36

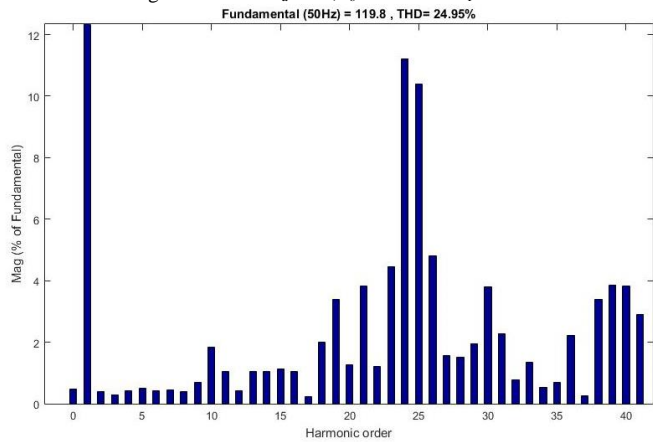Fig.7. THD for m_a= 0.8, f_s=1221 and m_f=24.42

Fig.8. THD for m_a= 0.8, f_s=1224 and m_f=24.48

I.a. PDPWM STRATEGY

In this strategy carriers have same frequency, amplitude and phase, but they are just different in DC offset to occupy contiguous bands. For this technique, significant harmonic energy is concentrated at the carrier frequency f_c but because it is a co-phase component, it does not appear in the line voltage. It should be noted that the other harmonic components are centered on the carrier frequency as sidebands. This technique employs (m-l) carriers which are all in phase for a m level inverter. In seven level converter all the six carrier waves are in phase with each other across all the bands as described in Fig.3 for a phase leg of a seven level AMLI structure with $m_a = 0.8$. The pulse pattern for AMLI with hybrid carriers Stepped sine PDPWM strategy is employed.
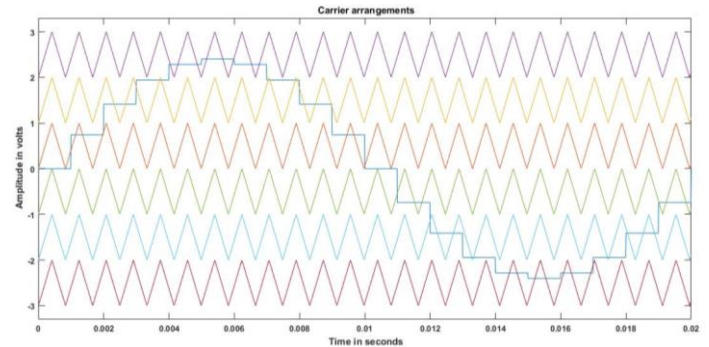

Fig.9 Carrier arrangement for m_a=0.8, f_s=1203 and m_f = 24.06
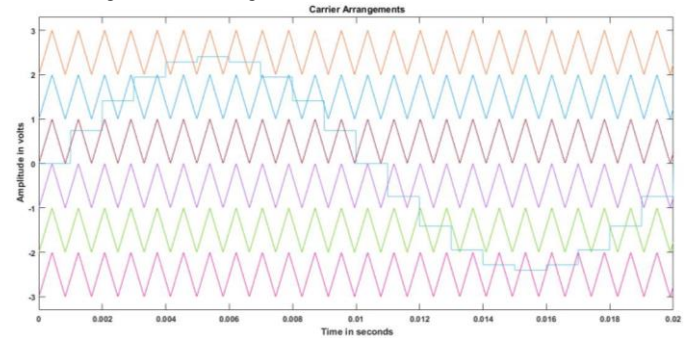

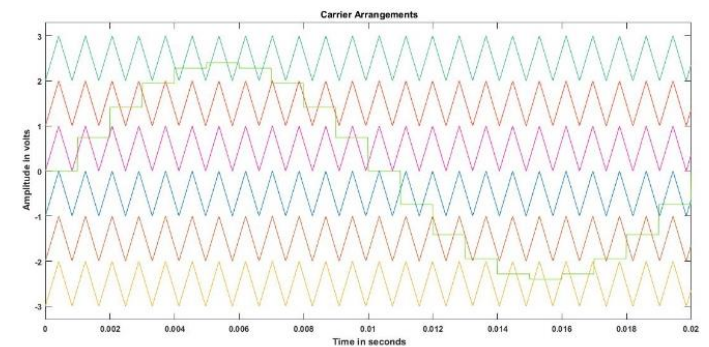Fig.10 Carrier arrangement for m_a=0.8, f_s=1206 and m_f=24.12

Fig.11 Carrier arrangement for m_a=0.8, f_s=1209 and m_f = 24.24

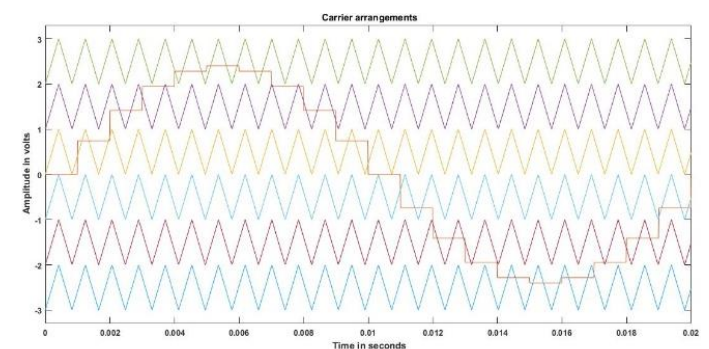

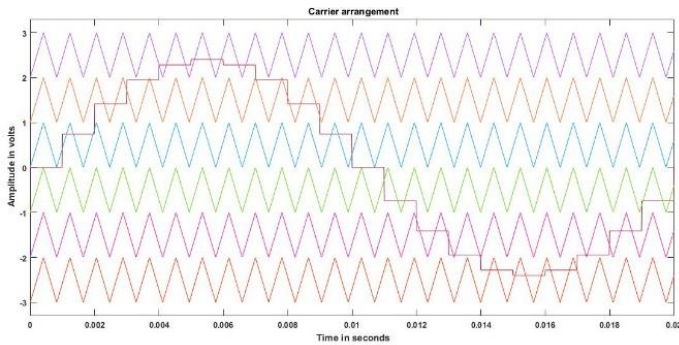Fig.12 Carrier arrangement for m_a=0.8, f_s=1212 and m_f=24.18

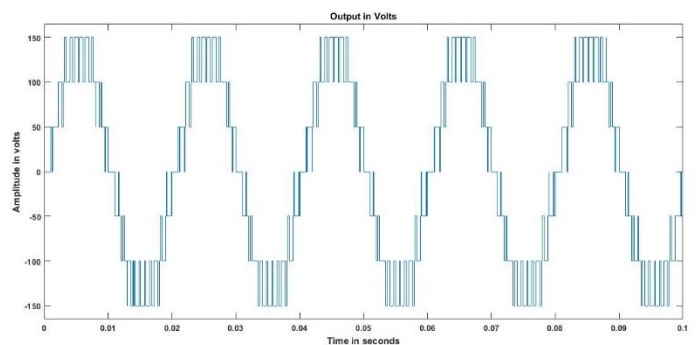Fig.13 Carrier arrangement for m_a=0.8, f_s=1215 and m_f=24.24

Fig.14 Carrier arrangement for m_a=0.8, f_s=1218 and m_f=24.36

Fig.14 Carrier arrangement for m_a=0.8, f_s=1221 and m_f=24.42

Fig.14 Carrier arrangement for m_a=0.8, f_s=1224 and m_f=24.48

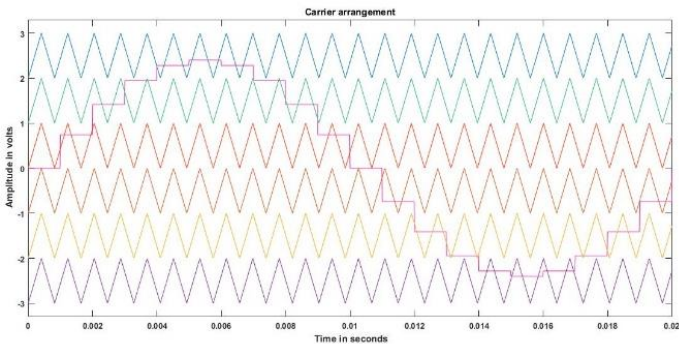Fig.15 Sample output voltage for m_a=0.8, f_s=1224 and m_f=24.48
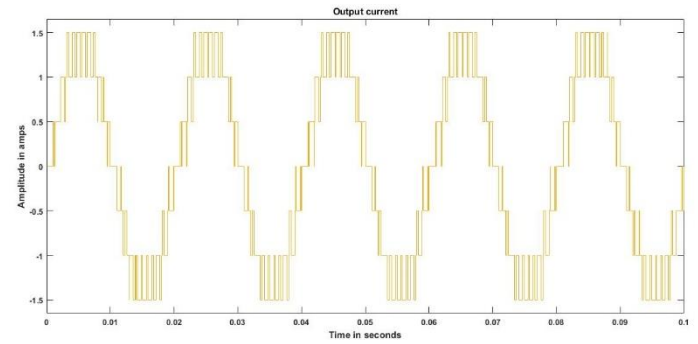
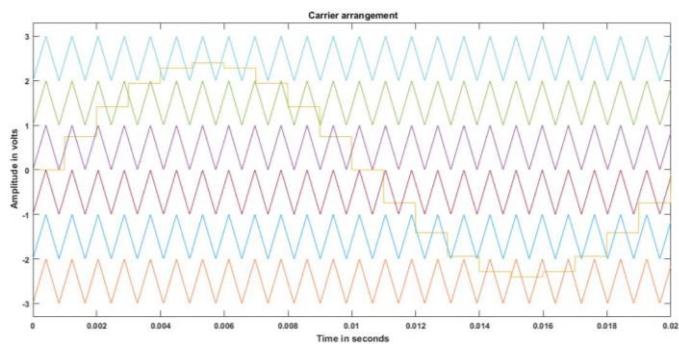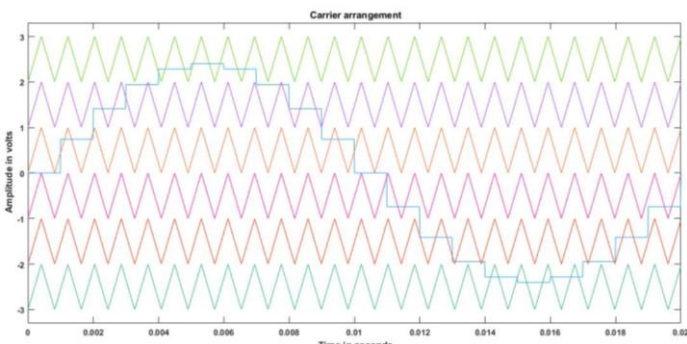Fig.16 Sample output current for m_a=0.8, f_s=1224 and m_f=24.48

ANALYSIS

CONCLUTION

The paper investigated the switching angles corresponding to the elimination of voltage harmonics in asymmetrical seven level inverters. It was found that the THD is better in few of the modulation index and eliminated in case of few cases.

REFERENCES

[1] L. M. Tolbert, J. Chiasson, K. Mckenzie, and Z. Du, 2005. "Elimination of Harmonics in a Multilevel Converter with Non Equal DC Sources",IEEE Transactions On Industry Applications, Vol. 41, No. 1, January/February pp. 589-595, 2003.

[2] X. Sun and Yun, "Multi-carrier PWM Control Method of a Novel Asymmetrical Multilevel Inverter", 2010. in Third International Conference on Intelligent Networks and Intelligent Systems, pp. 556-559.

[3] P. Palanivel P. and S. S. Dash, 2010. "Analysis of THD and output voltage performance for cascaded multilevel inverter using carrier pulse width modulation techniques", IET Power Electronics Received on 31st, vol. 4, no. pp. 951-958.

[4] B. Shanthi and S. P. Natarajan, 2008."Carrier overlapping PWM methods for single phase cascaded five level inverter", IJ-STA, Special Issue, CEM, December, pp. 590-601.

[5] Z. Du, L. M. Tolbert, S. Member, B. Ozpineci, and J. N. Chiasson, 2009. "Seven-Level Hybrid Cascaded H-Bridge Multilevel Inverter", IEEE Transactions On Power Electronics, pp. 25-33.

[6] B. Xiao, F. Filho, and L. M. Tolbert, 2011. "Single-Phase Cascaded H-Bridge Multilevel Inverter with Nonactive Power Compensation for Grid-Connected PhotovoltaicGenerators",EnergyConversionCongressandEx position(ECCE), IEEE pp. 2733-2737.

[7]   L. M. Tolbert, F. Z. Peng and T. G. Habetler, 2009. "Multilevel Inverters for Electric Vehicle Applications", WPET '98, Dearborn, Michigan, October 22-23, pp. 79-84.

[8]   P. T. Josh and J. Jerome, 2011."The Comparative Analysis of Multicarrier Control Techniques For SPWM Controlled Cascaded H-Bridge Multilevel Inverter", proceedings of ICETECT pp. 459-46.

[9]   I.Colak, E.Kabalci and R.Bayindir, 2010."Review of multilevel voltage source inverter topologies and control schemes",energy conversion and management, Elsevier.

[10]   R. Seyezhai and B.L.Mathur 2007."Investigation of Variable Frequency ISPWM Control Method for an Asymmetric Multilevel Inverter", International Journal of Electrical & Computer Sciences IJECS vol: 9 No: 10 pp. 55-64.

[11]   W.H Lau, Bin Zhou and H.S.H Chung, 2004. "Compact analytical solutions for determining the spectral characteristics of multicarrier-based multilevel PWM", IEEE Transactions on Circuits and Systems, (Aug.2004),vol.51, no.8, pp. 1577- 1585.

[12]   L. H. S. C. Barreto, G. A. L. Henn, P. P. Praca, R. N. A. L. Silva, D. S. Oliveira, and E. R. C. da Silva, 2012. "Carrier-based PWM modulation for THD and losses reduction on multilevel inverters", in Applied Power Electronics Conference and Exposition (APEC), Twenty-Seventh Annual IEEE, pp.2436-2441.

[13]   N. Yousefpoor, S.H. Fathi, N. Farokhnia, H.A. Abyaneh, 2012. " THD Minimization Applied Directly on the Line-to-Line Voltage of Multilevel Inverters ," *IEEE Trans. on Industrial Electronics,* vol. 59, no. 1,pp.373-380,(Jan2012)

[14]   A.L. Batschauer, S.A. Mussa, M.L. Heldwein, 2012." Three-Phase Hybrid Multilevel Inverter Based on Half-Bridge Modules ," *IEEE Trans. on Industrial Electronics,* (Feb 2012)vol. 59, no. 2, pp. 668-678,

[15]   B. Cougo, G. Gateau, T. Meynard, M. Bobrowska-Rafal, M. Cousineau, 2012." PD Modulation Scheme for Three-Phase Parallel Multilevel Inverters ," *IEEE Trans. on Industrial Electronics,* (Feb 2012.) vol. 59, no. 2, pp. 690-700.

[16]   Omar Fethi Benaouda, Azzedine Bendiabdellah, Bilal Djamal Eddine Cherif "Contribution to Reconfigured Multi-Level Inverter Fed Double Stator Induction Machine DTC-SVM Control