Leakage Tolerance High Performance Wide Fan-In Domino Logic Circuit Design

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Abstract

Robustness of high fan-in domino circuits is degraded by technology scaling due to exponential increase in leakage. In this paper, we propose domino logic circuit techniques to improve the robustness and performance along with leakage power. In this paper a new high performance low power and noise tolerant circuit technique for wide fan-in domino logic is proposed where feedback is done from the output of CMOS inverter to the gate of footer transistor. In this domino circuit a chain of evaluation network uses well known stacking effect technique to reduce the leakage. The leakage current is also decreased by exploiting the footer transistor in diode configuration, which results in increased noise immunity. Simulation results of wide fan-in gates designed using a 65-nm high-performance predictive technology model demonstrate 51% power reduction and at least 2.41× noise-immunity improvement at the same delay compared to the standard domino circuits for 8-bit OR gates.

Keyword:- *Current mirror; Domino logic; Evaluation Delay; Keeper transistor; Noise immunity; Wide fan-in gate.*

1. Introduction

The rapid integration of VLSI circuit is due to the increased use of portable wireless systems with low power budget and microprocessors with higher speed. To achieve high speed and lower power consumption transistor technology and power supply must be scaled down simultaneously. On the other hand, as the technology scales down, the supply voltage is reduced for low power, and the threshold voltage (V_{th}) is also scaled down to achieve high performance. Since reducing the threshold voltage exponentially increases the sub-threshold leakage current improving noise immunity are of major concern in robust and high-performance designs in recent technology generations, especially for wide fan-in dynamic gates. As technology is scaled down, power supply must be scaled to decrease power consumption. However, this leads to degradation of noise immunity because of lowering the switching threshold voltage.

The leakage immunity is more problematic in high fan-in domino circuits because of larger leakage due to more parallel evaluation paths. Since the leakage current is proportional to the fan-in domino OR gate, the noise immunity also decreases with fan-in increases (Peiravi et al. 2009). Leakage and noise immunity are major issues for the wide fan-in domino OR logic, because the evaluation transistor are all in parallel, leaking the charge from pre-charge node (Moradi et al. 2004). Keeper transistor upsizing is a conventional method to improve the robustness of domino circuit. A full keeper is added in pre-charge node to improve the robustness of the dynamic node. The keeper ratio (K) is defined as the ratio of the current drivability of the keeper transistor to that of the evaluation transistor,

$$K = \frac{\mu p \left(\frac{W}{L}\right) keeper\ transistor}{\mu n \left(\frac{W}{L}\right) evaluation\ transisitor}$$

where, W and L denote the transistor size, μn and μp are the mobility of electron and hole respectively.

Keeper transistor upsizing is a conventional method to improve the robustness of domino circuits. However, as the keeper transistor is upsized the contention between the keeper transistor and the evaluation network increases in the evaluation phase. This causes an increase in the evaluation delay of the circuit, increase in power consumption and degradation of performance. Therefore, to improve noise and leakage immunity, keeper upsizing is used as a compromise between delay and power.

The paper is organized as follows. Literature review about existing domino circuit discussed in section 2. Noise immunity metrics used for Unity Noise Gain (UNG) in section 3. The proposed circuit description is in Section 4. Simulation result is presented and compared in section 5 with the brief conclusion of the paper in section 6.

2. Literature Review

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Several domino circuits have been proposed in the literature such as conventional higher fan-in domino OR logic with footer less and footer transistor, high speed domino, conditional keeper domino & Proposed technique. The main goal of these circuit design technique is to improved noise immunity and circuit performance, especially for wide fan-in circuit. The working of Footer Less Domino Logic (FLDL) is shown in Fig.1 is similar to Footed Domino Logic (FDL) shown in Fig.2.

The advantage of FDL over FLDL is more noise immune. The noise immunity is higher because of using stacking effect due to the added footer transistor at the bottom of the evaluation network. FDL is preferred for noise immune applications but its speed is lower than FLDL (Moradi and Peiravi 2005).

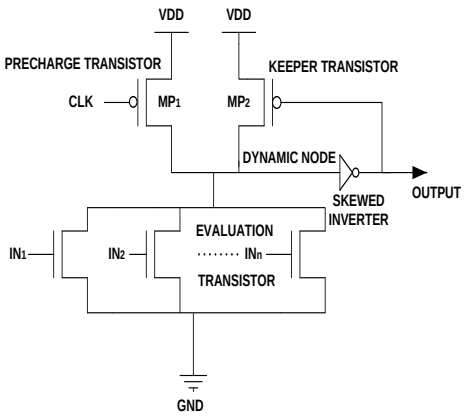

Figure.1. Conventional High Fan in Domino OR Gate with Footer less Domino Logic [FLDL]

High-speed domino logic (HS domino)

One of the existing leakage tolerant domino circuits is high speed domino logic (HSD) as shown in Fig 3. At the beginning of the evaluation phase, the input delay element is low and the clock is high. PMOS transistor MP_3 is ON and therefore it turns OFF the keeper transistor MP_2. After a delay equal to the delay of the inverters, when clock delayed is high, if the output node is high, M N_1 remains in the OFF

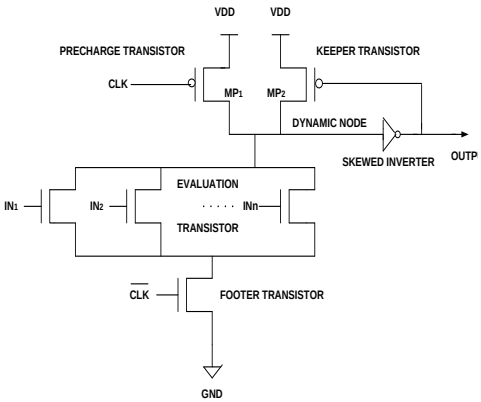

Figure2. Conventional High Fan in Domino OR Gate with Footed Domino Logic [FDL]

state and keeper transistor MP_2 remains off too. However, in the other case when output remains low after that delay (delay of inverters) in the evaluation phase, dynamic node is connected to the output node through the inverter. This causes PMOS transistor MP_2 (keeper transistor) to be turned ON to keep the dynamic node strongly connected to V_{DD} for the rest of the evaluation phase.

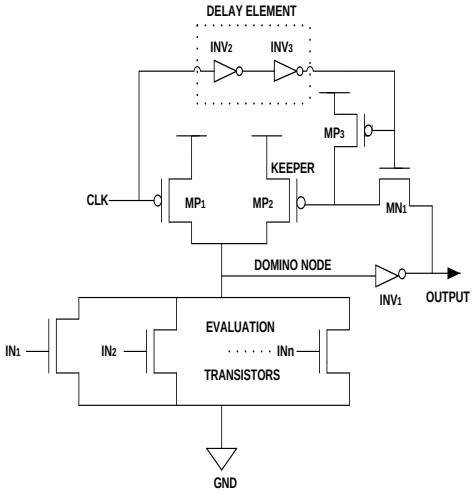

Figure.3. High Speed Domino [HSD] Logic Circuit

Conditional Keeper Domino Logic

Another existing leakage tolerant domino circuit is the Conditional Keeper Domino (CKD) logic. The circuit schematic of the conditional keeper is shown in Fig 4. The circuit works as follows: at the beginning of the evaluation phase, the smaller keeper (K1) is ON for keeping the state of the dynamic node. After delay of the inverters if the dynamic node is still high, the output of the NAND gate goes low to turn ON K2 (Zhao et al. 2007). This keeper transistor is sized larger than K1 to maintain the state of the dynamic node for the rest of the evaluation period. However, the conditional keeper remains OFF if the dynamic node is discharged to the ground. CKD logic has some problems like limitations on decreasing delays of the inverters and the NAND gate for improving noise immunity. Noise immunity can be improved by upsizing delay inverters, but this significantly increases power dissipation (Alvandpour et al. 2002).

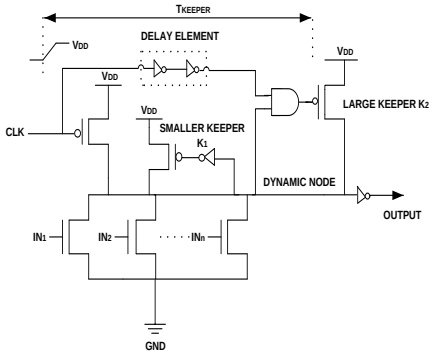

Fig.4. Conditional keeper circuit

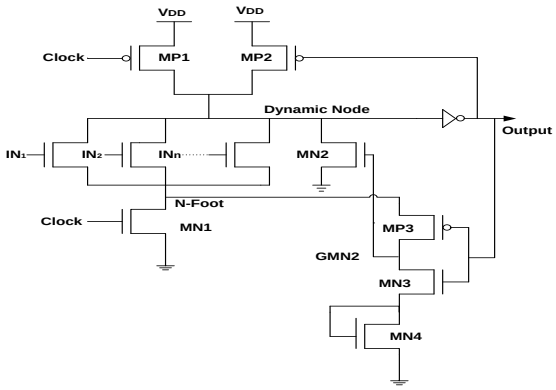

Fig.5. Proposed Circuit

3. Noise Metrics

The noise metrics is the metric that has been employed in. We apply a pulse noise to all inputs with amplitude which is a fraction of supply voltage and a pulse width equal to 50ps. Then, the amplitude of the input noise pulse is increased until the amplitude of the resulting output noise voltage is equal to that of the input noise signal. This noise amplitude is defined as Unity Noise gain (UNG):

$$UNG = \{V_{in}, V_{noise}=V_{output}\}$$

4. Proposed work

Author Proposed circuit topology is shown in Fig .5. The proposed circuit employs stacking effect(by adding the footer transistor MN1) to the tail of the evaluation NMOS tree for noise immunity improvement and uses the steady state voltage of N-FOOT node at the beginning of evaluation phase to reduce leakage of the evaluation network. The operation of the circuit is explained at different modes of operation.

Circuit Analysis

In the proposed circuit, some points have been considered. First of all we have employed the stacking effect in our scheme due to its ability to bring about improvement on noise immunity. Second, if voltage of source to bulk is greater than zero, the sub-threshold leakage current will be reduced. In fact, in this circuit we have used a conditional footer (MN1) that will be turned on if the output is low and clock is high.

Pre-charge Face

When clock is low, the circuit is in the pre-charge phase. MP1 is turned on and the dynamic node is charged to VDD. In addition, PMOS keeper transistor (MP2) is turned on helping the pre-charge, At the beginning of the pre-charge phase, MN1 is ON, connecting the N-FOOT node to ground. Furthermore, node GMN2 is low and MN2 is OFF. After the delay equals to the delay of the inverters (delay element), MN1 turns off. In this case, the voltage of N-FOOT rises to an intermediate voltage level. The evaluation transistors are sized such that the DC voltage on GMN2 node does not exceed the threshold voltage of MN2 to avoid any possibility of short circuit current in the pre-charge phase. Transistor MN2 is chosen large to help the evaluation of the circuit.

Evaluation Phase

When clock is high, there are two states, standby mode and active mode. In standby mode, at the beginning times of the evaluation phase, At the beginning of the evaluation phase, NMOS footer transistor MN1 is OFF which results in floated node N-FOOT. Therefore, N-FOOT node voltage reaches a DC value. The dynamic node is charge at high voltage level and of the output of the circuit is at low level which turns on the transistor MP3.

If one of the inputs to evaluation devices goes high, As it is shown, the increased voltage on node N-FOOT at the beginning of the evaluation phase turns on transistor MP3. Consequently, node GMN2 is charged to a voltage that is supplied by N-FOOT node voltage. Therefore, GMN2 voltage goes higher than the threshold voltage of MN2 depending on the sizing of the transistors. Then NMOS transistor MN2 turns on at the onset of evaluation phase (while the footer transistor MN1 is OFF), connecting the dynamic node to ground. However the amount of this discharging current through MN2 depends on the sizing of MN2 that has been selected large enough. When the dynamic

node goes low, the output node becomes high, turning on MN3 that leads to OFF MN2. However, the rest of evaluation phase (discharging of the dynamic node) completes through the evaluation network and the footer transistor that is fully on. Here we have more degree of freedom for increasing speed or enhancing noise immunity. For example, for improving speed, upsizing of MP3, MN3, MN2, MN1, evaluation transistors, and MN1 are all options.

5. Simulation result

Circuits are simulated using HSPICE simulator at temperature of 27 degree Celsius in 65 nm technology for bulk CMOS. Channel length and width taken for simulations for Keeper is .25 µm, PMOS 5 µm, NMOS 2.5 µm and load capacitance of 1µf, Supply voltage V_{dd} used is 1V. For the noise–tolerance measurement, noise immunity metric, unity noise gain (UNG). noise pulse width 50 ps (higher than gate delays) are taken and noise-voltages are applied to all inputs.

TABLE 1

Comparison of Power, Propagation delay, Power delay product, UNG and No of transistor for 8 input fan-in gate.

PARAMETERS	Footer less diode	Footed diode	High speed domino	Condit-ional keeper domino	Pro-posed circuit
POWER(µW)	2.87	3.023	456.19	287.9	2.986
NORMALIZED POWER	1	1.05	158.87	100.3	1.040
PRAPOGATION DELAY (ps)	14.1	21.432	11.797	14.31	18.17
NORMALIZED PROPOGATION DELAY	1.19	1.81	1	1.013	1.286
POWER DELAY PRODUCT (aJ)	40.5	64.78	53.81	41.20	54.15
UNG	.298	.327	.2962	.3079	.378
No. Of Transistors	12	13	18	23	17

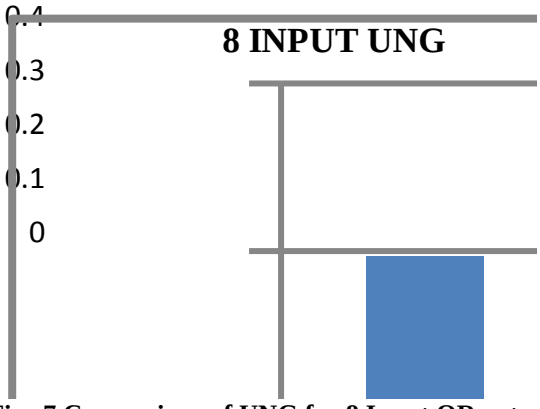

Fig:-7 Comparison of UNG for 8 Input OR gate

6. Conclusion

In this paper a new scheme for the domino logic is proposed which is robust and noise tolerant. The existing and proposed circuit is simulated using HSPICE simulator using 65 nm PTM for bulk CMOS model card at the power supply of 1V for 8 input for Wide fan-in OR gate.

The simulation result shows an improvement in UNG from 1.15 to 1.26 times and exhibits reduced up to 97% low PDP for 8 bit OR gate at the cost of 7% reduction in delay. Proposed scheme when compared with the recent proposals shows high power savings as well as less power-delay product with almost same noise immunity. Furthermore, UNG increases as fan-in increases. The proposed circuit can be used in design of high-speed embedded processors where low power consumption is an essential requirement. The proposed circuit also shows noise efficiency compared to previous work in the literature. The circuit is flexible and quite applicable for large fan-in gates.

10. References

List and number all bibliographical references in 9-point Times, single-spaced, at the end of your paper. When referenced in the text, enclose the citation number in square brackets, for example [1]. Where appropriate, include the name(s) of editors of referenced books.

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