Literature Review on the Power Reduction Techniques and Adders for Approximate Computation

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Abstract

This paper presents literature review on the various techniques involved in attaining power reduction in several computing applications, specifically for digital signal processing. As arithmetic circuits forms the basic functional units in DSP algorithm, the reduction in the complexity of the adder design can bring drastic improvements in the power savings attained. Introduction of designs based on approximate adders provide complexity reduction at transistor level and proved to reduce the switched capacitance, critical path reduction and hence enable voltage scaling provided that low power is attained. Since DSP applications like image compression and video compression are error tolerant, it can be found that even if there are errors in the intermediate outputs it will not form substantial reduction in final output quality.

Index terms *– Approximate adders, low power, DSP algorithm, voltage scaling.*

1. Introduction

In today's electronics industry, one of the main challenges faced is to attain low power designs for the several applications. As power dissipation has become an important issue it has made the way to consider the performance and area so that low power is achieved. The trend for considering low power designs began with a remarkable growth in the areas of personal computing like portable desktops, multimedia devices wireless communications etc., that particularly aim in high speed computations and complex functionality with reduced power consumption. The approximate computing has specification for selecting the hardware for DSP blocks. It has been observed that around 70% of the energy is used in transferring datas and instructions and 6% of energy to perform arithmetic operations. In such a condition approximate arithmetic will not provide much energy benefits when the complete processor is considered. General purpose applications include processors that are programmed to perform the required operations whereas in application specific integrated circuits (ASIC) implementations have error resilient applications like the image and video compression. So it can be stressed on the fact that approximate computing can be performed only on ASIC implementations as it can tolerate errors but general purpose processors cannot be suitable for approximations.

2. Algorithmic Noise Tolerance (ANT) for soft digital signal processing

Concept:

Low energy digital signal processing (DSP) can be obtained by scaling the supply voltage beyond critical voltage for the purpose of matching the critical path delay. Here a scheme called Algorithmic Noise Tolerance (ANT) was introduced that compensated for the degradation in output of system due to error from soft DSP. Soft DSP can be described as a scheme for DSP architecture operating at subcritical voltage and performs error control.

Purpose:

Inorder to enhance performance of filtering algorithm in the presence of soft computation errors can be done by a method called prediction based error control scheme.

Circuit used:

Frequency selective filter

Result:

- 60%-81% reduction in power dissipation
- Maximum of 0.5 dB degradation in output signal to noise ratio (SNRo)

Drawback:

Noise model of deep submicron (DSM) for arithmetic circuits in digital filters were not available.

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3. Approximation circuits and improvisation of speed in processors

Concept:

The main concept that can be discussed here is that by using certain approximation circuits the microprocessor's clock frequency can be increased. The approximation was based on replacing the entire logic function by a simple circuit which have the capability to mimic the function of the main circuit and also provides the predicted results.

Purpose:

Inorder to reduce the delay approximate adders were used in the microprocessors that developed shorter carry chains hence the speed can be increased.

Circuit used:

- Microprocessor and microarchitecture devices
- Adder circuits

Result:

- 50% delay reduced
- 65% accuracy for 32 bit addition was obtained with 4 bit carry and inputs.

Drawback:

Handshaking overhead is caused for the execution completion at each stage.

4. RPR for low power DSP applications

Concept:

The ANT technique was modified to form a novel approach called the reduced precision redundancy (RPR). Low power DSP applications are attained by using RPR where this technique is responsible for producing an output that is correct when compared to original system with errors. For this RPR requires reduced precision replica. The RPR technique is combined with VOS and soft DSP for obtaining the energy savings in the system.

Purpose:

Generate maximum energy savings in different systems with no much loss in signal to noise ratio (SNR).

System used:

- QPSK system
- FFT block in WLAN OFDM system.
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Result:

- 60% energy savings in QPSK system.
- 44% energy savings in WLAN OFDM system.

Drawback:

Presence of errors in the error reduction block and efficient error control scheme is not present.

5. Methodology for synthesizing low power design in fixed point FIR filter

Concept:

Here FIR filter synthesis technique is introduced that exploits the filter coefficients to obtain accurate filter response by voltage scaling. An algorithm called level constrained common sub expression elimination is used here where number of adder levels is constrained for complexity at each coefficient output.

Purpose:

Conventional FIR architectures failed to result the desired filter response during Vdd over scaling. This architecture showed accurate degradation in output response even when the voltage scales down.

Model used:

Filters implemented in the Predictive Technology Model (PTM) model.

Result:

Power savings of 25% - 30%

Drawback:

Complexity in architectural level design

6. Multiplier architecture showing trading accuracy for power

Concept:

In this inaccurate 2x2 multiplier architecture is considered which had tuneable error characteristics. The architectural designs were implemented on image filters and JPEG compression to show 2x- 8x times better signal to noise ratio (SNR). Here non error resilient applications can be shown for multiplier operations using residual adders.

Purpose:

The error based design techniques provide power savings and can be used for critical mode operations.

Circuit used:

2x2 inaccurate multiplier

Result:

Power savings of 31.78%- 45.4% with an average error rate of 1.39% - 3.32%.

Drawback:

Technique to provide maximum power benefit for a given error rate for other arithmetic circuits were not available.

7. Imprecision based adder design for low power DSP applications

Concept:

One of the major requirements of portable multimedia devices is low power consumption. As the multimedia applications are considered, there is no need for correct numerical output since the human eye cannot interpret the final output quality. Taking this into consideration approximate or imprecise fill adder cells are designed with complexity reduction at transistor level. These approximate adders are then applied to the image and video compression algorithms to compare the power savings.

Purpose:

To obtain maximum power savings and reduced area savings.

Circuit used:

- Mirror adder
- DCT architecture

Result:

- 69% of power savings for image compression
- Area reduced from 40.66 μm^2 in conventional MA to 15.56 μm^2 in approximate adder design.

Drawback:

Complexity at the transistor level design is high and need to be reduced to obtain better results.

8. Recommended Solution

As the previous works are considered it can be found that reduced power saving is important criteria for the electronic devices especially for portable multimedia devices are being used in a wide range. By taking this into consideration it is necessary to consider design techniques from the adders which form the basic unit of the building blocks of these devices.

Considering approximation in the adder design has been a great achievement in obtaining low power savings. The conventional mirror adder circuit using CMOS transistors can be overcome by using Complementary Pass transistor Logic (CPL) adders. CPL includes only NMOS pass transistor network for logic operations and the complexity in the logic circuitry can be reduced drastically when compared to that in CMOS adders.

CPL logic style mainly has advantages over area, speed, and power dissipation. Here the CPL offers reduction in parasitic capacitances and thereby improving the performance by increasing the speed. CPL also generates power dissipation around 30% less than CMOS circuits. The tabular column below shows the results obtained for power savings for previous works.

S. No.	PREVIOUS WORK	POWER SAVING (%)
1	ALGORTHMIC NOISE TOLERANCE FOR SOFT DSP	60-80%
2	APPROXIMATION CIRCUITS&IMPROVISATION OF SPEED IN PROCESSORS	40%
3	RPR FOR LOW POWER DSP APPLICATIONS	60%-QPSK system. 44%- WLAN OFDM system.
4	METHODOLOGY FOR SYNTHESIZING LOW POWER DESIGN IN FIXED POINT FIR FILTER	25-30%
5	MULTIPLIER ARCHITECTURE SHOWING TRADING ACCURACY FOR POWER	31.7- 45.4%
6	IMPRECISION BASED ADDER DESIGN FOR LOW POWER DSP APPLICATIONS	69%

Table1. Power savings obtained for previous works

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