Low Power Pulse Triggered Flip-Flop using Signal Feed- Through Scheme

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***Abstract* — The flip-flop is the one of the major component in VLSI low power circuits. The proposed method is pulse-triggered flip-flop (PT-FF) design based on a signal feed through scheme. Pass-transistor logic based NAND gate is designed for pulse generation which reduces circuit complexity and enhances for faster discharge. The transistor sizes of the delay inverter and pulse generation circuit are reduced for power saving. Simulation is performed for various pulse triggered flip-flop to demonstrate the effectiveness of our proposed system using Micro wind 120-nm technology, analysis of power reduction is simulated by using micro wind tool.**

Keywords* — *Flip-Flop, Pulse Triggered, Low Power

I INTRODUCTION

Flip-flops (FFS) are the fundamental storage parts used extensively altogether sorts of digital styles. In particular, digital styles today typically adopt intensive pipelining techniques and use several FF-rich modules. It is also estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is as high as 20%-45% of the total system power [1]. Pulse triggered FF (P-FF) has been thought of a preferred various to the traditional master-slave based FF with in the applications of high speed operations [2]-[5].

Flip-flop can be simple (transparent or opaque) or clocked (synchronous or edge-triggered). Although the term flip-flop has historically referred generically to both simple and clocked circuits, in modern usage it is common to reserve the term flip-flop exclusively for discussing clocked circuits. The simple ones are commonly called latches using this terminology; a latch is level- sensitive, whereas a flip-flop is edge-sensitive. When a latch is enabled it becomes transparent, a flip-flop's output only changes on a single type (positive or negative going) of clock edge.

If the power consumed by the flip-flop is reduced then there will be reduction on total power consumption of the clock system. Pulse triggered flip-flop (PT-FF) is considered as an alternative for the conventional transmission gate (TG) based or master-slave based edge triggered flip-flops. A PFF consists of single latch as compared with two latches in the conventional transmission gate (TG). This gives better power performance and speed. A PFF consists of a latch and pulse generator. If the width of the triggered pulse is narrow then the latch acts like an edge triggered flip-flop, these are of two types: implicit type and explicit type. In an implicit type, the clock generation is built in logic with latch. In an explicit type, the lock generation and latch are separate.

In this brief, are present a novel low -power P-FF design based on a signal feed-through scheme. Observing the delay discrepancy in latching data "1 or 0", the design manages to shorten the longer delay by feeding the input signal directly to an internal node of the latch design to speed up the data transition. This Method implemented by introducing a simple
pass transistor for extra signal driving

II. CONCEPT OF EXISTING SYSTEM

Here we analysis problems on previously designed typical low power flip-flops with comparison to a conventional flip-flop as in Figure 1 shows a classic explicit P FF design, named data closed to output (EP-DCO). It contains a NAND logic based pulse generator and a semi dynamic True Signal Phase Lock (TSPC) structured latch design. In this PFF design, inverters I3 and I4 are used to latch data, and inverter I1 and I2 are used to hold the internal node x.

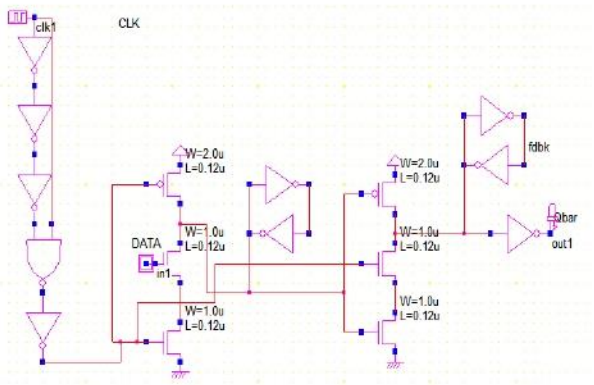

Fig. 1. Conventional explicit pulse data closed-to output flip-flop (EP-DCO)

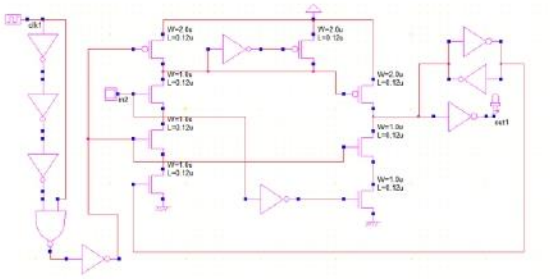

Fig. 2. Conditional discharge flip-flop (CD-FF).

The pulse width is determined by the delay of three inverters. This design suffers from a serious drawback, the internal node x is discharged on every rising edge of the clock in spite of the presence of a static input "1". This gives rise to large switching power dissipation.

Figure 2 shows a circuit of conditional- discharging flip-flop (CD-FF) [4]. An extra NMOS transistor MN3 controlled by the output signal Q-feedback. So that no discharge occurs if the input data remains "1". In addition the keeper logic for the internal node x is simplified and consists of an inverter plus a pull-up PMOS transistor only.

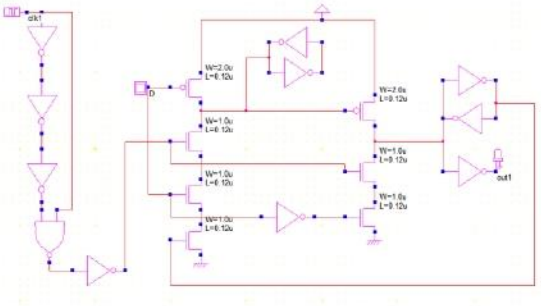

Fig.3. Static CD flip-flop

Figure 3 shows a similar P FF design using a static conditional discharge technique (SCD FF).The CD FF design in using a static latch structure. Thus node x from periodical pre charges. It exhibits a longer data o Q (D-to -Q) delay than the CD FF design. To overcome this delay for better speed performance, a powerful pull-down circuitry is needed, which causes extra layout area and power consumption.

The simulation output of EP-DCO flip-flop is shown below

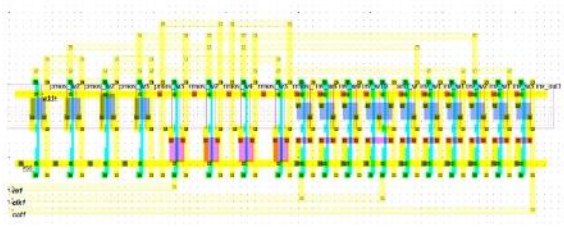

Fig.4. EP-DCO FF layout using in micro wind tool

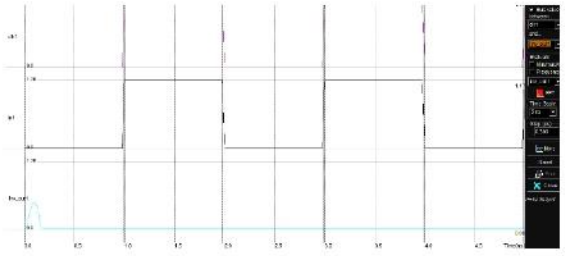

Fig.5. Power Calculation in EP-DCO flip-flop

The simulation output of conditional discharging flip-flop is shown below

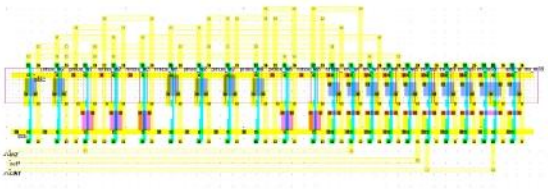

Fig.6. CD FF layout using in micro wind tool

III. DESIGN APPROACH

The power of the FF is mostly dissipated in the operation of clock-related NMOS transistors, and reduced the number of transistor and to reduce load capacitance in internal nodes, also reduced discharging path.

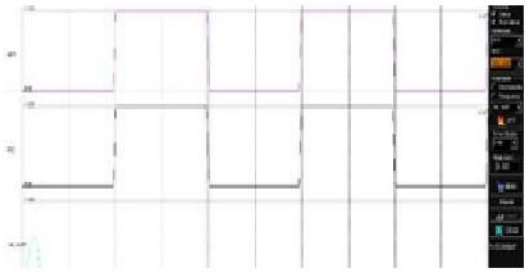

Fig.7. Power Calculation in CD Flip-flop

IV. CONCEPT OF PROPOSED FLIP-FLOP TRUE SINGLE - PHASE CLOCKING

Flip-flop used for the high speed digital design,short latency, is to have a simple and signal feed through scheme. A family of static and dynamic latches with such characteristics is true single- phase clocking(TSPC) [4]. TSPC latches can be combined in several different ways to implement edge triggered flip-flops. Advantages of TSPC flip-flop is small atency. For a sufficiently narrow pulse width on, the latch behaves as an edge-triggered flip-flop. When clock clk is low, the flip-flop is in the precharge phase. Node x is precharged to the level of the power supply, and node Q holds

its previous value. On the rising edge of the clock, the flip-floop enters the evaluation phase. In the first period, the pulse is active and circuit acts as the sampling mode. The internal node x is discharged, the output value of Q is precharged. Aplply Next clock cycle, the pulse is inactive. The ssampling of D is disabled,so X and Q will retain the values they acquired during the sampling period. Any chances at D after the sampling period will have no effect on Q.

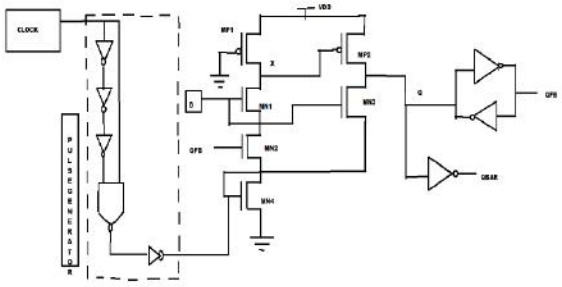

Fig. 8. Pulse triggered flip-flop(P-FF)

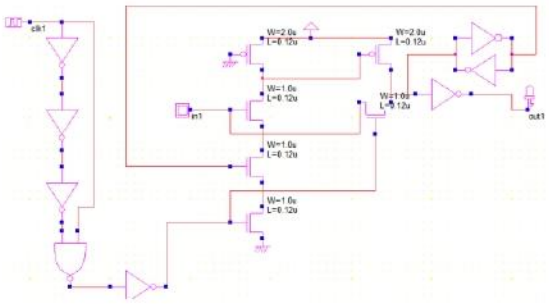

Fig. 9. Schematic diagram of proposed FF.

If the pulse generated externally, using a pulse generator, the circuit suffer from the charge sharing. To generate the pulse locally, in fig 4. So avoiding charge sharing, this local pulse generation allows better control of the pulse width, so that a very narrow effective pulse can be produced, an reduce potential race-through problems and also improve the noise sensitivity of the circuit.

A. Pulse Triggered Flip-Flop Design

The proposed design adopts a signal feed- through technique to improve this delay. The design also employs a static latch structure and a conditional discharge scheme to avoided switching at an internal node. This system solving long discharging path problem in conventional explicit type pulse-triggered flip-flop. When a clock pulse arrives, there is no data transition occurs. The input data and node Q at same level. Low power P-FF design based on a signal feed -through scheme. The design manages to shorten the delay by feeding the input signal directly to an internal node of the latch design to speed up the data transition. When combined with the pulse generation circuitry, it forms a new P-FF design with enhanced speed and power delay product (PDP) performances.

Signal feed-through scheme means, apply the data 1 and 0, the design manages to shorten the longer delay by feeding the input signal directly to an internal node of the latch design. When there is a data transition occurs (1 to 0) the delay will be reduced. The input signal is applied to the internal node(x), the data transition increase the speed. A low power flip-flop design featuring an explicit type pulse-triggered structure and a modified true single phase clock latch based on a signal feed-through scheme is presented. The proposed design successfully solves the long discharging path problem in conventional explicit type Pulse- Triggered FF (P-FF) designs and achieves better speed and power performance.

The design of pulse- triggered flip-flop, these are of two types: implicit type and explicit type. The clock generation is built in logic with latch. In an explicit type, the clock generation and latch are separate. Implicit type pulse triggered flip-flop is considered as more power efficient than explicit type pulse triggered.

B. The Principle of Proposed Pulse Triggered FF Design is explained as Follows

- When the clock signal is "low", input data is "0", output signal Q is "0" and control signal Q-Feedback is "1".
- When the clock signal is "low", input data is "0 to 1", as the control signal Q feedback is "1" at the previous state.
- When the clock signal is low to high, input data is 0 to 1, as a normal state transformation Occurs, the second and third transistor ON Condition.
- When the clock signal is high to low, input data is 1 to 0, the clock generator is off, output signal Q maintains the captured value of the previous state.

V. SIMULATION RESULT

The proposed design adopts a signal feed through technique to improve this delay. Similar to the SCDFF design, the proposed design also employs a static latch structure and a conditional discharge scheme to avoid switching at an internal node. However, there are three major differences that TSPC latch structure and make the proposed design distinct from the previous one.

First, a weak pull-up PMOS transistor MP1 with gate connected to the ground is used in the first stage of the TSPC latch. This gives rise to a pseudo-NMOS logic style design, and the charge keeper circuit for the internal node x can be saved. In addition to the circuit simplicity. This approach also reduces the load capacitance of node x.

Second, a pass transistor MN_X controlled by the pulse clock is included so that input data can drive node Q of the latch directly (signal feed-through scheme). The pull-up transistor MP_2 at the second stage inverter of the TSPC latch, this extra auxiliary signal driving from the input source to node Q and shorten the data transition delay occurs. Third, the pull-down network of the second stage inverter is completely removed. The newly employed pass transistor MN_x provides a discharging path. The MN_x is thus two fold, Provides extra

driving to node Q during 0 to 1 data transitions, and discharging node Q during 1 to 0 data transitions. Compared with the latch structure used in SCDFF design, the circuit savings of the proposed design includes a charge keeper, a pull-down network and a control inverter. The only extra component introduced is an NMOS pass transistor to support signal feed through scheme. This scheme actually improves the 0 to 1 delay and thus reduces the disparity between the rise time and fall time delays.

In comparison with other P-FF designs such as EP-DCO, CD FF, and SCD FF, the proposed design shows the most balanced delay behaviors.

A. Proposed Method

The simulation Output of pulse triggered flip-flop is shown below

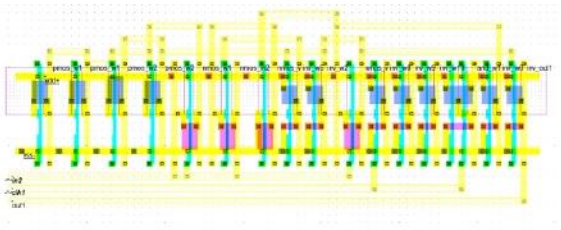

Fig.10. P-FF layout using in micro wind tool

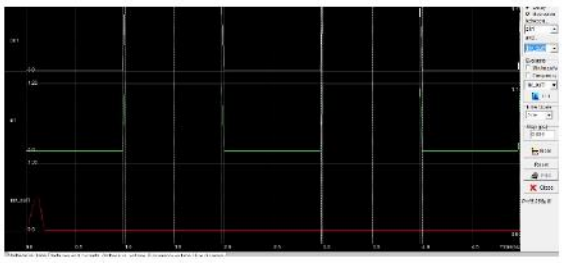

Fig.11. Power Calculation in P-FF

TABLE 1
Comparison of flip-flops

Flip-flop designs	Layout width (µw)	Number of transistor	Power (µw)
CD FF	28	30	15.548
SCD FF	26	31	19.185
EP-DCO FF	23	28	19.392
P FF	19	24	15.355

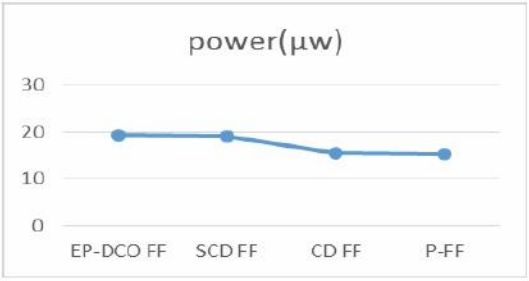

Fig.12. Power graph

VII. CONCLUSION

In this paper, novel low power flip-flops have been introduced. They achieve statistical power reduction by eliminating internal redundant transitions. They have negative setup time and thus provide small data to output latency. A novel low power pulse triggered FF design by employing new design measures. This method is successfully reduces the number of transistor stacked along the discharging path by incorporating a PFF based NAND logic. The simulation are performed in 120 nm technology, using power supply of 1v and clock frequency 500MHZ.

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