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Low Power Ram Testing using Bist in VHDL

Ritu Singh Thakur
M.Tech Scholor, ECE dept.
Dr. C. V. Raman University
Bilaspur, India

Akanksha Awasthi
Asst. Prof. ECE dept.
Dr. C. V. Raman University
Bilaspur, India

***Abstract*—Very large Scale Integration (VLSI) has created a dramatic impact on the growth of microcircuit technology. It has not only reduced the dimensions and also the value, but conjointly accumulated the complexes of the circuits. The improvements have resulted in important performance/ cost benefits in VLSI systems. Transparent BIST schemes for RAM modules assure the preservation of memory contents throughout –periodic testing. As the speed power area are the constraints of memory testing. In our proposed project main target of our project is to reduce power consumption without affecting fault coverage and reduce switching transition**

Keywords—BIST, VHDL, RAM, MISR.

I. INTRODUCTION

Logic built-in self-test (L-BIST) is an outline for testability (DFT) technique during which some of a circuit on a chip, board, or system is used to examine the digital logic circuit itself. Using logic BIST, circuits that generate test patterns and analyze the output responses of the useful electronic equipment of area unit embedded in the chip or elsewhere on constant board wherever the chip resides [1]. There are 2 sorts of memory for test at methods: electrical which is technology-dependent and useful which is technology-independent. Electrical memory testing consists of parametric testing, which includes testing DC and AC parameters, IDDQ and dynamic testing for recovery, retention and imbalance faults [2]. RAM modules are tested each once producing and periodicals in the field. During testing, some tests are applied to check that the RAM operates ordinarily [3]. With a built-in take a look at system positioned within the circuit, the analysis of every single a section of the circuit might become a simple task as a result of the number and price of the testing square measure curtail. This BIST technology is capable of saving the time and cost of maintenance that conjointly permit on-line designation, which will agitate the even bigger advance of embedded systems in future [4].
signature Symmetric clear intrinsic self-test (BIST) schemes skip the prediction section needed in ancient clear BIST, achieving a considerable reduction in take a look at the time.
The objective of this project is to develop a BIST for RAM by using VHSIC Hardware Description Language (VHDL).

II. LITERATURE SURVEY

In the year 1995 Tsuneo Matsumura et.all described novel algorithmic take a look at patterns appropriate for embedded multi-port RAM with BIST (built-in self-test) electronic equipment that realizes, for all ports. The functional memory test and the browse write disturb test at the same time whereas facultative memory operation. It will be shown that these patterns also can find BIST malfunctions despite the fact that they need regarding a similar pattern length because the normal purposeful test patterns for single-port RAMs.

In the year 2002, Jen-Ching Yeh et.all has implemented Bit-oriented and word-oriented March-like algorithms the March ft algorithms—are planned, which cowl all types of disturb faults outlined within the IEEE 1005 normal. The inherent regularity of March-like tests makes them especially appropriate for BIST and fault designation. We have enforced the BIST circuit for various flash recollections. In addition, a flash memory simulator is designed to facilitate the analysis and generation of the test the algorithms.

In the year 2002 Andreas Steininger proposed, however, This intrinsic Self-Test (BIST) approach offered not solely economic edges, but place along fascinating technical opportunities at stratified arrival and apply of check logic throughout the applying of the circuit. It was proposed technique entirely.

In the year 2003 Theo J. Powell et.all IEEE implement BIST, MUX logic is needed to permit BIST controller to work the memory. Also, to simplify ATPG effort for logic around recollections, it is desirable to feature bypass scan to manage memory outputs and observe memory inputs. Some TI memories have constitutional embedded MUXes and bypass scan already. The tool can acknowledge the existing MUXes and bypass scan logic and hook the BIST controller to the RAM properly while not duplicating BIST collar logic.

in the year, 2005 Srinivas Garimella (FPGA) independent BIST model is developed victimization VHDL. The parameterized VHDL model has been synthesized and used to test various sizes and varieties of embedded RAMS in SoCs and FPGAs.'

In the year 2011 V. SRIDHAR et.all has implemented the BISR. Built-in self-repair (BISR) technique has been wide used to repair embedded random access reminiscences (RAMs). If each serviceable RAM uses one self-contained BISR circuit (Dedicated BISR scheme), then the area worth of BISR circuits in associate degree passing SOC becomes high. This results in the converse effect on the yield of RAMs. This paper presents a reconfigurable BISR scheme for repairing RAMs with whole totally different sizes and redundancy organizations. An economical redundancy analysis formula is projected to apportion redundancies of defective RAM as. In the BISR, a reconfigurable built-in redundancy analysis circuit is designed to perform the redundancy formula for various RAMs. The BISR structure has been synthesized and found that the globe cost compared with the Dedicated BISR structure, is very little. The problem is with the globe.

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In the year 2011 M. H. Hussein, This has emphasized primarily on writing the analysis. ModelSim-Altera 6.4a is the software that is employed to BIST for Random access Memory (RAM) vogue, for every single module.Three things to be thought of for RAM, Test Pattern Generator (TPG), Output Response Analysis (ORA) and RAM. The output of a counter which is a quite TPG is analyzed to provide a pattern for the March check formula. At the mean time, the ORA compare the output from the decoder and the RAM output itself. The output of ORA, the comparator, is a unit which is able to show the circuit (RAM) is fault free or not It's biting size are often inflated.

In the year 2014 U. Siva Nagaraju et.all implemented identification and Fault Tolerance for Embedded BIST Rams. In this because of poor controllability and observability of address, control, and data lines embedded RAMs are terribly very hard to check. The memory cell in embedded RAM has various type of faults stuck-at faults, coupling faults, data retention faults, and bridging faults. To address this concern, we developed a technique that's used to note the fault, isolate the location of the fault and might predict the remaining helpful performance of embedded BIST RAMs for on- chip memory solely.

In the year 2014 Mrs. S. Enamel et.all Transparent inbuilt Self-Test for word-oriented RAMs produces take a look at knowledge with a high degree of symmetry. The transparent test approach is applied to the idle state of systems. Reducing the test time is very important for avoiding the interrupt of testing. Transparent word oriented March tests so. live directly obtained by repeated execution the corresponding bit oriented March test on equally of the word. In this system RAMs, an area of varied sizes is employed and every has utterly completely different breadth structure.

III-PROPOSED WORK

A. General BIST architecture

BIST technique can be categorized into general architecture and often classified to be centralized or distributed. These two basic BIST architectures are illustrated in Fig. 1.

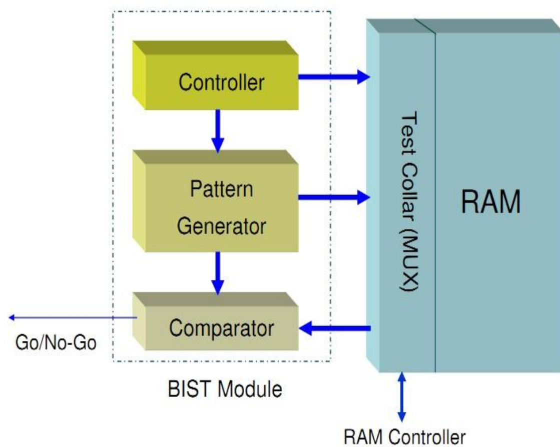

Figure 1.

B. Block diagram for BIST.

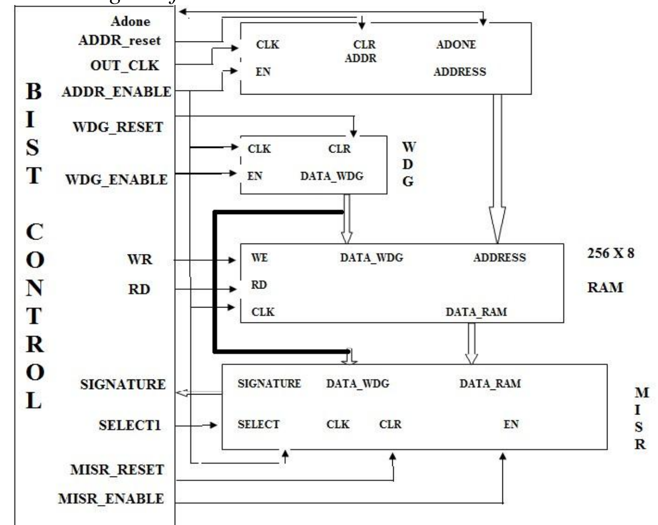

Figure. 2

B.1. Write data Generation: - There are various methods and approaches have been used to generate test patterns during BIST, here we have used **LFSR-** Linear Feedback Shift Register from figure 2.

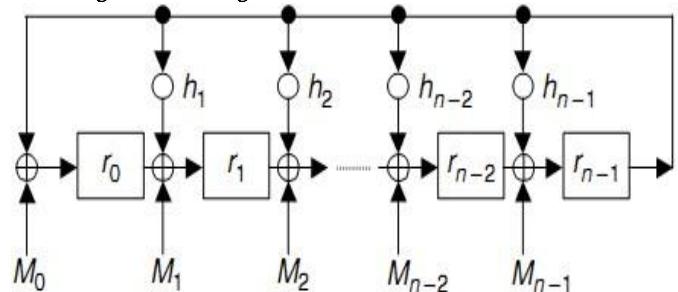

Figure 3. Modular LFSR

B.2 Circuit under Test (CUT): **-** For testing purpose, we have used RAM circuit under test shown in Figure. CUT is the system which is to be tested after its manufacturing It is the circuit of the IC that is going to be checked for any faults Any digital design represented in VHDL is used as a CUT. From fig. 2.

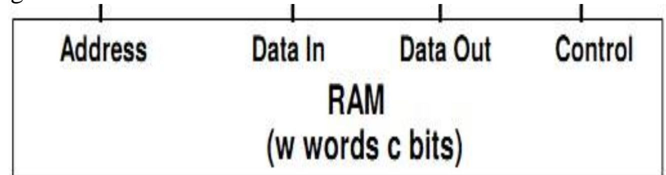

Figure 4. Basic RAM

B.3 BIST Controller: - BIST has a controller, which coordinates the operations of different blocks of BIST, based on the test mode inputs to the controller, the system operates in both the normal mode or the test mode. When the TM is 1, the system enters the test mode; it offers to enable signal to the LFSR that generates the patterns and then it offers to enable the signal to MISR for the compression of patterns from the RAM. It is the controller which decides for the way several cycles modify ought to be created one supported the length of the scan chains and therefore the input-output size of the RAM, from figure 2.

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B.4 Multiple Input Shift register:-

During BIST, for every test pattern that's being generated, the CUT produces a set of output values. To ensure the chip is fault free, every output values from the CUT for every test pattern can have to be compelled to compare with the proper output values obtained from the simulations. This is a tedious and time-consuming method. Thus, it is necessary to cut back the big of circuit responses to a manageable size will which will that be either stored on the chip or can simply compare with the golden response values. For example, a BIST pattern generator in a chip can turn out one million check pattern. If at the end of the BIST method the chip has a total of 100 primary outputs (PI), it will generate a complete of one million output values or 1000000 x100 = 100 million bits of output values. With such a huge quantity of knowledge, it is very pricey and virtually not possible to store within the storage or memory within a chip. There are many approaches and methodology will be used for response compaction, such as transition count response compaction, LFSR for response compaction, Modular LFSR response compaction, single-input signature register (SISR) and also MISR which is multiple input signature register. In this project, multiple input signature register as shown in Figure-2 will be used as response compactor

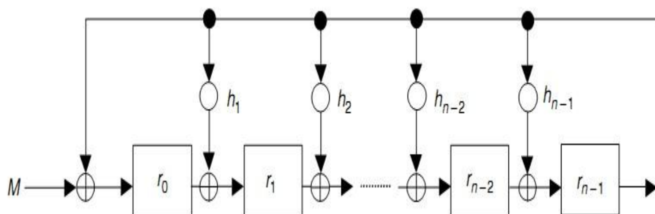

Figure-5 an n-stage multiple-input signature register (MISR)

IV- SIMULATION & ANALYSIS REPORT

1. BIST Controller:-

By using the BIST controller we run write data generation, the circuit under test, and multiple input shift register. The simulation result is shown below.

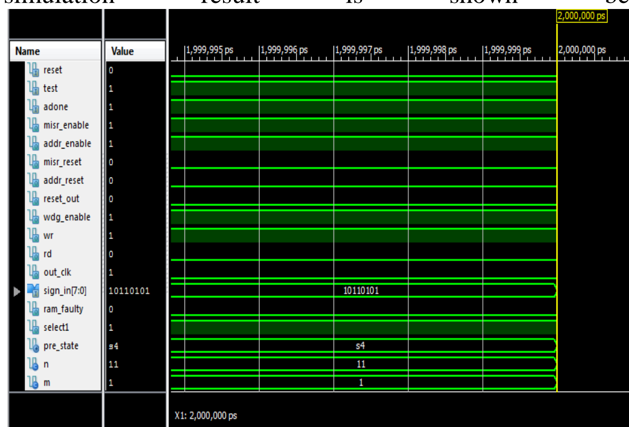

Figure-6

This simulation takes 0.167ns time delay to give output. The Power consumed in this circuit is 32mW.

2. Multiple Input Shift Register: -

In this block we minimize our test pattern response. Because writing information generation offers a lot of data patterns once, minimizing them by victimization Multiple input shift register. It gives a signature pattern that stores in read-only memory. We can do a comparison with this to seek out whether the RAM is faulty or not. Simulation process shows below that offers the range of the test pattern. Delay in the circuit is 0.165ns. The power consumed within the circuit is 32mW.

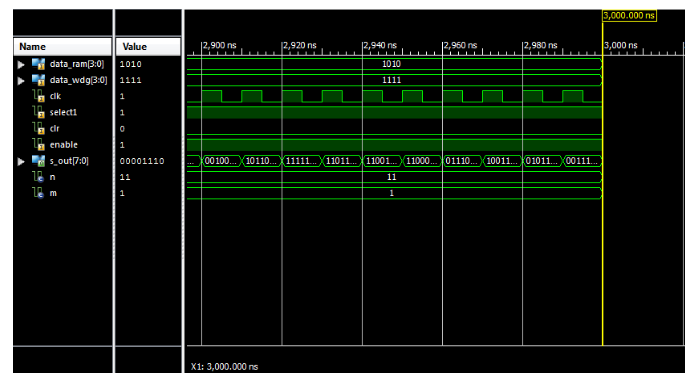

Figure-7

3-RAM:-

In this module, we offer input at some address of RAM & check that same output at an equivalent address show that we will make sure that the RAM is functioning properly and once we call it within the test bench it works properly.

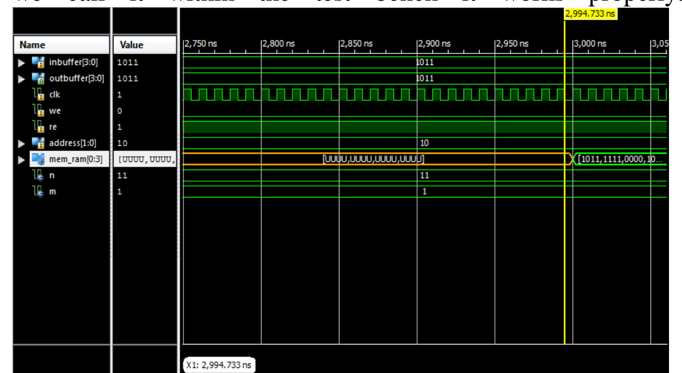

Figure-8

On the simulation of above block, the delay within the circuit is found in the synthesis report that's 0.158ns. The power consumed within the circuit is calculated employing a Xilinx Sparten3E spreadsheet that's 31mW.

4-Write Data Generator:-

In this module, we generate test pattern using the data generator which is Module LFSR. We use a Module LFSR because it has a smaller delay than the other test pattern generator. Here we use this block to generate a number of test pattern generator to save in the selected RAM address. After writing the test pattern in the RAM we read it at the same address using the BIST controller here we get the same address which we write in there. We found that our RAM fault free. The simulation result is shown in the figure. 6

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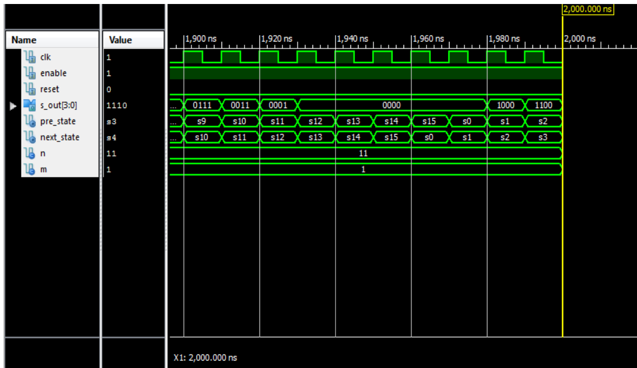
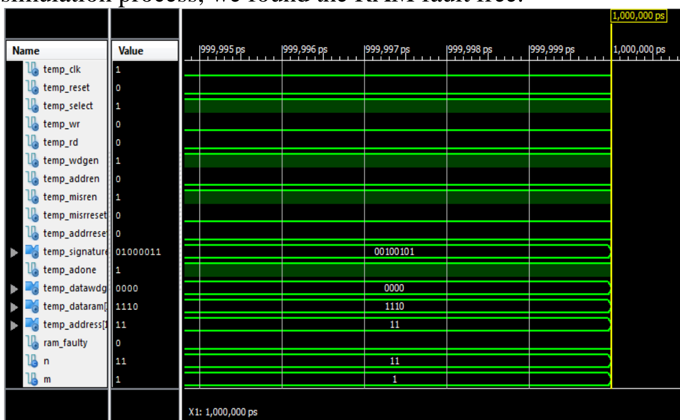


Figure-7

After doing the simulation process, we got a synthesis report in which the delay result is 0.157ns. The Power consumed in the circuit is 31mW.

4-Final Result test bench:-

This block calls all the components which are shown in the BIST architecture block diagram and make them run together this simulation process gives us whether the RAM faulty or not. It depends on the signature value and the output value which comes from the circuit under test here it is RAM. In the simulation process, we found the RAM fault free.



Delay on the simulation of the circuit is **8ns.** Comparable in power consumption in each module

MODULE	PROPOSED WORK DELAY (ns)	PROPOSED WORK POWER(mW)	DEALY	POWER
BIST controller	0.167	323		
MISR	0.165	334		
RAM	0.158	314		
WDG	0.157	325		384 [5]

CONCLUSION

Each & every component is simulated individually; also BIST is simulated using components. All the components and BIST show good results. Waveforms are shown in the report, which shows correct result. As a result testing power consumption is reduced without affecting the fault coverage.

FUTURE WORK

There were a lot of work remain in this field of memory testing like cross coupling fault and many other faults in the memory which should be removed for the betterment of the memory, because in the future memory plays a very important role in the era of the integrated circuits.

REFERENCES

[1] Tsuneo Matsumura "An Efficient Test Method for Embedded Multi-port RAM with BIST Circuitry" 0-8186-7102-5/95 $04.00 *0*1995 IEEE

[2] A. steininger "Using offline and online BIST to improve system dependability" vienna university IEEE 2002

[3] Srinivas Garimella "A System for Automated Built-In Self-Test of Embedded Memory System-on-Chip" IEEE 2005.

[4] Shaik Karimullah G1 Abdul Rahim b C.Ushasree2 " design and verification of online BISTfor different word sizes of memories"

[5] Chih-Sheng Hou, Jin-Fu Li Memory Built-In Self-Repair Planning Framework for RAMs in SoCs IEEE 2011

[6] M.H. Husin, S.Y. Leong, M.F.M. Sabri, R. Nordiana "Built in self test for RAM Using VHDL"2011 IEEE

[7] Chih-Sheng Hou, Jin-Fu Li," A BIST Scheme with the Ability of Diagnostic Data Compression for RAMs" IEEE 2013

[8] Pushpraj Singh Tanwar, Priyanka Shrivastava "VHDL Implementation of Logic BIST (Built In Self Test) Architecture for Multiplier Circuit for High Test Coverage in VLSI Chips."2014 IJARE

[9] Mrs. S. Ellammal M.E1, T.Saranya2 "Transparent Test Scheme in Online BIST For Word-Oriented Memories" 2014 IEEE

[10] V.Kirthi1, Dr.G.Mamatha Samson2,"Design of BIST with Low Power Test Pattern Generator" 2014 IOSR Journal

[11] Nptel.ac.in/courses/106103016/30

[12] M. Abramovici, M. Breuer and A. Friedman, Digital Systems Testing and Testable Design, Piscataway, New Jersey: IEEE Press, 1994.

[13] E. McCluskey, "Built-In Self-Test Techniques," IEEE Design & Test of Computers, Vol. 2, No. 2, pp. 21-28, March 1985.

[14] R. A. Frohwerk, "Signature Analysis: A New Digital Field Service Method," Hewlett-Packard Journal, vol. 28, no. 9, pp. 2–8, May 1977

[15] ShaikKarimullah G1, Abdul Rahim b C. Ushasree2." Design and verification of online BIST for Different word sizes of memories."

[16] Mrs. S. Ellammal M.E1, T.Saranya2" Transparent Test Scheme in Online BIST for Word-Oriented Memories" ISSN 2278 – 0882

[17] M.H. Husin, S.Y. Leong, M.F.M. Sabri, R. Nordiana "Built in self test for RAM Using VHDL" 2012 IEEE Colloquium on Humanities, Science & Engineering Research (CHUSER 2012), December 3-4, 2012,

[18] Andreas Steininger" Testing and Built-in Self-Test" Institute für Technische Informatik, Vienna University of Technology A-1040 Vienna / Austria, Treitlstrasse 3

[19] M.RAJENDRA PRASAD" Built-in self-repair (BISR) technique widely Used to repair embedded random access memories (RAMs)" International Journal of Computer Science Engineering (IJCSE)

[20] Version 2 IEEE IIT, Kharagpur" Built-In-Self-Test (BIST) for Embedded Systems"

[21] U.Siva Nagaraju, Dr.A.sahaya Anselin Nisha Diagnosis and Fault Tolerance for Embedded Bist RAM International Journal of Scientific Research, Vol.III, and Issue. IV Apr 2014

[22] Amit Bhanwal, Mayank Kumar, Yogendera Kumar," FPGA based Design of Low Power Reconfigurable Router for Network on Chip (NoC)", ISBN: 978-1-4799-8890 ©2015 IEEE, International Conference on Computing, Communication Automation (ICCCA2015).

[23] Madhuraj, Prince Kumar Pandey, Mayank kumar,"FPGA Implementation of Convolution using Wallace Tree Multiplier," International Journal of Engineering Research & Technology (IJERT) ISSN: 2278-0181 IJERTV3IS061634, Vol. 3 Issue 6, June – 2014.

[24] Mayank Kumar, Mharban singh, Rajiv Kapoor,"Area & Dynamic Power Optimization of CMOS 1-Bit Full Adder Using Genetic Algorithm," International Journal of Engineering Research & Technology (IJERT) ISSN: 2278-0181 IJERTV3IS061634, Vol. 3 Issue 5, may 2014.

(This work is licensed under a Creative Commons Attribution 4.0 International License.)

[25] Akash Kumar, Mayank Kumar, Varun Kumar, Sushant Shama4." Design of a Single Precision Floating Point Unit in Verilog," IJSRD - International Journal for Scientific Research & Development| Vol. 2, Issue 03, 2014 | ISSN (online): 2321-0613.

[26] Sony Rama, Kishore Kumar and P.Rajesh Kumar . Sony Comp. Sci. & Engg. Elixir ISSN: 2229-712x . 41 (2011) 5579

[27] Chih-Sheng Hou, Jin-Fu Li, Member, IEEE, and Tsu-Wei Tseng IEEE transactions on computer-aided . Design of integrated circuits and systems, vol. 30, no. 11, November 2011

[28] K. Zarrineh and S.J. Upadhyaya, "Programmable memory BIST and a new synthesis framework," in Proc. Fault-Tolerant Computing, 1999, pp. 352-355.

[29] B. H. Fang and N. Nicolici, "Power-constrained embedded memory BIST architecture," in Proc. Defect & Fault Tolerance in VLSI Systems, 2003, pp. 451-458.

[30] F. Karimi and F. Lombardi, "Parallel testing of multi-port static random access memories for BIST," in Proc. Defect and Fault Tolerance in VLSI Systems, 2001, pp. 271-279.

[31] T.J. Bergfeld, D. Niggemeyer, and E.M. Rudnick, "Diagnostic testing of embedded memories using BIST," in Proc. Design, Automation and Test in Europe, 2000, pp. 305-309.

[32] D.C. Huang and W.B. Jone, "An efficient parallel transparent diagnostic BIST," in Proc. of Asian Test Symposium, 2000, pp. 299-303.

[33] http://www.micron.com/

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