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Low Power Single Edge Triggered D Flip Flop Based Shift Registers Using 32nm Technology

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Abstract

In this paper, analysis of average power, delay and power delay product is done for various shift registers(SISO, SIPO, PISO and PIPO)using 32nm technology. Low power flip-flops are crucial for the design of low-power digital systems. As Metal Oxide Semiconductor Field Effect Transistor (MOSFET) devices are scaled down to nanometer ranges, Complementary MOS (CMOS) circuit's total Power consumption has a new definition. Due to integration of millions of components and shrinking process technology, nowadays leakage power tends to play a major role in total power consumption. In this paper, the shift registers are designed using 32nm technology with 1GHz and 2GHz frequencies and their performance are analysed.

Keywords *--- CMOS, MOSFET, D Flip Flop, Shift Registers, Single Edge Triggered flip flop, Power Consumption, Delay, Power Delay Product.*

1. Introduction

The development of microelectronics spans a time which is even lesser than the average life expectancy of a human, and yet it has seen as many as four generations. Early 60's saw the low density fabrication processes classified under small scale integration (SSI) in which transistor count was limited to about 10. This rapidly gave way to medium scale integration in the late 60's when around 100 transistors could be placed on a single chip[16].The system on chip (SoC) design will integrate hundreds of millions of transistors on one chip, whereas packaging and cooling only have a limited ability to remove the excess heat [2]. So large amount of heat should not be dissipated.

Thus low power design is the need of today's integrated systems. The low power design is also needed for the applications operated by batteries such as pocket calculators, wrist watches, mobile phones, laptops etc.

It is important to prolong the battery life as much as possible. Flip flops are the basic storage elements used extensively in all kinds of digital designs. As the feature size of CMOS technology process shrinks according to Moore's Law, designers are able to integrate more transistors onto the same die. The more transistors there are the more switching and the more power dissipated in the form of heat or radiation. Heat is one of the most important packaging challenges in this era; it is one of the main drivers of low power design methodologies and practices. Another mover of low power research is the reliability of the integrated circuit. More switching implies higher average current is flowing and therefore the probability of reliability issues occurring rises. The most important prime mover of low power research and design is our convergence to a mobile society. We are moving from laptops to tablets and smaller computing systems. With this profound trend continuing, and without a matching trend in battery life expectancy, the more low power issues will have to be addressed. This entails that low power tools and methodologies have to be developed and adhered to. The current trends will eventually mandate low power design automation on a very large scale to match the trends of power consumption of today's integrated chips.[10] The 32 nanometer (32 nm) node is the step following the 45 nanometer process in CMOS semiconductor device fabrication. Intel and AMD both produced commercial microchips using the 32 nanometer process in the early 2010s. IBM and the Common Platform also developed a 32 nm high-k metal gate process. Intel began selling its 32 nm processors as Core i3, Core i5, and the dual-core mobile Core i7. In this paper the background information about flip-flop based shift registers design and its characteristics are analysed.

2. Single Edge Triggered D-Flip Flop

The Low Power SET D-flip flop is shown in figure 1.This flip-flop is basically a Master Slave flip flop structure and it consists of two data paths. Basically, n-type pass transistors give weak high but in figure 1, the n-type pass transistors are followed by an inverter, which results in strong high. Thus the low power SET D-Flip Flop in figure 1 is free from threshold voltage loss problem of pass transistors. Thus the low power Single Edge Triggered D-Flip-Flop has become more efficient in terms of area, power and speed which claim for better performance than conventional designs.

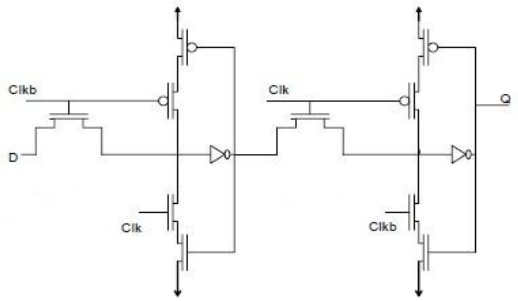

FIG.1 LOW POWER SET D FLIP FLOP[1]

3. Shift Registers

Shift registers are a type of sequential logic circuit, mainly for storage of digital data. They are a group of flip-flops connected in a chain so that the output from one flip-flop becomes the input of the next flip-flop. Most of the registers possess no characteristic internal sequence of states. All flip-flop is driven by a common clock. There are different kinds of shift registers.

* Serial in serial out shift register.

*Serial in parallel out shift register.
*Parallel in parallel out shift register.
*Parallel in serial out shift register.

The storage capacity of a register is the total number of bits (1 or 0) of digital data it can retain. Each stage (flip flop) in a shift register represents one bit of storage capacity. Therefore the number of stages in a register determines its storage capacity.

3.1 Serial in Serial out Shift Register

The serial in/serial out shift register accepts data serially – that is, one bit at a time on a single line. It produces the stored information on its output also in serial form. And the basic serial in and serial out shift register is show in fig 2.
The data string is presented at 'din', and is shifted right one stage each time 'data advance' is brought high. At each advance, the bit on the far left (i.e. 'Din') is shifted into the first flip-flop's output. The bit on the far right (i.e. 'Dout') is shifted out and lost. The data are stored after each flip-flop on the 'q' output, so there are four storage 'slots' available in this arrangement, hence it is a 4-bit register.

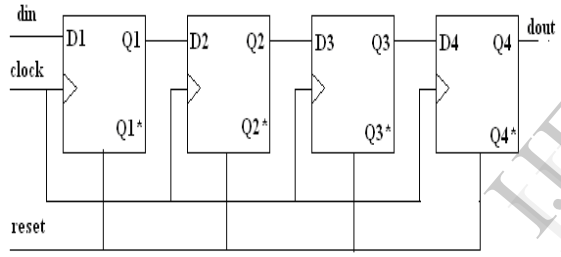

FIG 2: SERIAL IN-SERIAL OUT SHIFT REGISTER

3.2 Serial in Parallel out Shift Register

This configuration allows conversion from serial to parallel format. Data is input serially, as described in the siso section above. Once the data has been input, it may be either read off at each output simultaneously, or it can be shifted out and replaced. Serial in parallel out diagram is shown in fig 3.

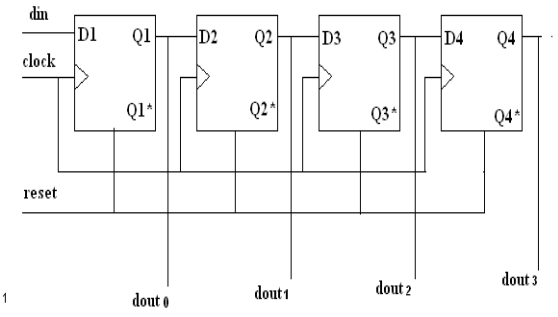

FIG 3: SERIAL IN-PARALLEL OUT SHIFT REGISTER

3.3 Parallel in Serial out Shift Register

This configuration has the data input on lines d1 through d4 in parallel format. To write the data to the register, the write/shift control line must be held low. To shift the data, the w/s control line is brought high and the registers are clocked. The arrangement now acts as a piso shift register, with d1 as the data input. However, as long as the number of clock cycles is not more than the length of the data-string, the data output, q, will be the parallel data read off in order. And the parallel in-serial out is shown in fig 4.

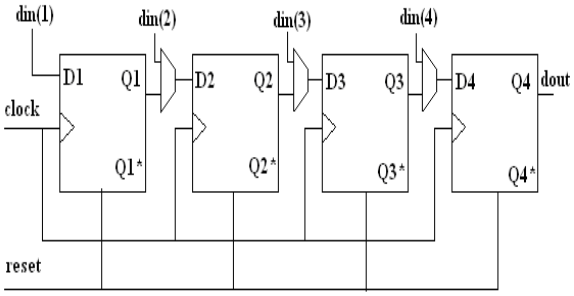

FIG 4: PARALLEL IN SERIAL OUT SHIFT REGISTER

3.4 Parallel in Parallel out Shift Register

For parallel in - parallel out shift registers, all data bits appear on the parallel outputs immediately following the simultaneous entry of the data bits. The following circuit is a four-bit parallel in - parallel out shift register constructed by d flip-flops and shown in fig 5.

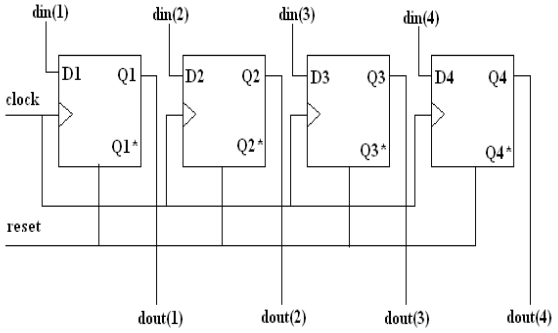

FIG 5: PARALLEL IN PARALLEL OUT SHIFT REGISTER

4.Simulation Results

To evaluate the performance, shift registers discussed in this paper are designed using 32-nm CMOS technology. All simulations are carried out using HSPICE simulation tool at nominal conditions with 1GHz frequency range. The simulated waveform of the Low Power SET flip-flop based shift registers is shown in Fig.6,7,8 & 9.

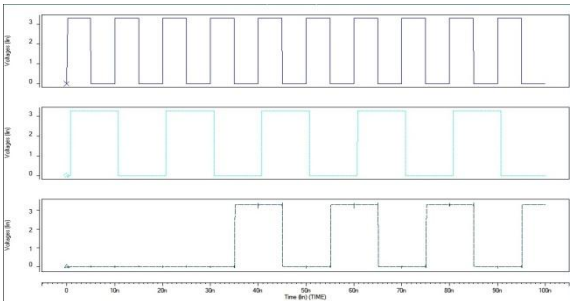

FIG.6 :OUTPUT WAVEFORM FOR SISO

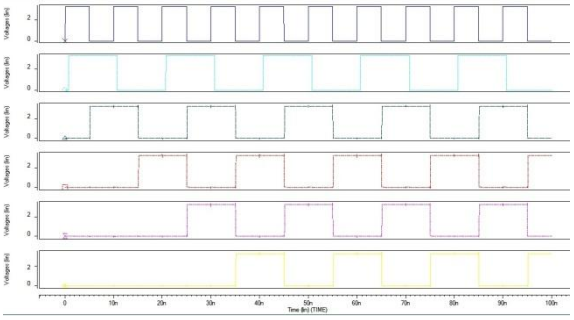

FIG.7 :OUTPUT WAVEFORM FOR SIPO

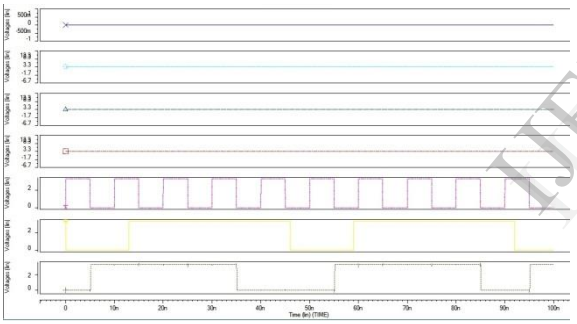

FIG.8 :OUTPUT WAVEFORM FOR PISO

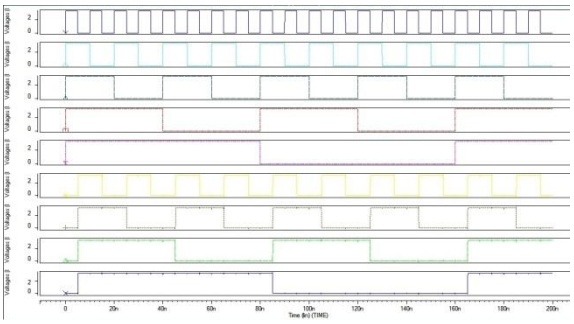

FIG.9 :OUTPUT WAVEFORM FOR PIPO

5.Performance Analysis

The performance of the shift registers is evaluated by comparing the average power, delay and power delay product (PDP). In general, a PDP based comparison is appropriate for low power portable systems in which the battery life is the primary index of energy efficiency. The following TABLE 1 & TABLE 2 furnished the performance parameters for different range of frequencies 1GHZ and 2 GHZ.

TABLE 1: OPERATING FREQUENCY AT 1GHz

SHIFT REG.	AVG POWER(W)	DELAY (s)	PDP (J)
SISO	2.082e-05	3.015n	6.27e-14
SIPO	2.082e-05	12.34p 1.015n 2.016n 3.015n	25.6e-17 2.11e-14 4.19e-14 6.27e-14
PIPO	7.810e-06	13.467p	105.12e-18
PISO	7.347e-06	3.029n	22.2e-15

TABLE 2: OPERATING FREQUENCY AT 2GHz

SHIFT REG.	AVG POWER(W)	DELAY (s)	PDP (J)
SISO	2.692e-05	2.012n	5.41e-14
SIPO	2.692e-05	14.794p 0.515n 1.014n 2.012n	39.8e-17 1.38e-14 2.72e-14 5.41e-14
PIPO	9.711e-06	14.184p	137.7e-18
PISO	4.541e-06	2.024n	9.19e-15

6.Conclusion

In this paper, we have designed low power single edge triggered D-FF based shift registers design using 32nm CMOS technology. The shift registers are simulated with different clock frequencies 1GHz and 2GHz.The shift registers design is efficient by comparing average power, delay and power delay product. Hence by performance analysis the low power single edge

triggered D-FF based shift registers design is efficient for low power applications.

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