Mathematical Modeling Of Digitally Controlled RF Self-Interference Canceller for Full-Duplex Transceiver

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***Abstract*—The mobile communications systems revolution the way in which the people communicate with each other. Nowadays Wide range of telecommunication services including advanced mobile services supported by mobile and fixed networks, which are increasingly packet based, along with a support for low to high mobility applications and wide range of data rates for multiuser environment are provided by 4G wireless standard LTE (Long Term Evolution). For the next generations of wireless technology will be required to achieve as much as a thousand-fold throughput increase over the current 4G systems. This can be achieved through different physical layer techniques such as a use of massive number of antennas and the use of centimeter and millimeter wave spectrum among others. In addition to this, more sophisticated transceiver architecture is required to increase the throughput with the physical layer techniques. In band full duplex technology will double the spectral efficiency. This transceiver architecture will help to reduce the demand from applications such as machine to machine communications called Internet of Things (IoT). To simulate the full duplex transceiver architecture using XILINX ISE 14.7. The simulated results produces increased throughput with reduced delay.**

***Keywords*—5G, FDD, LTE, In-band full duplex transceiver, IoT, Peak service rate, digital self-interference cancellation, spectrum efficiency, throughput, VLSI signal processing**

I. INTRODUCTION

The wireless cellular networks of 4G LTE technologies are having great communicational technologies globally. Most of the devices communicate each other via broadband wireless networks because of the advantages of wireless connectivity. This will helps to motivate the major manufacturers and mobile network operators for the development of LTE and LTE-Advanced standards. The road map from LTE to LTE-Advanced is illustrated in Fig.1.

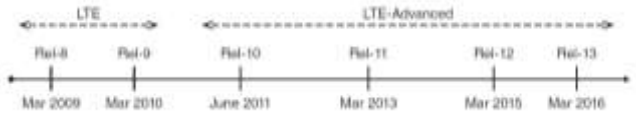


Fig.1. Road map from LTE to LTE Advanced

Signal processing is the most important role in the wireless technology. There are more number of signal processing techniques will be used in next wireless technology of 5G in order to increase the peak service rates, and also greatly increasing capacity, coverage, compatibility, reliability, convergence and efficiency in terms of both power and spectrum. In order to design the more sophisticated transceiver to increase the throughput, In-band full-duplex technology can be used to double the spectrum efficiency (bit/second/Hz) and it helps to reach the 5G standard with full potential [1].

The LTE-Advanced networks use cellular bands from 600 MHz to 3.5 GHz. The new frequency bands above 6 GHz (upto 100GHz) including the so called millimeter (mm) wave bands are expected in 5G. The standardization process for 5G is also expected to play a crucial role for the commercial success in the upcoming year [2].

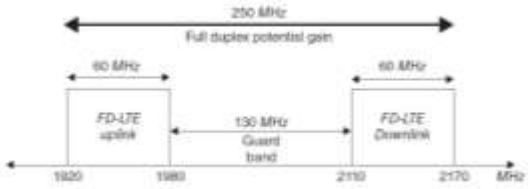


Fig.2. LTE FDD Spectrum Allocation

Full duplex means that "Bi-directional Communication", the device can transmit and receive at the same time over the same frequency. This will be used in 5G to reuse radio resources simultaneously for access and backhaul. The implementation of full duplex is the self-interference (SI) signal (i.e.).the part of the transmitted signal that leaks into the receiver chain.

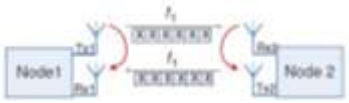


Fig.3. In-band full duplex

II. SELF-INTERFERENCE

The "Transmitter Leakage" that the signal leaks from the device transmitter to its own receiver. It will become an serious issues in decoding the desired signal, which could be noisy with a dramatically affected Signal-to-noise-ratio (SNR). In order to achieve the best performance of a full

duplex system, the Self Interference (SI) signal has to be suppressed to reach the receiver's noise floor. There are several SI cancellation methods are described in the current scenario.

The unavoidable SI in the full duplex transceiver limits the throughput, when the transmitted signal couples back to the receiver. Even though the transmitted signal is known in the digital baseband, it cannot be eliminated completely in the receiver because of Radio Frequency (RF) impairments [3] and large power difference between the transmitted and received signals. Co-channel Interference is also a dominant issue than SI. So it is the most challenging task to realize the higher levels of SI cancellation as the required isolation bandwidth is greater and also cause multipath scattering. It is possible for SI cancellation with multi antenna in full band radio transceivers by the use of non linear adaptive SI cancellation algorithms.

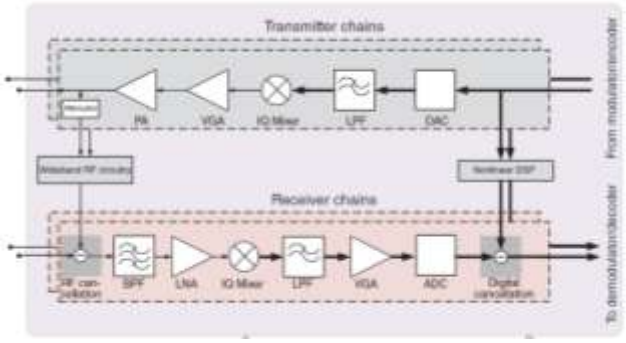


Fig.4. A multiantenna radio transceiver

III. DIGITAL SELF INTERFERENCE CANCELLATION ALGORITHMS

A. *Signal Model*

The baseband model of a communication link of a communication link with full duplex transceivers is shown in the Fig.1. It shows that the system includes bidirectional communication (source and destination are the same node). Here the full duplex transceiver acts as a relay link and it is simultaneously serving an uplink user and a downlink user in the same frequency band.

Where, A_s Source transmit antennas and A_D destination receive antennas. A_{tx} transmit antennas and A_{rx} receive antennas. These two antenna arrays are spatially separated and the model is applied to the single array design [4][5].

Equation (1) for the MIMO channels from the source to the transceiver.

$$H_{ST}[n] \in C^{A_{rx}\ X\ A_S} \quad (1)$$

Equation (2) for the MIMO channels from the transceiver to the destination.

$$H_{TD}[n] \in C^{A_D\ X\ A_{tx}} \quad (2)$$

At the time n, the source transmits signal vectors in Equation (3)

$$X_S[n] \in C^{A_S} \quad (3)$$

At the time n, the transceiver transmits signal vectors in Equation (4)

$$X_T[n] \in C^{A_{tx}} \quad (4)$$

While it simultaneously receives signal vector in Equation (5)

$$Y_T[n] \in C^{A_{rx}} \quad (5)$$

The output $Y_T[n]$ creates an unavoidable SI feedback loop from the transceiver output to the transceiver input through channel shown in Equation (6)

$$H_{TT}[n] \in C^{A_{rx}\ X\ A_{tx}} \quad (6)$$

Spatial interference suppression is provided by the precoding matrix $G_{tx}[n]$ and beamforming matrix $G_{rx}[n]$ and $A[n]$ is used to subtract the contribution of the transmitted signal form the received signal for the purpose of cancellation. The corresponding received signals in the transceiver and in the destination node can be expressed in Equations (7) and (8).

$$Y_T[n] = G_{rx}[n] * (H_{ST}[n] * X_S[n] + H_{TT}[n] * G_{tx}[n] * X_T[n]) + n_T[n] \quad (7)$$

$$Y_D[n] = H_{TD}[n] * G_{tx}[n] * X_T[n] + n_D[n] \quad (8)$$

Equations (9) and (10) are additive noise vectors in the transceiver and in the destination ($* refers\ to\ convolution$)

.

$$n_T[n] \in C^{A_{rx}} \quad (9)$$

$$n_D[n] \in C^{A_D} \quad (10)$$

Here the signal is capable of modeling multipath MIMO channels in the time domain with arbitrary modulation.

B. *Basic Principles*

Digital cancellation techniques includes the SI signal is generated and then subtracted from the received signal. But here we can apply spatial suppression if transmitter and receiver antennas are spatially separated. This requires multiple antennas in both ends, at the transmitter side precoder is used and the receiver side beam former is used to simultaneously attenuate the SI signal and receive the payload signal. In order to attenuate the effect of RF imperfections RF beam former is used, because they pass through the same channel together with the known part of the SI signal.

This may cause interference in the system, to make a nearly interference–free system, the proper cancellation method is used for each application. When both transmit and receive sides of the full-duplex device behave primarily like a linear filter, cancellation can be reduced to designing a filter that identifies the SI channel, since the transmitted signal is known at every time instant. Any linear cancellation architecture cannot mitigate nonlinear behavior and noise sources, such as nonlinear distortion of the PA, I/Q imbalance during modulation/demodulation, phase noise, or quantization noise at the receiver [6][7][8][9]. So we use the nonlinear architecture for full duplex transceiver architecture. Here digital mitigation is performed in both the time domain and the frequency domain.

The mitigation in the frequency domain involves the processing of each subcarrier signal individually, which may cause the computational demand if the number of subcarriers

is large. On the other hand, mitigation in the time domain involves processing the signal samples independently of the number of subcarriers, but, due to the different interference paths between antennas, requires gauging the delay spread of the SI channel [10]. Mitigation takes place after baseband demodulation and digital conversion of the received signal, usually being the first operation within the digital pipeline. As a result, the employed signal must be sampled above the Nyquist rate, which demands the use of special techniques to deal with arbitrary signal spectra [10].

C. Spatial suppression

Spatial-domain suppression [11] employs receive- and/or transmit-side feed forward filters, namely $G_{rx}[n]$ and $G_{tx}[n]$, which are matched to the SI channel alone without relying upon accurately knowing actual signals. This is in contrast to the feedback filters used in subtractive cancellation for generating an estimated copy of the SI signal from the imperfectly known transmitted signal. Nevertheless, spatial suppression can similarly mitigate SI; the pros and cons are weighed up next, when we compare the approach to time-domain cancellation.

In principle, suppression works by employing beam forming filters that direct reception and/or transmission of the signal of interest to the null space of the SI channel such that signal propagation is ideally blocked completely or, if the spatial degrees-of-freedom are scarce, to the weakest Eigen modes thereof such that the effective gain of the residual feedback channel is minimized. Mathematically this means solving in terms of some suitable matrix as in Equation (11)

$$\min ||G_{rx}[n] * H_{TT}[n] * G_{tx}[n]|| \xrightarrow{ideally} G_{rx}[n] * H_{TT}[n] * G_{tx}[n] = 0 \qquad (11)$$

Such a mitigation approach is therefore applicable only with multi-antenna transceivers, and having low rank in the SI channel can boost suppression performance significantly. Likewise, beamforming always consumes the degrees-of-freedom, restricting the trade-off between spatial diversity and multiplexing in the signals of interest, which can be seen as reducing the effective number of antennas used for data transmission if suppression is implemented transparently around actual en/decoding blocks. Suppression is also obviously sensitive to estimation error in feedback channel-state information, not so unlike cancellation. However, the residual interference signal is not linearly proportional to the error term or its gain level because estimation error manifests itself as distorted beam patterns.

The main benefit of suppression over cancellation is the fact that it mitigates blindly all signal, distortion and noise components that pass through the loopback SI channel. Such a receive filter satisfies the Equation (12)

$$\min ||G_{rx}[n] * H_{TT}[n]|| \xrightarrow{ideally} G_{rx}[n] * H_{TT}[n] = 0 \qquad (12)$$

This means that all the adverse transmit-side components caused by non-linear RF imperfections are suppressed at the receiver side together with the linear signal components, no matter how large the transmitter's EVM is Yet suppression is achieved with simple linear digital signal processing without any need for modeling or implementing complex transceiver electronics, in contrast to analog or non-linear digital cancellation. Transmit-side beam forming will conversely suppress SI on-the-air before it even reaches the receiver front end such that problems related to limited ADC dynamic range and quantization noise are alleviated. In Equation (13)

$$\min || H_{TT}[n] * G_{tx}[n]|| \xrightarrow{ideally} H_{TT}[n] * G_{tx}[n] = 0 \qquad (13)$$

Thus it is also beneficial to employ spatial-domain suppression together with linear time-domain cancellation such that the latter efficiently eliminates the linear signal components and then takes care of the residual non-linear distortion components in an economic way.

IV. NONLINEAR CANCELLATION

The different RF impairments distort the observed SI signal such that it is no longer a linear transformation of the original TX signal. This means that nonlinear modeling is required to fully grasp the effects of the effective SI propagation channel, which includes various sources of nonlinear distortion. Nonlinear effects, such as amplifier distortion or mixer nonlinearities, can be accurately modeled using polynomial-based systems [12, 13, 14], whereas I/Q imbalance can be modeled using widely linear filters [24], which have been extensively studied in the literature.

As a starting point, the baseband signal of TX j (j = 1, 2,. . . , N_{tx}) is denoted by $x_j(n)$. The first component distorting the TX signal is the I/Q modulator, [14] which will inherently introduce some I/Q imbalance. The output signal of the I/Q modulator model (using a frequency-independent model for simplicity) is in Equation (14)

$$x_j^{IQM}(n) = k_{1,j}\, x_j(n) + k_{2,j}\, x_j^*(n) \qquad (14)$$

$$k_{1,j} = 1/2(1 + g_j \exp(j\varphi_j)) \qquad (15)$$

$$k_{2,j} = 1/2(1 - g_j \exp(j\varphi_j)) \qquad (16)$$

where g_j , φ_j are the gain and phase imbalance parameters of TX j. Notice that for any practical TX front end $|K_{1,j}| \gg |K_{2,j}|$. The strength of the induced I/Q image component, represented by the conjugated signal term in Equation (14), is typically characterized with the image rejection ratio as $10\, log_{10}\, (|K_{1,j}|^2/|K_{2,j}|^2)$.

The output signal of I/Q modulator is then fed to the TX PA, which will further distort it. A common approach is to use polynomials to model the nonlinear distortion produced by the PA. In brief, polynomial-based systems model nonlinearities by processing higher-order terms of the input signal. Typically, a parallel Hammerstein (PH) model with polynomial branch nonlinearities and FIR branch filters is assumed for the PA. Using the PH model, the output signal of the PA can be written as in Equation (17).

$$x_j^{PA}(n) = \sum_{\substack{P=1 \\ P\ odd}}^{P} \sum_{m=0}^{M} h_{p,j}(m)\varphi_p\,(x_j^{IQM}(n-m)) \qquad (17)$$

where M and P denote the memory depth and nonlinearity order of the PH model, $h_{p,j}(m)$ denote the FIR

filter impulse responses of the PH branches for TX j, and the basis functions are defined as in Equation (18).

$$\varphi_p(x(n)) = |x(n)|^{p-1}x(n) = x(n)^{\frac{p+1}{2}}x^*(n)^{\frac{p-1}{2}} \quad (18)$$

In general, the number of parameters of a Hammerstein model grows linearly with order P, while in the MIMO case, the increase is also relative to the number of TX and RX antennas [14]. The PH nonlinearity is a widely used nonlinear model for direct as well as inverse modeling of PAs and has been observed, through RF measurements, to characterize the operation of various PAs in an accurate manner [15].

Using Equation [14] and [17], the overall output signal of the TX can be expressed as

$$x_j^{PA}(n) = \sum_{\substack{P=1 \\ P\ odd}}^{P} \sum_{m=0}^{M} h_{p,j}(m)\varphi_p\,(x_j^{IQM}(n-m)) \quad (17)$$

1.4 Layer Mapping

The Layer mapping process maps the complex valued modulation symbols onto each layer used for transmission. Two layers are used to carry modulated transmit code words with transmit diversity. Transmit diversity is used to separate one source signal into two or more independent signals. The use of transmit diversity is implied when using DCI format 1A [6].

1.5 Pre Coding

The vectors $x(i)= [x^{(0)}(i) \dots x^{(v-1)}(i)]^T, i= 0,1,\dots,M_{symb}^{layer}-1$ is the input block of the precoder from the Layer mapping and generates a block of vectors $y(i) = [\dots y^{(P)}(i) \dots]^T$, $i = 0,1,\dots,M_{symb}^{ap}-1$ to be mapped onto resources on each of the antenna ports, where $y^{(P)}(i)$ repersents the signal for antenna port p.

1.6 Mapping to Resource Elements

The RE mapping process maps complex-valued modulation symbols for each antenna port to corresponding REs on resource grids. All REs are mapped in terms of Resource Element Groups (REGs)[8]. Every four REs available for mapping L1/L2 control signals forms a REG. Each REG is mapped with a symbol quadruplet which consists of 4 complex-valued symbols. This mapping method is used to support transmit diversity.

2.PCFICH Receiver

The receiver part of the PCFICH from the channel including the reverse process of transmitter part block and get the original CFI value are discussed below.

2.1 Layer Demapping and Deprecoding

The layer demapping and deprecoding returns the block of symbols d_i. After layer mapping and precoding$r_i^{(p)}$, where p is the antenna port index, the process is according to Equation 1 and 2.

$$d_{2i} = \mathrm{Re}(a_i^0) + \mathrm{Im}(b_i^0) \cdot j \text{ for } i = 0, \dots, \frac{N}{2} - 1 \quad (1)$$

$$d_{2i+1} = \mathrm{Re}(a_i^1) + \mathrm{Im}(b_i^1) \cdot j \text{ for } i = 0, \dots, \frac{N}{2} - 1 \quad (2)$$

where N is the length of input complex-valued symbols and $a_i^{(p)}$ and $b_i^{(p)}$are generated according to Equation 3, 4,5and 6.

$$a_i^0 = r_{2i}^{(0)} + r_{2i+1}^{(1)}\ for i = 0, \dots, \frac{N}{2} - 1 \quad (3)$$

$$a_i^1 = r_{2i}^{(1)} - r_{2i+1}^{(0)}\ for i = 0, \dots, \frac{N}{2} - 1 \quad (4)$$

$$b_i^0 = r_{2i}^{(0)} - r_{2i+1}^{(1)}\ for i = 0, \dots, \frac{N}{2} - 1 \quad (5)$$

$$b_i^1 = r_{2i}^{(1)} + r_{2i+1}^{(0)}\ for i = 0, \dots, \frac{N}{2} - 1 \quad (6)$$

2.2 Demodulation

The BPSK demodulation generates a block of bits $\beta_i\, for i = 0,1, \dots, N-1$ where N is the length of input block of symbols d_i. The BPSK demodulation process is according to Table III

TABLE III BPSK demodulation lookup table

d_i	β_i
$1 + 1i$	0
$-1 - 1i$	1
0	0

The QPSK demodulation generates a block of bits $\beta_i\, for i = 0,1, \dots, 2N-1$, where N is the length of input block of symbols d_i[11].The process has hard decision type and soft decision type. The hard decision process returns the bit sequence with value 0 or 1 and is used for PCIFCH demodulation. The hard decision process is done according to Table IV.

Table IV Hard decision QPSK demodulation

$\mathrm{Re}(d_i)$	$\mathrm{Im}(d_i)$	b_i , b_{i+1}
≥ 0	≥ 0	00
≥ 0	< 0	01
< 0	≥ 0	10
< 0	< 0	11

2.3 Descrambling

The descrambling process is the reverse of scrambling process which returns the unscrambledbit sequence b_i from scrambled bit sequence B_i. The process is as defined by the Equation 7.

$$B_i = (B_i + c_i) \bmod 2 \text{ for } i=0,\ldots, L-1 \quad (7)$$

WhereL is the length of B_i and $c_i$is the scrambling sequence, generated as described in the Section 1.2.

IV PCFICH ARCHITECTURE

The Architecture flow of the PCFICH is drawn based on the blocks present in the block diagram. The flow of this diagram is fully based on the DSP. This can be made efficient using the various VLSI concepts like unfolding and retiming. Here both of the conceptsare used to achieve the efficient architecture.

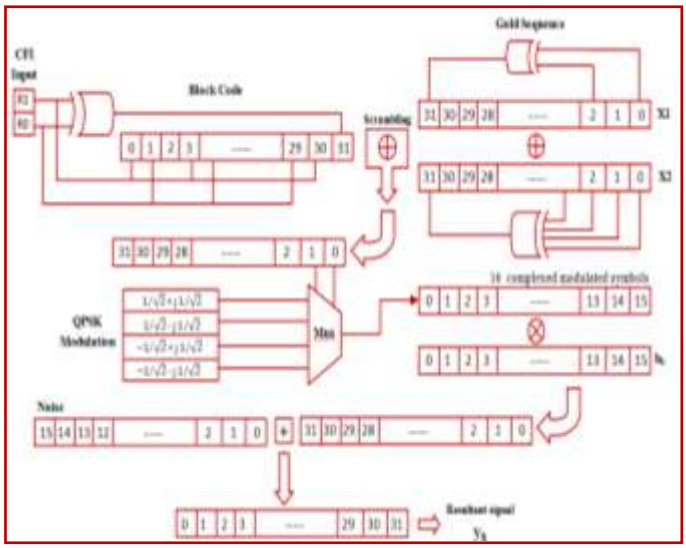


Fig.4 PCFICH Transmitter architecture

3.1 PCFICH Transmitter Architecture

The transmitter architecture of PCFICH downlink physical control channel is presented in Fig.4. The block diagram of the PCFICH transmitter is discussed in the chapter III.The first block of this architecture is block coding.

The input of this block code is the 2 bit CFI value R1 and R0. The 2 bit value is converted into 32 bit value by block coding.The first two bits are same as the original bits and the third bit is the XOR value of the first two bits. The 3 bit pattern is repeated until the required 32 bits are obtained[10]. It is represented in Fig.5. These 32 bits form the CFI codeword.

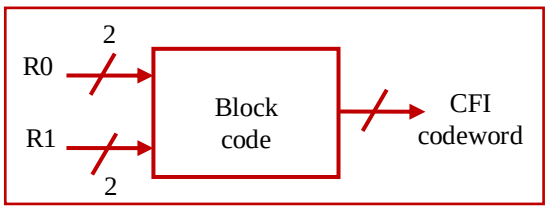


Fig.5 Block code

The second block is the scrambling process. This process requires gold sequence generation. The gold sequence is produced by using the two sequences $x1$ and $x2$. Here the x1 sequence is the predefined sequence i.e,"10000000000000000000000000000000". The $x2$ sequence also have 31 bits that is assumed according to the applications. The 32ndbit of both sequences are calculated using Equation (8),(9) and (10). Then these 2 sequences are XORed to get the gold sequence. The result is also a 32 bit value.

$$x1(n+31) = (x1(n+3) + x1(n)) mod 2 \quad (8)$$

$$x2(n+31) = (x2(n+3) + x2(n+2) + x2(n+1) + x2(n)) mod 2 \quad (9)$$

$$c(n) = (x1(n) \oplus (n)) mod 2 \quad (10)$$

Then scrambling is done by XOR of the block coded sequence and the gold sequence. It is shown in Fig.6

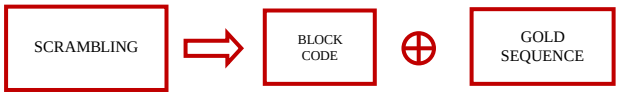


Fig.6 Scrambling process

The resultant scrambled sequence isstored in a shift register. The shift register is set to shift 2 bitsper clock cycle for QPSK modulation. The shifted 2 bits aregiven as control lines for the multiplexer. The inputs to themultiplexer are stored in RAM table. There are 4 possible complexmodulated QPSK symbols. Based on thecontrol, the output appears, which is represented as 16 bitvalue.

The 16 complex modulated symbols are then layer mappedto one, two or four layers based on the information fromhigher layer.Z1 is the output if one antenna is selected.Z2,Z3are outputs if 2 antennas are selected and Z4,Z5,Z6,Z7 if 4antennas are selected.

The modulated symbol is multipliedwith the complex channel frequency response vector h_k, whichis also represented as a 16 bit value. The resultant is a 32 bitvalue. Then noise which is represented using 16 bits is added.Thus the resultant signal y_k is a 32 bit value.

3.2 PCFICH Receiver Architecture

The received signal is demapped from the 16 positions of first OFDM symbol, where CFI value is available. The receiver architecture is presented in Fig.7. It is known that, there are only three possibilities of signal transmitted, namely01,10 or 11(CFI-1,2 or 3)[12].So, the demodulated signal will be one among the three. The received signal is y_k and is multiplied with the conjugate of the complex channel frequency response vector h_k^*, element by element. Then thisresultant term undergoes inner product with the three possible values of d(m). The inner product is done using.

$$\sum_{0}^{32}$$

The $d^{(m)*}$ is multiplied with $(y_k^0 h_k^*)$ product .For allthe elements the multiplication is done and the results areaccumulated, and the result is a 64 bit value[13]. The real part of accumulated value alone is taken, which is a 32 bit value.

This process is done for the three values viz. $d^{(0)}$,$d^{(1)}$,$d^{(2)}$.Then among the three results, the codeword which has the maximum argument value is detected as the CFI.

In the receiver side, after removal of cyclic prefix from the received signal, then FFT is performed and then resource element demapping is done. The complex valued output at the *k*-th receive antenna is modeled in Equation(11)

$$y_k = h_k^0 d^{(n)} + u_k \, , k = 1,2, \dots , k \qquad (11)$$

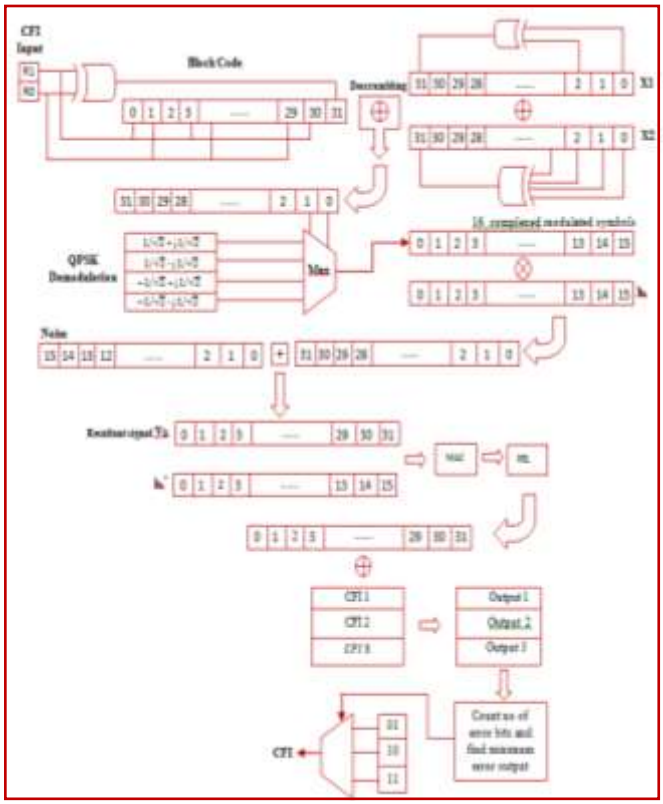


Fig.7 PCFICH Receiver architecture

$y_k$is 16x1 received subcarrier vector, $d^{(n)}$ is the 16x1complex QPSK symbol vector corresponding to the 32-bit CFI code words, where n varies from 1 to 3, $h_k$is 16x1complex channel frequency response and u_k represents the contribution of thermal noise and interference.

The received signal y_k is represented in the figure 2,for single antenna case. The noise term $u_k$is modeled as zero mean circularly symmetric complex Gaussian with covariance$E[u_k u_k^H] = \sigma_u^2 I$,since the interferers are uncorrelated due to independent large scale propagation, short term fading and uncorrelated scrambling sequences.

4.1CFI Estimation

The ML decision rule, by maximizing the log-likelihood function of y_k *and* $h_k$is given in Equation (12)

$$\text{CFI} = \min_{m=1,2,3} \sum_{k=1}^{k} \left| y_k - \left(h_k^0 \, d^{(m)} \right) \right|^2 \qquad (12)$$

Which simplifies to

$$CFI = \text{argmax}_{m=1,2,3} \, z^{(m)} \qquad (13)$$

Where the soft outputs are given by

$$z^{(m)} = \sum_{k=1}^{k} z_k^{(m)} \qquad \text{for m = 1,2,3} \qquad (14)$$

Which is simplified as

$$\text{CFI} = \underset{m=1,2,3}{\text{argmax}} \sum_{k=1}^{k} Re\left\{ \langle y_k^0 h_k^* d^{(m)} \rangle \right\} \qquad (15)$$

4.2 Received Signal

The received signal $y_k$is element by element multiplied with the conjugate of the complex channel frequency response vector h_k^*.Then this term and three possible values of *d* (*m*) undergoes inner product. The inner product is given in Equation (16)

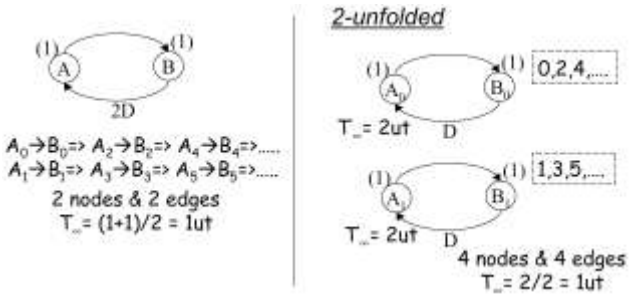
$$\langle x, y \rangle = \sum_{k=1}^{k} x_i y_i^* \qquad (16)$$

The real part of the resultant value is taken. This is done for number of times as the number of antennas used to receive. Then argument max among the three values is selected as the CFI value. If CFI is maximum value when m=1, then the codeword detected is 01, when m=2, it is 10 and when m=3, it is 11.

V UNFOLDING AND RETIMING

5.1 Unfolding

Unfolding = = Parallel Processing



In a 'J'unfolded system each delay is J-slow. if input to a delay element is the signal x(kJ + m), the output is in Equation (16)

$$x((k-1)J + m) = x(kJ + m - J) \qquad (16)$$

Algorithm for unfolding

For each node U in the original DFG, draw J node U_0, U_1,U_2,… , U_{J-1}

For each edge U→ V with w delays in the original DFG, draw the J edges $U_i \rightarrow V_{(i+w)\%J}$ with [(i+w)/J] delays for i= 0, 1, … , J-1.

Unfolding of an edge with w delays in the original DFG produces J-w edges with no delays and w edges with 1delay

in J unfolded DFG for w < J and unfolding preserves precedence constraints of a DSP program[14].

Properties of unfolding :

Unfolding preserves the number of delays in a DFG. Thiscan be stated as follows(17),

□w/J□□+ □(w+1)/J□□+ … + □(w + J - 1)/J□□= w (17)

5.2 Retiming

This section considers some techniques used for retiming.

First, two special cases of retiming, namely, *cutset retiming* and *pipelining*, are considered. Two algorithms are then considered for retiming to minimize the clock period and retiming to minimize the number of registers that are required to implement the circuit.Cutset Retiming is a useful technique that is a special case of retiming. A *cutest* is a set of edges that can be removed from the graph to create 2 disconnected subgraphs. Cutset retiming only affects the weights of the edges in the cutset. If the 2 disconnected subgraphs are labeled G_1 and G_2, then cutset retiming consists of adding k delays to each edge from G_1 to G_2 and removing k delays from each edge from G_2 to G_1. For example, a cutset is shown with a dashed line in Fig. 4.4(a). The 3 edges in the cutset are $2 \rightarrow 1$, $3 \rightarrow 2$, and $1 \rightarrow 4$. The 2 subgraphs G_1 and G_2 found by removing the 3 edges in the cutset are shown in Fig.8. For $k = 1$, the result of cutset retiming. The edges from G_1 to G_2 are $3 \rightarrow 2$ and $1 \rightarrow 4$, and one delay is added to each of these edges[15]. The edge from G_2 to G_1 is $2 \rightarrow 1$, and one delay is subtracted from this edge[7].

VI RESULTS AND DISCUSSION

6.1 Simulation result for PCFICH

The each and every block of the PCFICH downlink physical control channel is simulated using the Xilinx ISE 14.7 software.Verilog Hardware description language (VHDL) is used to simulate the codes for each and every block for PCFICH transceiver with unfolding and retiming approach for efficient architecture. The CFI is detected as the output of the after 15 time units.

6.1.1 Block coding

The input of the block code is 2 bit and the output of this block code is 32 bit. It is analyzed based on the CFI present in the system and also depicted according to the application. The simulation waveform for the block code is depicted in the Fig.9.

Fig.9 Simulation result for Block coding

6.1.2 Scrambling and Descrambling

The input of the scrambler block is 32 bit and the output of this scrambler block is also 32 bit. Here 31 gold sequence also generated using the cell specific sequence generator. It was analyzed based on the CFI present in the system and also depicted according to the application. The original CFI value is get back in receiver. The simulation waveform for the block code scrambling and descrambling is depicted in the Fig.10.

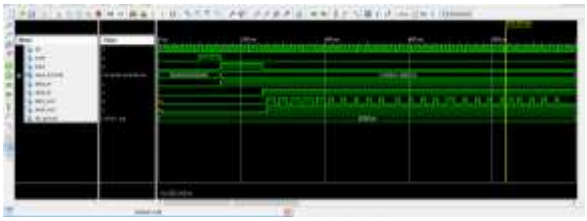


Fig.10 Simulation result for scrambling block

6.1.3 QPSK Modulation and Demodulation

The output of the 32bit scrambling sequence is given to the input of the QPSK modulation and the reverse process is the QPSK demodulation and the simulation result for QPSK modulation and demodulation is shown in Fig.11.

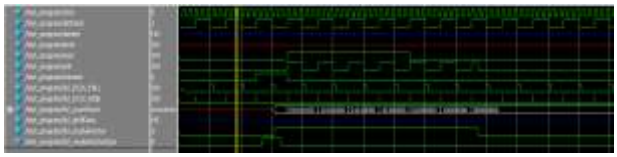


Fig.11 Simulation results of QPSK modulation and demodulation

6.1.4 PCFICH Transceiver Output

The entire block of the transceiver architecture coded and combined as the consequence of output to get the simulation result as in Fig.12.

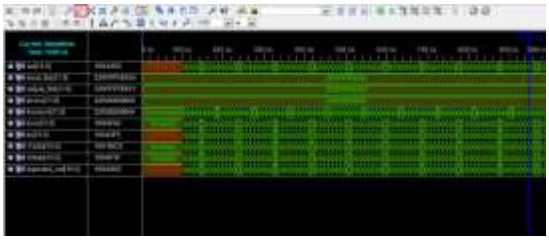


Fig.12 Simulation results of PCFICH Transceiver

6.1.5 Unfolding and Retiming

The Output of the PCFICH transceiver is fed into the unfolding and retiming process to get the efficient output of minimum delay and maximize the efficiency. It is shown in Fig.13.

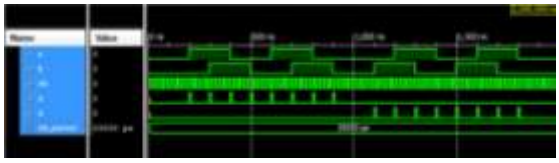


Fig.13.Simulation results of Unfolding and Retiming

VII CONCLUSION

This paper describes about simulated results of each and every block of the transceiver architecture. The output of the entire block is combined and the total output of the system in the receiver side is getting the CFI value. This output will have larger delay due to the channel noise and architecture flow. The unfolding concept is used at the CFI of the receiver architecture to reduce the delay and power consumption. The retiming is also used to reduce the number of registers present in the architecture. The output of the normal architecture will give the best result of time delay of 5 time units. The increased efficiency of architecture is 1.44. The overall architecture result produced in our paper creates the better performance than the previous one. In future work the proposed work will be extended to minimize the number of delays by the use of any other VLSI DSP concept techniques.

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