

Mitigation of Power Quality Problems using open UPQC

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Abstract:-Voltage sags and current harmonics are prominent power quality issues that are needed to be taken into account primarily. For mitigation of such power quality issues an Open Unified Power Quality conditioner (UPQC), for which the necessary reference signals are extracted using an algorithm that relies on the Enhanced phase locked loop and adaptive non-linear filter has been used. The complex nonlinear and time variant algorithm is analyzed in a simple way. Gate pulses for the UPQC are generated through hysteresis control. A new fast sag/swell detection technique along with fast termination of enable signal has been proposed. Along with this time limit on duration of compensation has been imposed. The proposed system was simulated in Matlab/Simulink and results are verified with standards.

Keywords-PLL, UPQC, PLL

I. INTRODUCTION

With wide spread use of power electronic technology, there is an alarming raise of power quality problems. UPQC can be used to mitigate some of those problems. Passive filters have been used age long to minimize the harmonics, which involves complex tuning of filters for eliminating each frequency. Because of which the current quality improvement is limited. Means, Total harmonic distortion cannot be improved below 15%. The control technique used for series and shunt converter must be fast in dynamic response in order to quickly detect and track the respective command signal. For the shunt converter the reference signals necessary are usually generated by P-Q theory [2] and for series converter d-q transform[3].

In this paper for both the converters a new algorithm from[1] has been used to extract the necessary reference signals. Generally, the hysteresis method for shunt converter and SVPWM for series converter are used for power amplification. In this paper, hysteresis method is used for both the converters because of its high dynamic performance which is essential for this particular application.

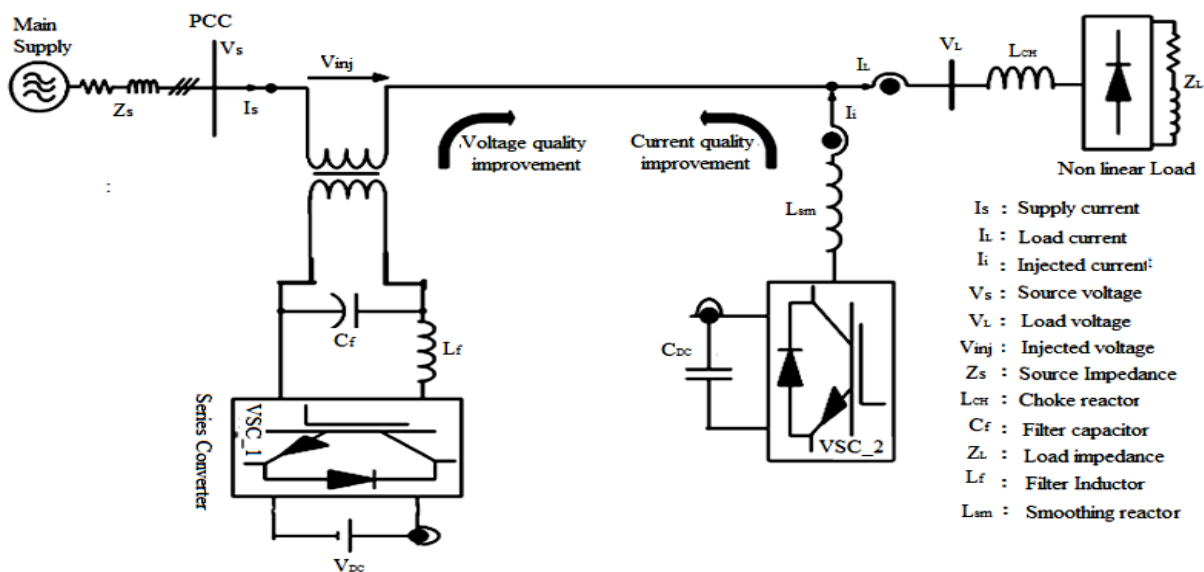


Fig.1: Block diagram of proposed system connected to open UPQC

The sag detection by monitoring of $\sqrt{(v_d^2 + v_q^2)}$ used in [4] and Fast sag detection which is proposed in [1] has certain disadvantages. Hence the method proposed in [1] has been improved.

The contributions of this paper are:

1. A control algorithm based on enhanced PLL and non-linear adaptive filter has been implemented and analyzed in a simple way. For the compensation purpose open UPQC is used.
2. Hysteresis method is used for generating gate pulses to both shunt and series converters.
3. The novel sag detection method which can both detect the sag quickly and terminate the enable signal quickly soon after voltage sag, is being implemented. Along with this time limit of compensation has been imposed on the system.

II. UPQC CONNECTED TO PROPOSED SYSTEM

The Open UPQC configuration selected consists of two voltage source converters [VSC1 and VSC2]. This configuration has the advantage of elimination of large dc link capacitor required and a controller required to maintain its output voltage constant. VSC1 is the series converter and VSC2 is the shunt converter, which are connected back to back through a dc voltage source. The L_f and C_f forms the filter circuit, L_{sm} is for smoothing of current injected and L_{ch} is for enhancement of load. A simple diode non-linear load is considered for analysis. The parameters of the test system are given in [1]. The whole setup is shown in figure.2.

The circuit of VSC2 consists of a three phase inverter while the circuit of VSC1 consists of three single phase H-bridge inverters. The inverters can be operated in two modes. The shunt converter operates continuously injecting harmonics, while the series converter comes into picture on the detection of sag.

III. CONTROL OF SERIES CONVERTER

It includes individual extracting of error signal from each phase, detecting the sag and generating the Gate pulses at respective time of occurrence of sag.

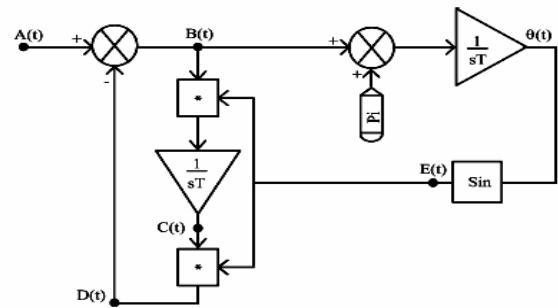


Fig.2: Proposed algorithm

A(t) = Input Signal

B(t) = The difference between input and system

C(t) = The amplitude of D(t)

D(t) = Synchronized fundamental component

E(t) = PLL Signal

The proposed algorithm is extracted from the novel reference signal generation method [1]. The PLL signal unlike normal PLL not only locks the phase but also the magnitude of the supply signal. The error signal can therefore be obtained by subtracting PLL signal from supply signal. The mathematical analysis of the algorithm is given in [1].

A. Simulation of algorithm

An L-G fault on the proposed system is created in between 1.5 to 1.6 sec which creates sag of 0.25p.u. various reference signals obtained from the simulation of algorithm are as shown below.

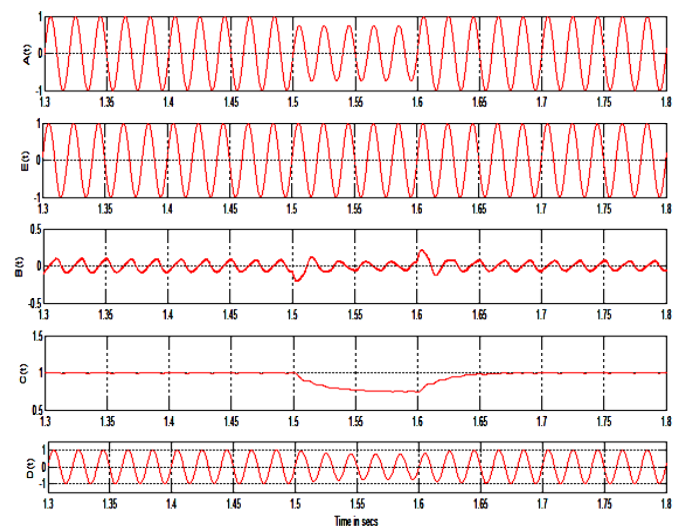


Fig. 3: Extracted components from supply voltage

B. Analysis of the algorithm:

The algorithm is analyzed in a simple way other than that in [1].

Step1: $A(t) = B(t) = \sin wt \dots$ from fig 2

The output from summer block = $\sin wt + \pi$

(Considering, $\tau = 0.01$)

Step 2: $\theta(t) = (1/0.01) * \int (\sin wt + \pi) . dt$
 $= 100 * [-\cos wt/w + \pi * t]$

The first term being small when compared with second term, hence can be neglected.

Hence $\theta(t) = 100 * \pi * t = 314t$.

Step 3: $E(t) = \sin(314t)$ (1)

Equation (1) is Enhanced Phased Lock Loop (PLL) Signal.

Step 4: $C(t) = \int [B(t) * E(t)] . dt$ (2)

For first half cycle:

$C(t) = 1/0.01 \int_0^{0.01} \sin wt * \sin wt . dt + C_i$ (3)
 $= 1/0.01 \int_0^{0.01} (1 - \cos 2wt) / 2 . dt$
 $= 1/0.01 * [1/2 t] = 1/2$ ----- after half cycle.

$D(t) = 0.5 \sin wt$, $B(t) = A(t) - D(t) = 0.5 \sin wt$

For second half cycle:

$C(t) = 1/0.01 \int_{0.01}^{0.02} 1/2 \sin wt \times \sin wt + C_i$ (4)

$C(t) = 1/4 + 1/2$

Then after a full cycle, $D(t) = 3/4 \sin wt$,
 $B(t) = 1/4 \sin wt$,

After integration;

$C(t) = 1/8 + 1/4 + 1/2;$

$C(t)$ follows the sequence

$C(t) = 1/2 + 1/4 + 1/8 + 1/16 + \dots \dots \dots \infty$.

They are in Geometric Progression.

Sum of infinite terms = $a / (1-r) = 0.5 / (1-0.5) = 1$. Where, 'a' is the initial term and 'r' = multiplication factor.

Therefore $C(t)$ settles to 1 while $D(t)$ settles to $1 \sin wt$.

C. Analysis of the algorithm when 0.25 p.u. sag has occurred

$A(t) = 0.75 \sin wt$ and $D(t) = \sin wt$

Therefore, $B(t) = -0.25 \sin wt$

$C(t) = 1/0.01 \int_{0.01}^{0.02} -0.25 \sin^2 wt . dt + C_i$ (5)

= $-1/8 + 1$ after first half cycle of occurrence of sag.

After consecutive half cycles

$= 1 - (1/8) - (1/16) - (1/32) - \dots \dots \dots$ infinite terms
 $= 0.75 p.u$

Whenever the sag terminates $A(t) = \sin wt$, $D(t) = 0.75 \sin wt$

$C(t) = 1/0.01 \int_0^{0.01} 0.25 \sin^2 wt . dt + C_i$ (6)

$C(t) = 1/8 + 0.75,$

After consecutive cycles

$= 0.75 + 1/8 + 1/16 + 1/32 \dots \dots \dots = 1$ as they are in G.P.

D. Analysis of algorithm when third harmonic is present in A(t):

Consider the input signal to the algorithm has third harmonic component

$A(t) = \sin wt + 0.2 \sin 3wt = B(t)$

For first half cycle;

$C(t) = 100 \int_0^{0.01} (\sin wt + 0.2 \sin 3wt) \times \sin wt . dt + C_i$ (7)

$= \int_0^{0.01} [(1 - \cos 2wt) / 2] + 0.2 / 2 \times (\cos 2wt - \cos 4wt) . dt =$

$1/0.01 * [1/2 t] + 0 = 1/2$ ----- after half cycle.

$D(t) = 0.5 \sin wt$, $B(t) = A(t) - D(t) = 0.5 \sin wt + 0.2 \sin 3wt$

After few consecutive half cycles, $C(t)$ becomes equal to 1 (the reason explained above) and hence $D(t)$ becomes $\sin wt$, hence $B(t) = A(t) - D(t) = (\sin wt + 0.2 \sin 3wt) - (\sin wt) = 0.2 \sin 3wt$.

$t \xrightarrow{Lt} \infty B(t) = 0$ [In case $A(t)$ is free of harmonics]

$t \xrightarrow{Lt} \infty B(t) = \text{Sum of all the harmonics}$ [In case $A(t)$

contains harmonics].

E. Hysteresis voltage control

Hysteresis voltage control is used for power amplification of error signal [5]. This is chosen because of its high dynamic performance. The block diagram involving the series converter control is as follows.

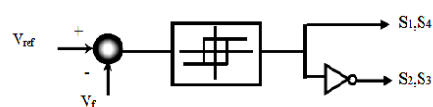


Fig.4: Hysteresis voltage controller

$$V_f = V_{ref} + HB \text{ in rising case.}$$

$$V_f = V_{ref} - HB \text{ in decreasing case.}$$

Hysteresis voltage controller uses the on-off relay to give the gate pulses to the series convertor. A fixed band is set through the on-off relay. The output of on-off relay changes every time the inverter output touches the band limits and a sinusoidal wave at the inverter output is obtained within the band to be injected into the line [5]. This should happen only when the error is between 0.1-0.9 so an enable signal is used to pass the gate pulses only when the error is within the IEEE standards.

F. Sag/Swell Detection Method

The sag/swell detection method proposed in [1] has the disadvantage of time taking in turning down the enable signal if the sag is deep. Hence the inverter continues to inject error voltage before $c(t)$ can settle to 0.9 p.u. which can result in unnecessary injection of harmonics. Hence a new method that uses error derivate term over a cycle is also considered for success full termination of enable signal soon after the termination of sag. The derivative of $1-C(t)$ changes from positive to negative soon after sag. This logic is used to make the enable signal low soon after sag.

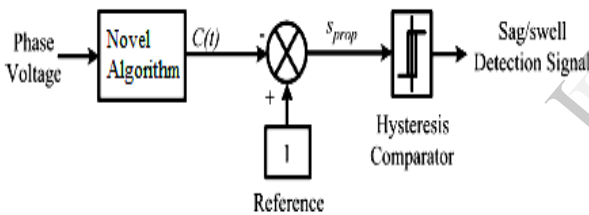


Fig.5: Block diagram of sag detection technique in[1]

Sag of magnitude 0.25 p.u. from 1.5 to 1.6 is created on the proposed system and the sag is detected after 0.0054 sec after initiation of sag as shown below. The sag detection method's ability to terminate the enable signal soon after the sag is compared with that in [1].

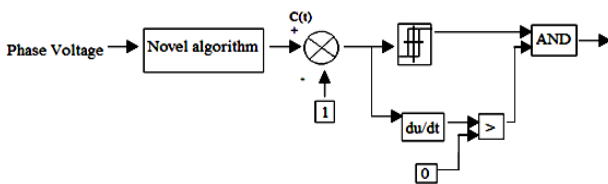


Fig.6: Block diagram of the proposed Sag detection method .

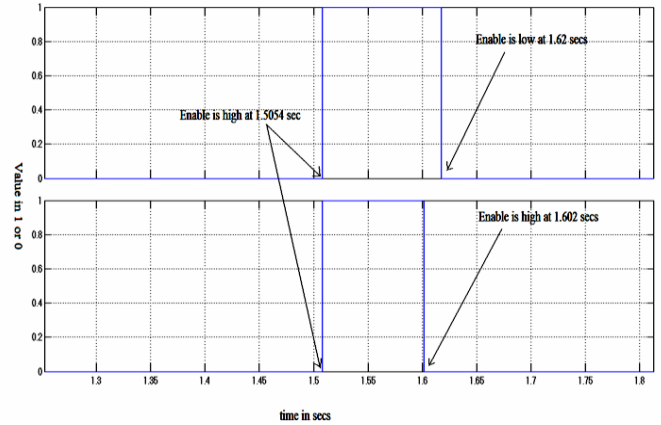


Fig.7 : a)Enable signal termination capability of the method used in[1] and b)proposed method.

It can be clearly observed that the enable signal prolongs up to 1.62 sec using the method in [1] whereas using the proposed sag detection method it is up to 1.602 sec. This will enhance the quality of voltage injection using series inverter which would be discussed in the results part.

G. Modified Technique that Considers Time into account

The integration of $1-C(t)$ term is considered in order to take time into account. There is a need to differentiate between sag and under voltage. Under voltage is for long duration (greater than 1 min) and hence should be taken care by the source. The integrated value of $1-C(t)$ term is compared with the value of $1-C(t)$. Here the unit is designed for voltage compensation only up to 1 sec. Similarly, time limit can be set for 1 min also.

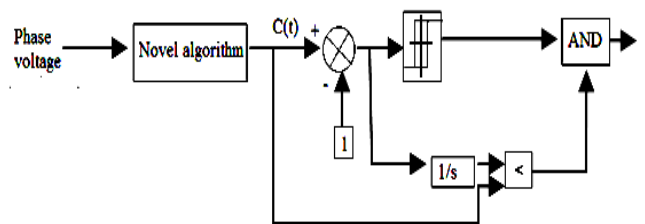


Fig.8: Modified technique considering time of compensation

III. CONTROL OF SHUNT CONVERTER

The shunt converter control includes the extraction of harmonic components and generating the gate pulses to the converter.

The same algorithm used for extraction of reference signals for series convertor is also used for the shunt convertor

control. B (t) signal is harmonic component in p.u. that is to be injected. The B (t) signal is power amplified using shunt converter.

For generating gate pulses for the shunt converter hysteresis current controller [6] which is similar to that of hysteresis voltage controller has been used. The extracted current reference signals are as follows. The gate firing circuit for three phase converter is shown below:

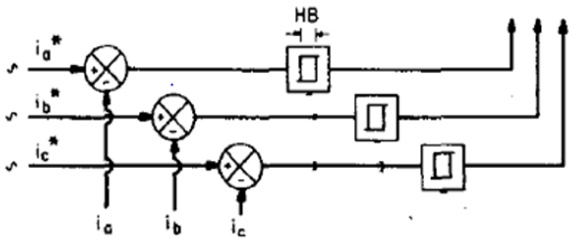


Fig.9: Gate pulse firing circuit for shunt converter

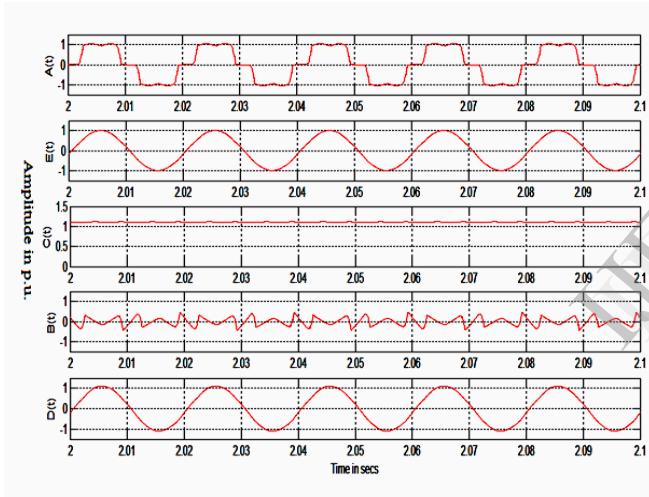


Fig.10: Various extracted components of load current.

IV. SIMULATION RESULTS:

Two test cases are taken,

A. Case.1: operation under normal condition:

Under normal condition, VSC1 is on and VSC2 is off. Due to non-linear load the THD of the supply current is about 25% whereas after the compensation the THD has been improved to 4.15% by the use of hysteresis current control technique. The THD analyses of supply current before and after compensation are given in fig.10. Various harmonic components of load current and source current are given in table 1.

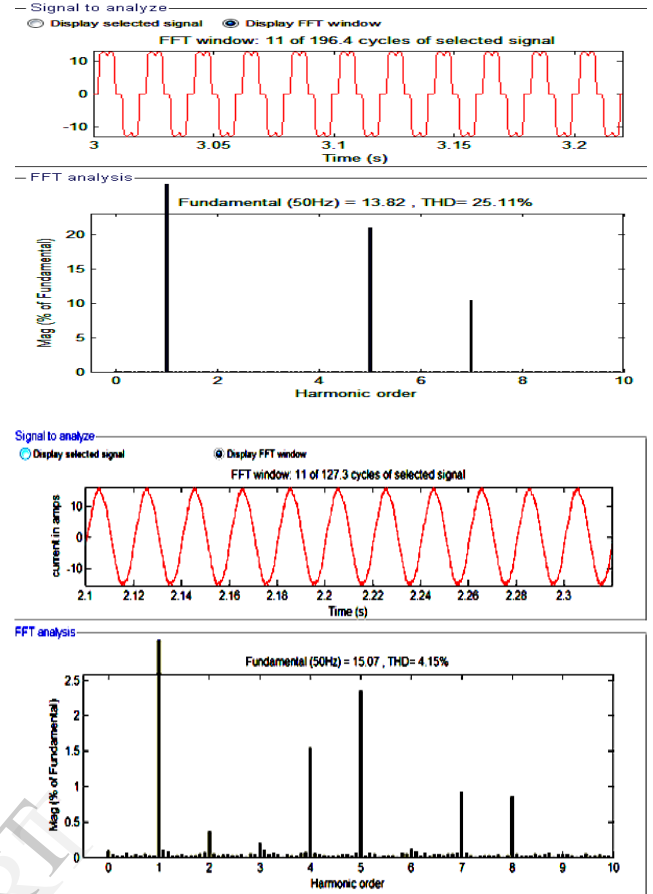


Fig.11: a) The THD analysis of supply current before compensation and b) after compensation.

B. Case.2: Under fault condition

A single phase L-G fault of magnitude 0.25 p.u. is created from 1.5 to 1.6 secs. As soon as the sag occurs, the sag detection technique enables the gate pulses to the inverter. So, both VSC1 and VSC2 are on during this test case. The deficit voltage is injected by series converter as soon as sag is detected as shown in fig.13

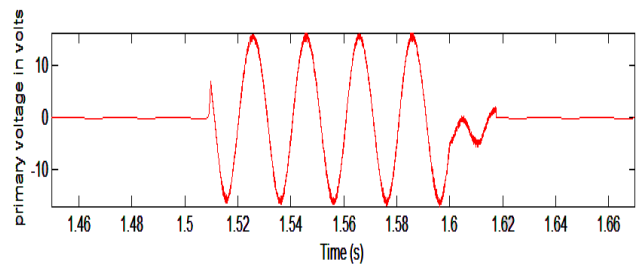


Fig.12: Injected voltage due to proposed sag detection technique in [1].

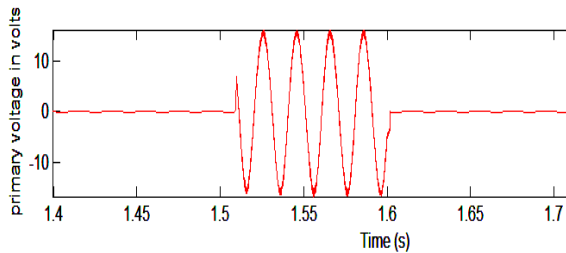


Fig.13: Injected voltage using proposed sag detection and enable termination method.

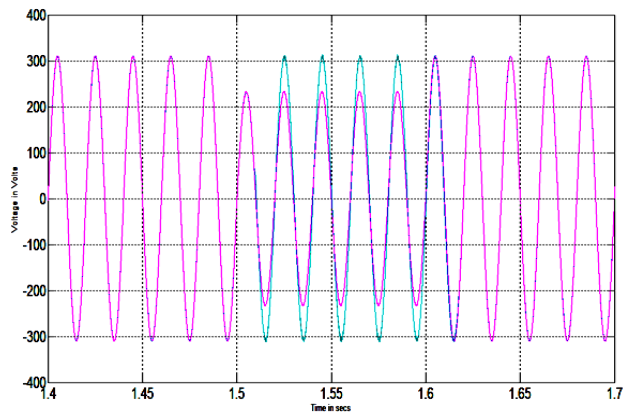


Fig.14: Load voltage and Source Voltage.

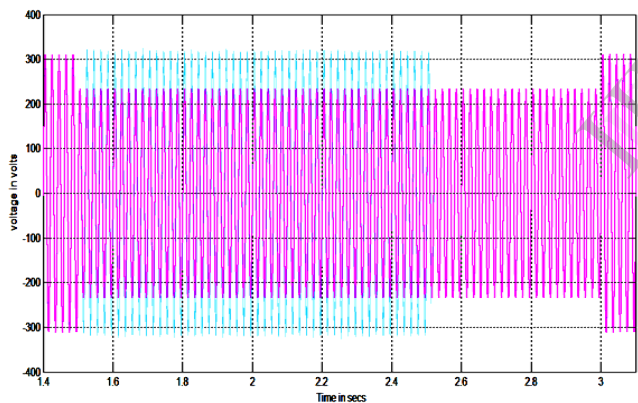


Fig.15: Load Voltage and Source when sag of duration 1.5 secs is created

The extra injection of the voltage as shown in fig.12 due to method in [1] is inappropriate after the sag is terminated. The proposed method however eliminates the inappropriate voltage injected after the termination of sag. That extra voltage can cause unwanted current harmonics in the system.

Along with that a unit that imposes time limit on the compensation is proposed. To check its efficacy a reduction in voltage of 1.5 secs is created. The UPQC is made to compensate for 1 sec only i.e., up to 2.5 secs as shown in fig.15. similarly, time limit on compensation can be set to 1 min.

Table.1: Harmonic components of load current and source current w.r.t fundamental.

THD content of I_L Load current				THD content of I_s Source current			
Order	%	Order	%	Order	%	Order	%
1	100	16	0	1	100	16	0.14
2	0.01	17	2.69	2	0.35	17	1.34
3	0.04	18	0	3	0.42	18	0.09
4	0	19	2	4	1.44	19	0.56
5	20.99	20	0	5	1.68	20	0.26
6	0	21	0.02	6	0.22	21	0.05
7	10.47	22	0	7	1.26	22	0.16
8	0	23	1.15	8	0.87	23	0.91
9	0.04	24	0	9	0.12	24	0.16
10	0	25	0.9	10	0.58	25	0.56
11	6.62	26	0	11	0.14	26	0.17
12	0	27	0.01	12	0.08	27	0.06
13	4.54	28	0	13	0.87	28	0.09
14	0	29	0.71	14	0.11	29	0.69
15	0.03	30	0	15	0.08	30	0.06

VI. CONCLUSION

A novel algorithm based on the enhanced phase locked loop and non-linear adaptive filter is used and analysed in a different and simple manner. The Gate pulses for Open UPQC are generated through hysteresis control technique and the sag detection and enable termination method has been improved and a time limit is imposed on duration of compensation. The THD of the supply current is as low as 4.15%. The load voltage is maintained within in the IEEE standards using Open UPQC.

REFERENCES

- [1] AhmetTeke, lutfuSaribulut and Mehmet Tumay, "A Novel Reference Signal Generation Method for Power Quality Improvement of Unified Power Quality Conditioner", IEEE Transactions on Power Delivery Vol. 26, No.4, pp. 2205-2214, October 2011.
- [2] F. Z. Peng, G. W. Ott, and D. J. Adams, "Harmonic and reactive power compensation based on the generalized instantaneous reactive power theory for three-phase four-wire systems," *IEEE Trans. Power Electron.*, vol. 13, no. 6, pp. 1174-1181, Nov. 1998.
- [3] H. Fujita and H. Akagi, "The unified power quality conditioner: The integration of series and shunt-active filters," *IEEE Trans. Power Electron.*, vol. 13, no. 2, pp. 315-322, Mar. 1998.
- [4] A. Teke, K. Ç. Bayindir, and M. Tümay, "Fast sag/swell detection method for fuzzy logic based dynamic voltage restorer," *Inst. Eng. Technol. Gen., Transm. Distrib.*, vol. 4, no. 1, pp. 1-12, 2009.
- [5] FatihaMekri, Nadia Ait Ahmed, Mohamed Machmoum, BenyounesMazari, "A novel hysteresis voltage control of series active power filter", IREENA (Institut de Recherche en Electrotechnique et Electronique de NantesAtlantique)
- [6] Hirofumi akagi, Yoshihira kanazawa, and Akira nabae, "Instantaneous Reactive Power Compensators Comprising Switching Devices without Energy Storage Components" *IEEE Trans. ON INDUSTRY APPLICATIONS*, IA-20, NO. 3, MAY/JUNE 1984.