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Modeling Method to Develop an AMBA AXI4 Bus Interconnect: A Survey

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***Abstract*—Due to the increased customer demands design complexity of system on chip (SOC) increases day by day. Hence there is always a productivity gap [8].To address this issue various advanced methods are adopted during the design, development and verification phase of any project. It might be developing an Intellectual property (IP), using an automated tool, hardware software co design or using various modeling methodologies [8] at the earlier phase of the project for system level architecture exploration.**

In this paper we are discussing two modeling techniques to develop and verify the Advanced Extensible interface (AXI4) bus interconnect , they are Register Transfer level (RTL) method and Transaction Level modeling (TLM) method. From this analysis we come to the conclusion that using TLM method increases the simulation speed, and reduces the effort due to the availability of open source packages which can support the Transaction Level modeling (TLM) method

Keywords—Register Transfer level (RTL), Transaction Level modeling (TLM), Intellectual property (IP), Advanced Extensible interface (AXI), System On Chip (SOC), Advanced Micro Controller Bus Architecture (AMBA), CORE CONNECT, Result oriented model (ROM), Instruction Set Simulator (ISS), International Business Machine (IBM),s Cycle Aaccurate (CA).

I. INTRODUCTION

Any digital system or hardware test bench or software test bench has many components which are interconnected to meet the required functionality. In order to address the increased productivity gap and the time to market it is necessary to develop and verify these interconnect at the architectural level in a less time at the earlier phase of the project [1].

In the early days standard interconnects like AMBA (Advanced Micro Controller Bus Architecture) from ARM, CORE CONNECT from IBM came into the market to enable the reusability of IP. Of which AMBA from ARM become the most popular due to the availability of wide variety of IPs for this bus architecture. There are various versions of AMBA from AMBA1.0 to AMBA5.0 [9] [2]. AMBA AXI has well through put compared to previous versions [3].

There are various methods of modeling the system or an interconnect to verify the functionality at the architecture level like RTL, cycle accurate (CA), temporal model and TLM model, Result oriented model (ROM). Each has its own disadvantage like, RTL method requires more simulation time, Cycle accurate model cost is more, Result oriented model is platform based. But TLM stands better compared to other modeling methodologies [4].

In Transaction level model [TLM], Transaction is an "object that encompasses the handshakes and the signals which are required to establish the communication between the components or the modules". Here the communication is performed by using the functional calls [fig 2]. All the components of the system are represented in terms of TLM modules. The TLM channels are used to connect different modules. Modules are bound to channels through the TLM ports. The module that requests the transaction is called the TLM master or TLM initiator. And the module which does the requested operation is called the TLM target or TLM slave. Using TLM raises the abstraction level above the RTL. Hence it is placed above the RTL level in the SOC design flow [8].

II. RELATED WORK

Reference [4] describes different modeling methodologies that are adopted in order to address the SOC design complexity by raising an abstraction level. Any modeling methodology that is adopted should satisfy the requirements like

- It should have high simulation speed.
- It should provide acceptable accuracy.

The effort and the time required to develop the model should be less.

Various modeling methodologies like RTL method, Cycle Accurate method (CA) and TLM method are compared in [4]. The RTL method requires more simulation time and modeling time as it involves pin level detail [Fig 1] and also the effort required to develop an RTL model is more. In cycle accurate method non processor parts of the system are simulated using Instruction set simulator (ISS) which uses c language. Hence there is a raise in the abstraction level. But the increase in the simulation speed which is obtained by using this method is very less for the cost that needs to be bared. Also, always it may not be necessary to obtain cycle accurate information. The Fig 3 shows the comparison of different modeling methodologies with respect to simulation speed and the modeling speed. TLM has high simulation speed and modeling speed compared to other modeling methodologies .There are different TLM models like Timed model (timing information is considered) and Untimed model (no timing information is considered).

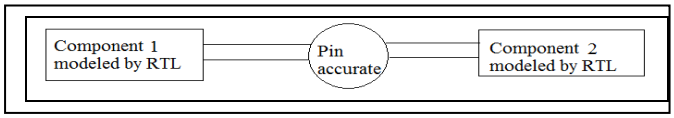

Fig 1: RTL model simulates every event

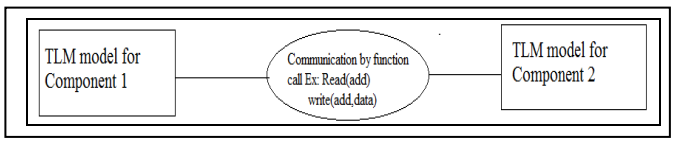

Fig 2: TLM model, Simulation speed higher then RTL

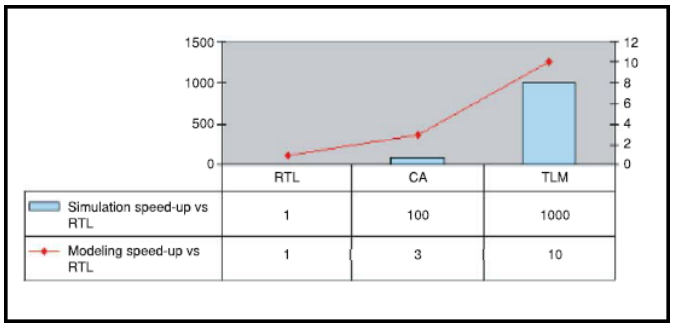

Fig 3: Comparison of various modeling methodologies [4].

Reference [5] simulates AMBA AHB by RTL (Register transfer level) method and TLM (Transaction level modeling) method using System C. And proves that TLM method raises the abstraction level above the RTL, also the simulation speed increases by order of two then RTL. For the same simulation, on the same machine, if a system C 2.0 TLM model requires one day to run, then system C 2.0 RTL model requires 100 days to run.

Reference [5] concludes describing the low level or pin level details while designing a hardware bus communication interface (i.e. using RTL method)

- Makes the process slow.
- Difficult as pin level details are required.
- Probability of error in such a design is more.

Table 1: Comparison of simulation Speed using RTL and TLM model on Sun Ultra 60 for AHB bus [5].

Simulation Speed	RTL Model for AHB bus using System C	TLM Model for AHB bus using System C
Kilo Cycles per Second	3	300

Reference [6] takes R8 processor as an example and does comparison of Transaction level (TLM) modeling approach in System C with that of the Register transfer level (RTL) modeling approach in VHDL. It also compares the RTL modeling method of VHDL with that of the RTL modeling method of System C for R8 processor.

R8 processor is RISC machine. But it misses the important feature of RISC machine that is pipelining. This processor is available as an IP core and is used in many academic based projects.

- It is having load store architecture.
- All instructions are having the same size and contain the information related to the operation code and the operands if present.
- Data bus and the address bus is 16 bit wide.
- There are 16 general purpose registers present in the register bank.
- Only few status flags like zero, carry, overflow and negative are supported.
- 2 to 4 clock cycles are required to execute any instruction.

This processor is implemented as

- Three TLM modules like memory, execution unit and bank of registers.
- Three TLM channels for flags, registers and memory.
- Each of these channels is connected to the module through the port.

Reference [6] concludes that a simulation time for system C TLM model of R8 processor is less compared to RTL model developed in VHDL. Also it concludes that hardware size obtained by using RTL of VHDL and the RTL of system C is the same.

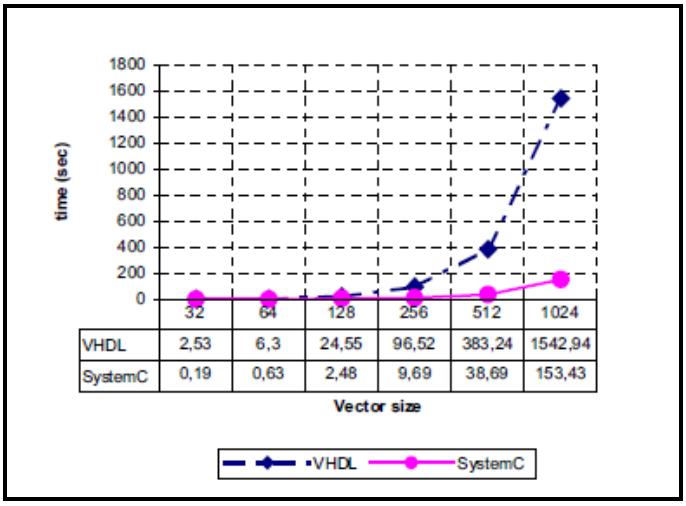

Fig 4: RTL versus TLM simulation time Comparison [6].

Table 2 gives the comparison of RTL and TLM model method.

Table 2: RTL and TLM model method

Parameter	TLM Model	RTL Model
Simulation time	Less time	More time
Using for an application	This technique is fast enough to run an application.	This technique is too slow to run an application.
Implementation detail	No implementation Details involved.	Pin accurate and register accurate details are involved.
Timing information	No timing information involved.	Cycle accurate timing information involved.

Reference [7] contains the open source VHDL verification methodology (OS-VVM) packages that are readily available, which will support Transaction level modeling. Randomly generating the stimulus required and the functional coverage becomes very important features while verifying the system level designs. Standard VHDL supports for all these features. Implementing these features requires good coding skills .Such features are created and are readily available as VHDL packages in the open source VHDL verification methodology forum. OSVVM packages available in this forum can be used by anybody and interested can also contribute to make it better.

Advantages of this methodology are:

- It works with VHDL2002 but is mainly based on VHDL 2008.
- Random generation and functional coverage present here are having advanced features.
- Randomized values also support various distributions like Gaussian and Poisson distribution.
- The Transaction level modeling (TLM) can also be implemented using these packages.
- Reporting features for functional coverage is also been implemented.
- Randomizing the values is done by checking whether all the possibilities are covered or not. This feature is called intelligent randomization.

Following packages are taken from this forum to support the TLM method in this project

- Random package.
- Coverage package.

Random package helps to generate the required data randomly. Coverage package is used to check whether all the data generated by the random package covers all the scenarios or not, So as to ensure the correct functionality of the system. These packages have standard function calls .These calls are used to achieve the transaction level modeling.

CONCLUSION

From the above analysis we can conclude that using TLM technique to develop and verify the bus interconnect i.e. AXI4 is better than the RTL technique [4] [5] [6] [8]. Also the availability of the VHDL open source packages reduces the time and the effort [7].

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REFERENCES

(1) Transaction-based SoC Design Techniques for AMBA AXI4 Bus Interconnects using VHDL (By Daniel C.K. Kho Tauhop Solutions and Kumar Munusamy ,Multimedia University, Faculty of Engineering).
(2) Arm Amba2.0,Amba3.0,Amba4.0 specification document. www.infocenter.arm.com
(3) Comparing AMBA AHB to AXI Bus using System Modeling. (By Deepak Shankar)
(4) TRANSACTION LEVEL MODELING, An Abstraction Beyond RTL. (By Laurent Maillet-Contoz and Frank Ghenassia, STMicroelectronics, France)
(5) M. Caldari, M. Conti, M. Coppola, S. Curaba, L. Pieralisi, and C. Turchetti. ”Transaction-level models for AMBA bus architecture using SystemC 2.0.” Proc. IEEE Conf. Design, Automation and Test in Europe. vol. 2, Mar. 2003.
(6) From VHDL Register Transfer Level to System C Transaction Level Modeling: a Comparative Case Study (By Ney Calazans, Edson Moreno, Fabiano Hessel, Vitor Rosa, Fernando Moraes, Everton Carara Pontifícia Universidade Católica do Rio Grande do Sul [FACIN-PUCRS] Av. Ipiranga, 6681 - Prédio 30 / BLOCO 4 - 90619-900 - Porto Alegre – RS – BRASIL)
(7) J. Lewis. The OS-VVM packages. [Online http://osvvm.org/].
(8) Analysis and Optimization of Transaction Level Models for Multi-Processor System-on-Chip Design (By Hans Gunar Schirner, UNIVERSITY OF CALIFORNIA).
(9) http://en.wikipedia.org/wiki/Advanced_Microcontroller_Bus_Architecture