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Modeling of Power Planes for Improving EMC in High Speed Medical System

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***Abstract*— Electromagnetic compatibility (EMC) is an important parameter in medical systems. Multilayer printed circuit board (PCB) itself injects switching noise in the board, which is the main cause of decrease in the EMC performance of medical instruments. Medical instruments are very sensitive to any noise and the output of the instrument may change because of it. In addition, common mode (CM) current and leakage current also cause problems in design of medical electronic devices. In this work, better EMC is achieved by using plane layers as an inbuilt capacitor in a multilayer PCB of medical devices. Suppression of electromagnetic interference (EMI) effect at the component and printed circuit board level is very difficult for most of the medical applications, but using the power plane coupling method at the front end of the design cycle, eliminates many EMC problems. The inbuilt interplane capacitance between the plane layers reduces the harmonics in PCB at the rate of 5dB to 28dB.**

Keywords*— Electromagnetic compatibility, electromagnetic interference, printed circuit board and signal integrity.

I. INTRODUCTION

The design technology of biomedical systems for both EMC compliance and functionality has advanced to a state where current board design techniques are becoming less effective. All EMC problems begin and end with electronic circuitry. Suppression of EMI at the component and PCB level is nearly impossible for most of the medical applications [1]. In complex equipment, it may not be possible to protect the entire system. Analog circuit performance is often affected adversely by high frequency signals in the PCB [2]. Medical equipment containing analog circuitry may also adversely affect the systems. Medical devices are affected by EMI for many reasons, including electrostatic discharge, power line disturbances and ground plane bouncing. The signal integrity (SI) problems occur in the PCB level due to signal frequency increase in the PCB. PCBs and undesired electromagnetic emissions (EM) represent one of the most critical issues to be accounted for in electronic system design. The sizes are getting smaller and smaller and the signal speed increases, which results in severe EMC problems. EM fields radiated by high speed signal traces can cause both narrow and broadband interference with nearby electronic equipment.

EMI is a major problem in modern electronic circuits. In order to reduce the interference in any electronic system, either remove the source of the interference or protect the circuit being affected [3]. Although, the circuit may be working at the board level, it may be radiating noise to other parts of the circuit, causing problems at the system level. Emissions from any digital circuit are normally of higher frequency, which are coming from the harmonics produced by the high-frequency signals in PCB [4]. The fast switching current flows in loops, which act as small antennas in the PCB, radiate magnetic fields known as differential-mode radiation [5]. A major EMC problem occurs when there are discontinuities in the current return path. These discontinuities cause the return current to flow in larger loops, which increases the radiation from the board, as well as, increases the crosstalk between adjacent traces and causes waveform distortion [6].

II. POWER PLANE MODELING

Multilayer PCBs have a power and ground plane distributed network to enhance the overall performance of system operation. The plane layers provide a low impedance path [7]. A low impedance path allows the minimum amount of voltage drop across the power supply of components. If an imbalance exists within the power distribution network, the common mode RF energy is developed [8]. The physical relationships of plane layers separated by a dielectric core create a large capacitor [9]. Depending on the thickness of the core material and the dielectric constant in layer stack up, various values of interplane capacitances are created. By taking advantage of the interplane capacitance between the power and the ground planes of a PCB, EMC of the system is improved. The increase in interplane capacitance is achieved either by reducing the layer spacing or by increasing the dielectric constant of the PCB material [10]. The value of PCB capacitance is estimated by $C = \varepsilon A/S$, where ε is the dielectric constant, S is the spacing between plane layers, and A the effective area of the planes.

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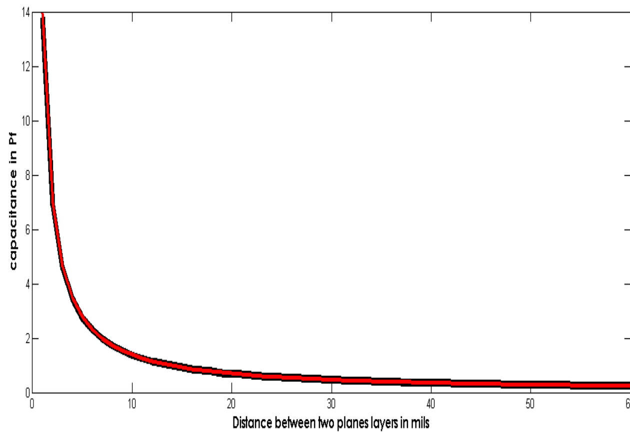

Figure 1 Interlayer plane capacitance varies with respect to dielectric thickness between two plane layers.

Figure 1 shows that decreasing the layer spacing between the power layers results in an increased effective interplane capacitance. If the dielectric constant of the PCB material is increased, it results in an increase in the interplane capacitance [11]. Power and ground planes have very small inductance which is utilized during return current path [12].

III. METHODOLOGY

In the present study, two different 4 layer stack up boards have been analyzed for EMC performance in the PCB. In the first case, Figure 2 shows a standard 4 layer stack up, 5 x 4 inch FR4 PCB with 62 mil board thickness which is used in most of the medical products.

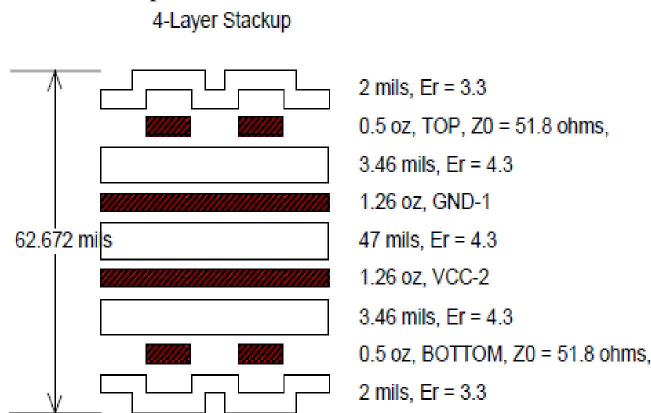

Figure 2 Standard 4 layer stack up with 63 mil board finishing

Top and bottom layer core thickness is 3.46 mil and the plane layers are separated by a 47 mil dielectric core. In the standard board, the power and ground plane coupling is very weak due to thick dielectric core layer between the plane layers. Effectively, the plane capacitance value is very small between the plane layers. Figure 3 shows the proposed 4 layer stackup board, the inter layer capacitance is increased by changing the PCB thickness of 62 mil to 30.5 mil. The dielectric core thickness, 3 mils is also decreased between the plane layers.

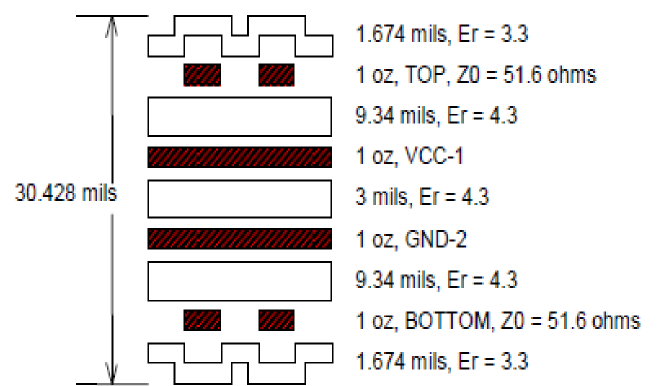

Figure 3 Proposed 4 layer stack up with 32 mil board finishing

Adjacent pair of ground and power plane layers in a PCB's layer stack up provide an intrinsic, distributed capacitance that still behaves like a capacitor up to GHz range.

The characteristic impedance of the plane layer is calculated by using the equation, $Z0=1/2\pi fC$. The characteristic impedance depends upon the interplane capacitance between the ground and the power layers. The interplane capacitance also depends upon the core thickness between the power plane layers. Figure 4 shows that the impedance of the power plane layer decreases with the increase in the signal frequency at different dielectric thickness values, i.e. 5 mil, 10 mil, and 50 mil. In a normal 4 layer stack up, plane impedance is higher than the proposed layer stack up PCB.

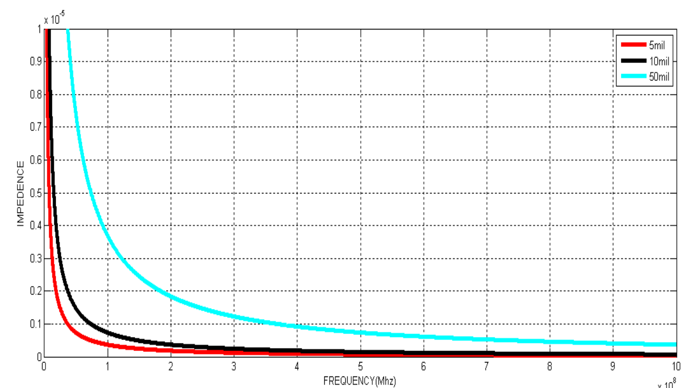

Figure 4 Impedance of power plane layer change with frequency.

If a noise source is placed near to instrument system, it affects the performance of the system. Electronic equipment is constantly evolving, there is always a possibility of interference in medical equipment from mobile communications devices like cell phone, walkie talkie and other radio devices. The electric field intensity of any radio device or system measured in "volts/meter". Transmitter powers of the communication device can calculate distance from the antenna by using formulae:

$$E\ (V/m) = 5.5\ \sqrt{PA}/d$$

where *P* is transmitter power (watts), *A is* antenna gain and *d* is the distance from the antenna (meters). The electric field from a 1-W radio with a zero gain antenna at 1 m is about 8 V/m, while the electric field from a 5W Walike Talkie at 1 m

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is about 12 V/m. Most unprotected equipment can fall in 0.01 to 1.5 V/m range.

IV. SIMULATION RESULTS AND DISCUSSION

Figure 5 (a) and 5 (b) shows the EMC simulation results of the standard and proposed 4 layer stack up boards. In Figure 5 (a) harmonic at 500 MHz, 750 MHz, and 1 GHz frequency is 50dB. When the dielectric thickness between power and ground plane is 47 mil, the interplane capacitance is small across plane layers. This layer stack up is less effective for EMC product. Figure 5 (b) shows that when dielectric core thickness is 3 mil between the plane layers, the harmonic is reduced at the rate of 15dB to 25dB. Plane capacitor is directly proportional to dielectric core thickness between power plane layers.

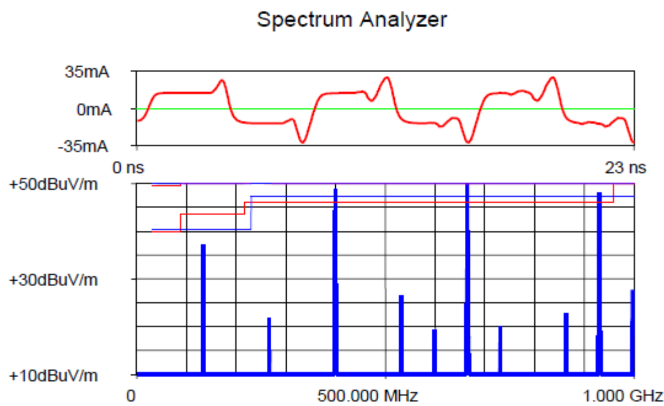

Figure 5 (a) EMC simulation for standard 4 layer PCB

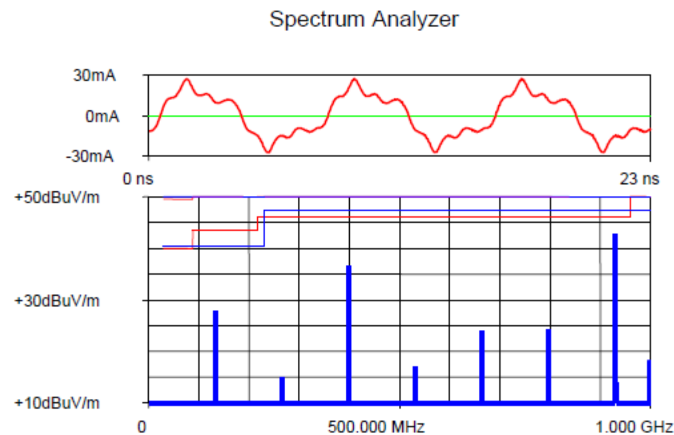

Figure 5 (b) EMC simulation for proposed 4layer PCB

Figure 6 (a) shows the measurement setup for the standard as well as the proposed boards and Figure 6 (b) compares the oscilloscope waveform for both the boards when a Walkie-Talkie radio system is put at a distance of less than 1 meter from the boards. The signal waveshape at receiver end is degrading due to noise source to change the shape of the signal in the PCB. The current waveshape is also affected by radio system to reduce the EMC of the system. This system is less sustainable if EMI source is close to the system. On the other hand, the signal waveshape is less affected in the proposed board. The EMC performance of the system is thus improved.

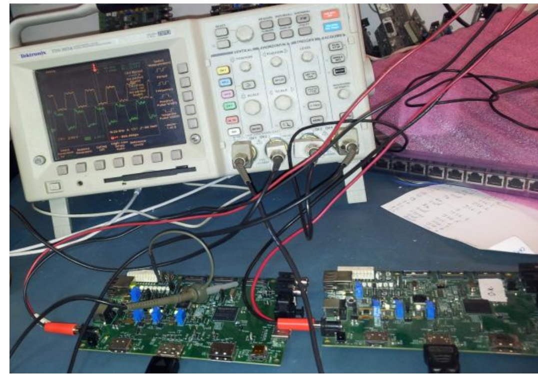

Figure 6(a) Real Meaurement setup for standard and proposed boards

Figure 6 (b) comparision of the waveshapes, yellow waveshape(upper) represent for proposed board and green (lower) for standard board.

EMC of the system is further improved by using two sets of power and ground planes with different dielectric spacing between the planes layers, the multiple inbuilt capacitors build internal in the PCB.

Figure 7 (a) shows the 6-layer stack up with two sets of power and ground plane layers and Figure 7 (b) shows the simulation result where less harmonic is generated; reduced by 18dB to 28 dB at different frequencies. The improvement in EMC by using the proposed 4 and 6 layer stack up boards, which radiates less emission at different frequencies as compared to the standard 4 layer stackup board, are shown in Table 1.

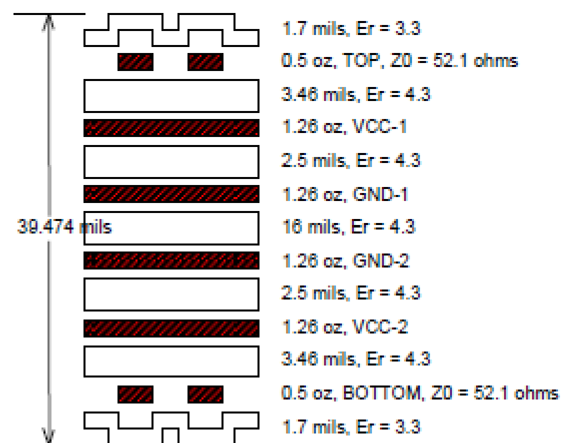

Figure 7(a) 6 layers stack up with two sets of power and ground planes

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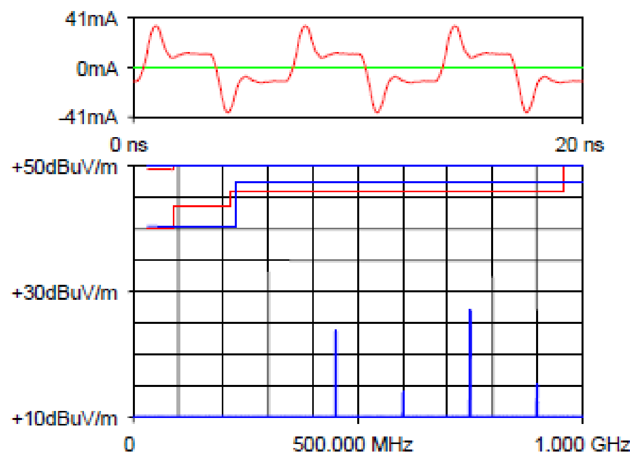

Figure 7(b) EMC simulation for 6 layers PCB

Table 1 Comparison of the emission level at different frequencies for standard 4 layer, proposed 4 and 6 layer boards.

S.No.	Frequency (MHz)	Standard 4 layer	Proposed 4layer	Proposed 6 layer
		Emission (µV/m)		
1	130.863	1.404971	0.47302	0.125017
2	131.478	4.569807	1.538881	0.406706
3	132.094	60.591801	20.407991	5.393551
4	132.710	72.415909	24.3944	6.447174
5	265.112	12.179284	5.593587	0.869591
6	331.621	3.002558	0.496251	0.214614
7	395.667	4.732378	2.207284	0.61995
8	396.283	9.12237	5.855924	1.195979
9	397.515	165.14473	67.2668	21.680374
10	399.362	10.185191	1.258397	1.339113
11	531.148	14.076144	4.862829	0.798772
12	664.166	101.266724	3.40705	3.342648
13	927.123	7.970347	9.606318	2.097764
14	930.202	20.774591	11.363628	2.48249

V. CONCLUSION

Development of a quality medical product design for better EMC takes advantage of the interplane capacitance in the PCB. The result shows that when using thin (3 mil) core between plane layers, the harmonic is reduced at the rate of 15dB to 25dB; whereas using two sets of power plane layers reduces the harmonics further by 5dB to 28dB at different frequencies. At higher frequencies, the interplane capacitance is more effective due to the inductance of the track to the discrete capacitor, which limits the amount of charge supply of very short time. Use of power planes as a decoupling capacitor helps in reducing the RF energy in high frequency signals. By minimizing the board resonances using decoupling capacitors and a proper power and ground plane design reduce radiated emissions that cause EMI in PCB. The result shows that EMC of any medical system is further improved by using two sets of power and ground plane layers in a multilayer PCB.

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