Modified Full Adder Architecture For Area Efficient Carry Select Adder

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Abstract— Area, power and delay are the three parameters of interest when designing any digital system. Often altering one of the parameter always results in the modification of other two parameters in a negative way. Say if area is to be reduced then either the power increases or the delay increases. Optimization happens when the extent of this modification is less when compared to the improvisation of our parameter of interest. This paper presents a similar approach in improvising the performance of the square root carry select adder (SQRT CSA) where the number of gates is reduced at a little cost of increasing the delay. The paper also address the slight increase in delay by improvising the performance of full adder cells used within SQRT CSA. The SQRT CSA is simulated with Modelsim 6.3f and synthesized with Xilinx ISE-8.1 which shows that the proposed carry select adder outperforms its counterparts exhibiting less number of gates and reduced delay.

Keywords **— Carry select adder, Low power, 1-bit adder, critical path.**

I. INTRODUCTION

A carry-select adder is a logic element that computes the n+1 bit sum of two n bit numbers. The carry-select adder generally consists of two ripple carry adders and a multiplexer. Adding two n-bit numbers with a carry-select adder is done with two adders (therefore two ripple carry adders) in order to perform the calculation twice, one time with the assumption of the carry being zero and the other assuming one. After the two results are calculated, the correct sum, as well as the correct carry, is then selected with the multiplexer once the correct carry is known. Therefore the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input Cin =0 and Cin =1, then the final sum and carry are selected by the multiplexers (mux). The basic idea of this work is to eliminate RCA with Cin = 1 and instead add a bit to the result obtained from RCA with Cin = 0 in the regular. The main advantage of this logic comes from the lesser number of logic gates than the n–bit Full Adder (FA)

structure. The increased delay is compensated by modifying the internal structure of full adder cell by using the carry signal as the select signal instead of the XOR signal used in existing SQRT CSA's.

This brief is structured as follows. Section II deals with the delay and area evaluation methodology of the basic adder blocks and also presents the internal logic structure adopted as standard in previous papers for designing a full-adder cell. Section III presents the detailed structure and the function of the BEC logic and introduces the alternative internal logic structure of full adder cells. Section IV reviews the results obtained from the simulations. Finally, the work is concluded in Section VI.

I. EXISTING FULL ADDER OPTIMIZATION

A. Gate Count And Delay Of Basic Carry Select Adder

The delay and area evaluation methodology considers all gates to be made up of AND, OR, and Inverter, each having delay equal to 1 unit and area equal to 1 unit. We then add up the number of gates in the longest path of a logic block that contributes to the maximum delay. The area evaluation is done by counting the total number of AOI gates required for each logic block. Based on this approach, the CSLA adder blocks of 2:1 mux, Half Adder (HA), and FA are evaluated and listed in Table I.

TABLE I
DELAY AND AREA COUNT OF THE BASIC BOCKS OF CSLA

Adder blocks	Delay	Area
XOR	3	3
2:1 Mux	3	4
Half Adder	3	6
Full Adder	6	13

The structure of the 16-b regular SQRT CSLA is shown in Fig. 1. It has five groups of different size RCA. The delay
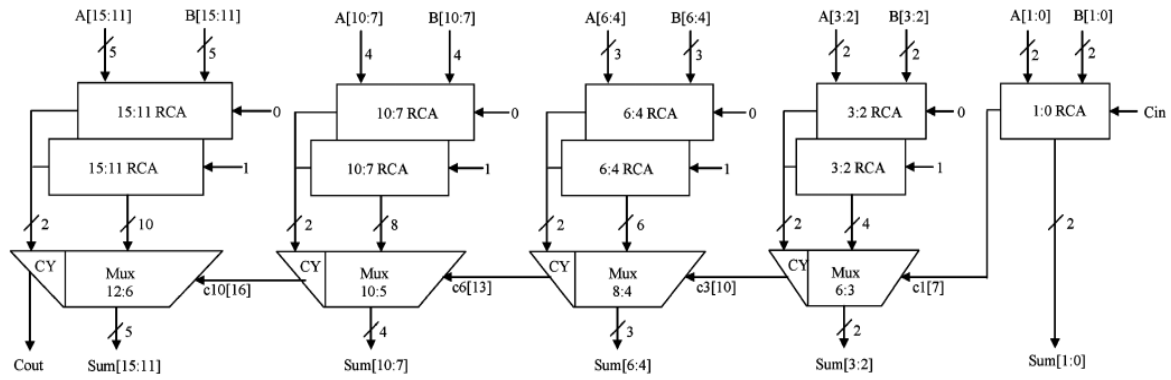
Fig. 1. Regular carry select adder

and area evaluation of group 3 is shown in Figure 2, in which the numerals within [] specify the delay values.
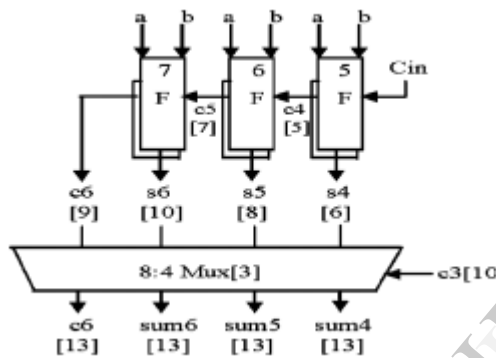

Fig. 2. Delay in Group 3

1) Group 3 has 3 sets of 2-b RCA. Based on the consideration of delay values of Table I, the arrival time of selection input c3[time(t) = 10] of 8:4 mux is later than s4[t=6], s5[t=8] and c6[t=9]. Thus, sum4[t=13] is summation of c3 and mux[t=3].

2) Except for group 2, the arrival time of mux selection input is always greater than the arrival time of data outputs from the RCA's.

3) The one set of 3-b RCA in group 3 has 3 FA for Cin=1 and the other set has 2 FA and 1 HA for Cin = 0. Based on the area count of Table I, the total number of gate counts in Group 3 is determined as follows

Full Adder = 13 * 5 = 65
Half Adder = 6 * 1 = 6
Mux   = 4 * 4 = 16

Total Gate count   = 87
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4) Similarly, the estimated maximum delay and area of the other groups in the regular SQRT CSLA are evaluated and listed in Table II.

TABLE II
DELAY AND AREA COUNT OF REGULAR SQRT CSLA GROUPS

Group	Delay	Gate Count
Group 2	11	57
Group 3	13	87
Group 4	16	117
Group 5	19	147

B. Previous Full Adder Optimizations

The internal logic structure shown in Fig. 3 has been adopted as the standard configuration in most of the enhancements developed for the 1-bit full-adder module. In this configuration, the adder module is formed by three main logical blocks: a XOR-XNOR gate to obtain $A \oplus B$ and $\overline{A \oplus B}$ (Block 1), and XOR blocks or multiplexers to obtain the SUM (So) and CARRY (Co) outputs (Blocks 2 and 3).
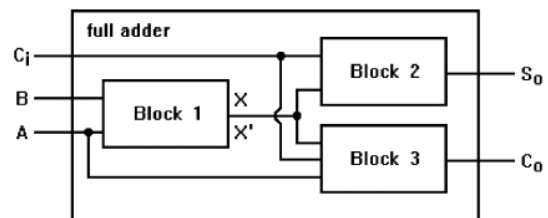

Fig. 3. Full adder with 3 main blocks

The major problem regarding the propagation delay for a full-adder built with this logic structure is that it is necessary to obtain an intermediate $A \oplus B$ signal and its complement,
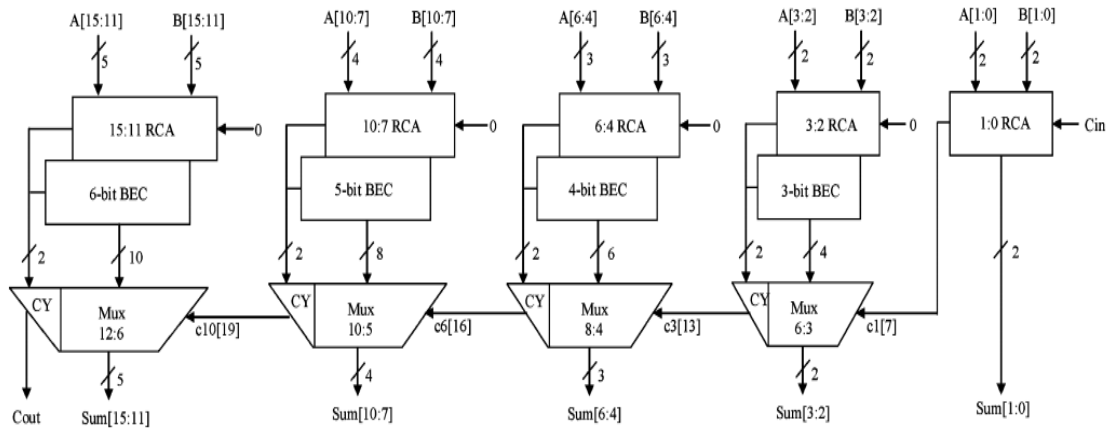
Fig. 4. Modified 16-b SQRT CSLA. The parallel RCA with Cin = 1 is replaced with BEC

which are then used to drive other blocks to generate the final outputs. Thus, the overall propagation delay and, in most of the cases, the power consumption of the full-adder depend on the delay and voltage swing of the signal $A \oplus B$ and its complement generated within the cell. So, to increase the operational speed of the full-adder, it is necessary to develop a new logic structure that does not require the generation of intermediate signals to control the selection or transmission of other signals located on the critical path.

II. PROPOSED CARRY SELECT ADDER

The structure of the proposed 16-b SQRT CSLA uses addition by 1 bit to the result obtained from RCA with Cin=0. We again split the structure into five groups. The delay and area estimation of each group 3 is shown in Fig. 4.

1) 1) The group 3 has one 3-b RCA which has 2 FA and 1 HA for Cin =0. Instead of another 3-b RCA addition by one logic is used to the output from 3-b RCA with Cin=0.

2) The arrival time of selection input c3[time(t)=13] of 8:4 mux is later than the s4[t=4] and s5[t=9] and c6[t=12]. Thus, the sum4, sum5, sum6 and final carry c6 (output from mux) depends on the arrival time of mux selection input and the mux delay.
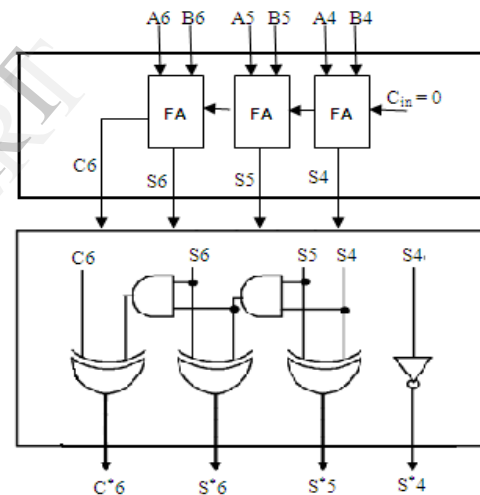

Fig. 5. Addition by 1 bit to the result of RCA with Cin =0

3) The area count of group 3 is determined as follows:

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Full adder  = 13*2  = 26
Half adder  = 6*1   = 6
And         = 1*2   = 2
Not         = 1*1   = 1
Xor         = 5*3   = 15
Mux         = 4*4   = 16
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Total                = 61
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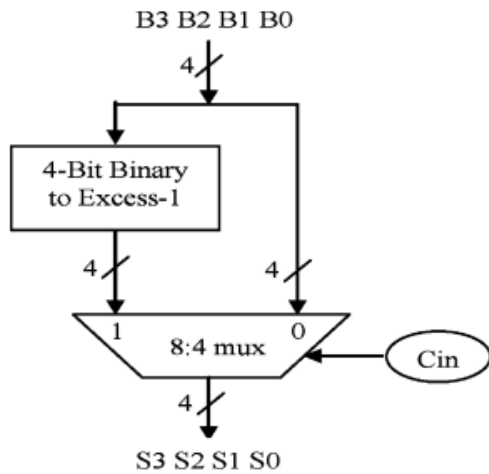
Fig. 7. 4-b BEC with 8:4 mux.

Fig. 6. Alternative logic scheme for designing full-adder cells

3) Similarly, the estimated maximum delay and area of the other groups of the modified SQRT CSLA are evaluated and listed in Table IV. Comparing Tables III and IV, it is clear that the proposed modified SQRT CSLA saves 113 gate areas than the regular SQRT CSLA, with only 11 increases in gate delays.
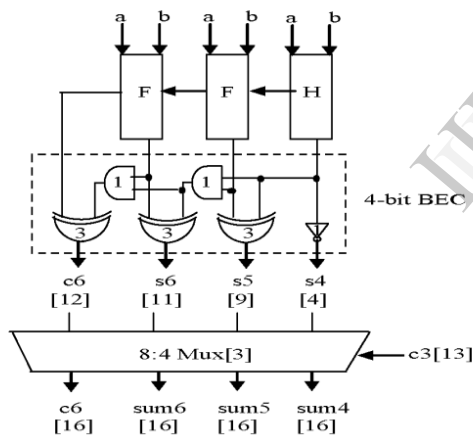
Fig. 8. Delay and area evaluation of group 3 of modified SQRT CSLA

TABLE III
DELAY AND AREA COUNT OF MODIFIED SQRT CSLA

Group	Delay	Gate Count
Group 2	13	43
Group 3	16	61
Group 4	19	84
Group 5	22	107

Examining the full-adder's true-table in Table I, it can be seen that when $Cin = 0$, the sum output is equal to the value $A \oplus B$ and carry is A.B and when Cin=1, the sum is equal to $\overline{A \oplus B}$ and carry is A+B. Thus, a
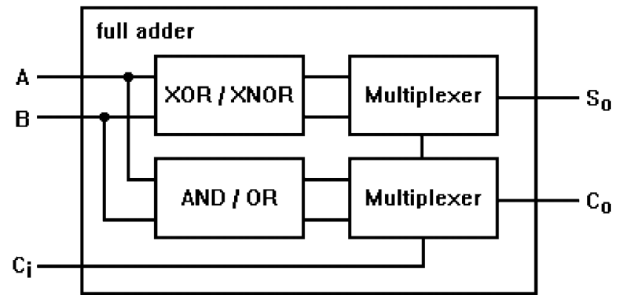
multiplexer can be used to obtain the respective value taking the C input as the selection signal. Hence, an alternative logic scheme to design a full-adder cell can be formed by a logic block to obtain the $A \oplus B$ and $\overline{A \oplus B}$ signals, another block to obtain the A.B and A+B signals, and two multiplexers being driven by the carry input to generate the So and Co outputs, as shown in Fig. 8. The features and advantages of this logic structure are as follows.

• There are not signals generated internally that control the selection of the output multiplexers. Instead, the input signal, exhibiting a full voltage swing and no extra delay, is used to drive the multiplexers, reducing so the overall propagation delays.

• The capacitive load for the input has been reduced.

• The propagation delay for the So and Co outputs can be tuned up individually by adjusting the XOR/XNOR and the AND/OR gates.

Thus the full-adders implemented in SQRT CSA have been designed using DPL logic styles to build the XOR/XNOR gates, and a pass-transistor based multiplexer to obtain the So output as shown in Fig. 8

III. SIMULATION RESULTS

In an effort to provide guidance to their users, Field Programmable Gate Array (FPGA) manufacturers, including Xilinx, describe the capacity of FPGA devices in terms of "gate counts." "Gate counting" involves measuring logic capacity in terms of the number of 2-input NAND gates that would be required to implement the same number and type of logic functions. The resulting capacity estimates allow users to compare the relative capacity of different Xilinx FPGA devices. Hence Gate count metric is used in this paper to compare the regular and improvised Full adder designs.

TABLE IV
COMPARISON BETWEEN EXISTING AND MODIFIED
CARRY SELECT ADDER

Scheme	Power(µW)	Gate Count
Regular full adder	184	8149
Improvised full adder	124	6344

The existing method was simulated in ModelSim SE6.3f for logic verification and the waveform of both standard and modified carry select adder is obtained. It is synthesized using Xilinx ISE 8.1i which shows power consumption and area.

The output of the existing Carry Select adder for the given binary inputs is simulated using Modelsim software and the results of performance comparison is shown for sixteen bit A and B inputs.

It can be seen that the number of gates used in the modified carry select adder is just 8149 gates as opposed to the 6344 gates used by the existing carry select adder. This large number of reduction in the number of gates shows a substantial decrease in the area and the overall area of the chip.

To obtain the power report for comparison purpose of Full Adders we use the Xilinx ISE 8.1i software. The table shows power savings up to 32.6% and area reduction of 28.45% with the same functionality.

IV. CONCLUSION

This paper presents an approach in increasing the performance of the square root carry select adder (SQRT CSA) by reducing the power and power consumption. The extra delay incurred is addressed by improvising the performance of full adder cells used within SQRT CSA. The proposed method shows power savings up to 32.6% and area reduction of 28.45% with the same functionality. The modified CSLA architecture is there-fore, low area, low power, simple and efficient for VLSI hardware implementation.

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