Multi Input Direct DC–AC Converter With High-Frequency Link For Clean Power-Generation Systems

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Abstract:- **This paper proposes a new topology for bidirectional multiinput direct dc–ac converter for clean-power-generation system, therefore, at the input port, a boost converter is used to meet the requirement of many distributed generation systems, such as photovoltaic, and fuel cell systems. The boost converter can increase the dc input voltage. This point results in a turn ratio reduction of high-frequency isolating link transformer. Furthermore, the boost inductor reduces the input current ripple, therefore, the saturation of the transformer can be avoided for higher output currents. The count of used devices has been reduced in the proposed converter. As a result, the cost, size, and the volume of the converter can be reduced. The reduced conversion steps increase the efficiency of the converter. The converter is analyzed step by step to show the principles of the operation in providing energy management based on duty-cycle variations. The system capability in different operation conditions has been simulated, and the simulation results have been compared with measurement results. Dynamic analysis and control design of the bidirectional dc–ac converter is presented based on nonlinear control by input–output feedback linearization.**

Index terms—*Index Terms—***Clean power generation (CPG), dc–ac converter, distributed generation (DG) interface, high-frequency isolating link (HFIL), input–output feedback linearization (IOL), multiinput converter, steady-state analysis..**

I. INTRODUCTION

Now a days   clean power-generation (CPG) systems play a significant role in providing reconciliation between development and environment. CPG systems are significantly investigated and developed to meet the requirements of distributed generatio n (DG) systems. Therefore, power electronic conversion (PEC) systems have been considered as an essential part of the DG systems. They should be studied and developed further to manage the generated energy of DG systems. have been used in photovoltaic (PV) [1], hybrid electric vehicles [2] and [3], fuel cell (FC) [4], and uninterruptible power supplies systems [5]. In many of these applications, dc–ac or dc–dc power electronic converter (PEC) system with a highfrequency link and galvanic isolation can be used to eliminate the dc link capacitor and the bulky power frequency (50 or 60 Hz) transformer [1], [6]–[9]. This solution offers high conversion efficiency due to the reduced conversion steps, a compact

size, small weight, and low cost converter. In addition, an integrated dc–ac or dc–dc PEC system contains a multiinput port to accommodate diverse DG sources along with /energy storage systems (ESSs). Therefore, bi-directional-power-flowcapability

for the ports connecting to ESSs is necessary. The series resonant dc–dc converters are mainly proposed for their capabilities to achieve soft switching, high-frequency operation, and highest efficiency [10], [11]. A three-port series-resonant converter operating at constant switching frequency has been proposed in [12], which offers a wide selection range for inductances and the switching frequencies. Although, it is possible to obtain soft switching, but higher conduction losses may occur due to the high current amplitude in the converter. In addition, the existence of one or more resonant loops can lead to increased complexity in converter design.

As a result, the control strategy and the stability analysis of the converter are much more complex in comparison to those that use leakage inductance to transfer power in both directions. A direct dc–ac converter with a high-frequency link has been proposed in [13]. This converter contains a boost converter accompanied by a dc link capacitor. In this converter, high conversion efficiency may be reduced due to the existence of the dc link capacitor and considerable number of conversion steps. In [14], a multiple-input hybrid energy-conversion topology has been proposed that can manage energy among different sources with different voltage/current characteristics, while achieving low parts number and bidirectional energy conversion.

This converter has not any highfrequency isolating link (HFIL), and hence, no safety is provided for domestic or hybrid electric vehicles applications. Also, the converter has high current peaks, which lead to high conduction losses. An attempt to minimize the total number of components in multipleinput dc–dc converters has been presented in [15].

But neither bi-directional-power-flow capability, nor isolation is provided. Similarly, multiple-energy source-conversion topologies have been presented in [16]. Although, the topology is capable of interfacing sources of different voltage/current characteristics to a common load and achieving a low part count, the
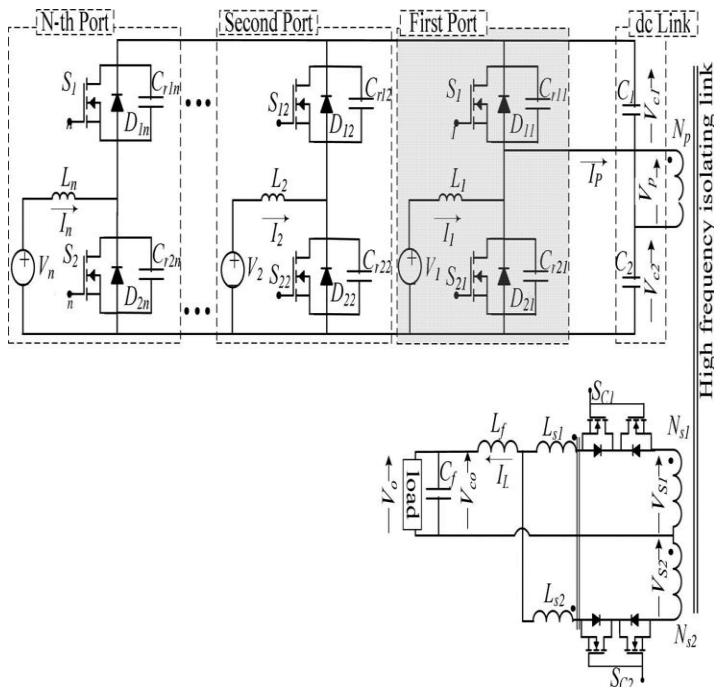
reverse-blocking diodes only allow unidirectional power flow, and this topology can not be used for ESSs and bidirectional power flow are needed. Multiple port, bidirectional converter topologies that may be suitable for the CPG systems can be found in the literature [17]–[19]. Suitable interface circuit for a hybrid FC/battery system to control the power flow is shown in [17], [18], but this three-port bidirectional converter need separate transformer winding for each port. Whereas, in paper [19], a three-port bidirectional converter is used one transformer winding for two input ports, but this topology can be used only for two CPGs.

In this paper, a multiinput port bidirectional dc–ac converter is proposed, which consists of high-frequency boost converters, an HFIL transformer, and a cycloconverter at the secondary side of high-frequency isolating transformer (HFIT). This topology uses only one transformer windings for all input ports. The analysis of the proposed system to manage power flow under different operation conditions is carried out, and simulation and experimental results have been compared. Dynamic analysis based on input–output feedback linearization (IOL) for a bidirectional dc–ac converter is presented too. The experimental results of a prototype, which is a two-input-port converter with low-voltage application, i.e., 110 V–60 Hz, has been provided to confirm the theoretical analysis.

II. PROPOSED CONVERTER TOPOLOGY

Multiinput dc–dc or dc–ac converters are used to combine different types of energy sources to obtain a regulated dc or ac voltages [9]–[12]. They have become popular due to increasing applications in CPGs, such as PV systems, FC, systems, and wind turbines. Fig. 1 illustrates the power-circuit diagram of the proposed multiinput direct dc–ac converter. In the proposed topology, DG systems with dc output like PV and FC, and ESSs

like batteries can be co nnected to the input ports. The converter is composed of half-bridge inverters, HFIL transformer, and cycloconverter. At the input side, the structure is modular and each input port contains a boost half-bridge inverter and a dc voltage source. The boost half-bridge inverters provide bidirectional power flow as well as increase the input voltage level, Increasing this voltage results in a reduction of input current ripple and the turn ratio of the transformer. At least one of the dc voltage sources (e.g., second port) should have an ESS to provide energy management in the proposed converter for the generation systems, such as FC. The HFIL transformer has three windings. The dc capacitors (i.e., C_1 and C_2) provide a dc link, and the voltage of them remains constant in all operation conditions, as discussed in Section III. Thus, the input ports can have different input voltages and operate independently. Therefore, an input port can be added or omitted from the system. The cycloconverter consist of two bidirectional switches S_{c1} and S_{c2}, which are in series with a snubber coupled-inductor L_{s1} and L_{s2}, respectively. The snubber inductors (L_{s1} = L_{s2}) play a significant role in reducing the switching stress of the cycloconverter. If the switch S_{c1} is on, it cannot be off unless S_{c2} starts to conduct, i.e., there is an overlapping switching interval considering the continuity of inductive current. In the case of the condition of both switches, the inductive current changes its path smoothly from one (which starts blocking) to another (which starts conducting). Therefore, soft switching is obtained for both switches at turn-ON and turn-OFF conditions. The output inductor L_f reduces the high frequency components of the cycloconverter voltage and cooperate with the output capacitor C_f as an low-pass filter. The other features of the proposed converter are given as follows.

1) The main input port (e.g., first port) works with a duty cycle equal to 50%, but the duty cycle of the other port is dependent upon the required current.
2) It is possible to draw power from all the input ports at the same time.
3) The gate-control signals between each input port are shifted 180° to achieve minimum current ripple for the dc link and small-size capacitors.
4) Compared to other topologies, in this circuit, dc voltage is converted to an ac one directly.
5) The voltage of the dc capacitors is regulated with the first input port, and adding or disconnecting of the other ports has no effect on the voltage of dc capacitors (i.e. C_1 and C_2).
6) The electric isolation is implemented with an HFIL transformer that has three functions in this paper:
   a) providing the electrical isolation between input ports and output port;
   b) stepping up the voltage; and
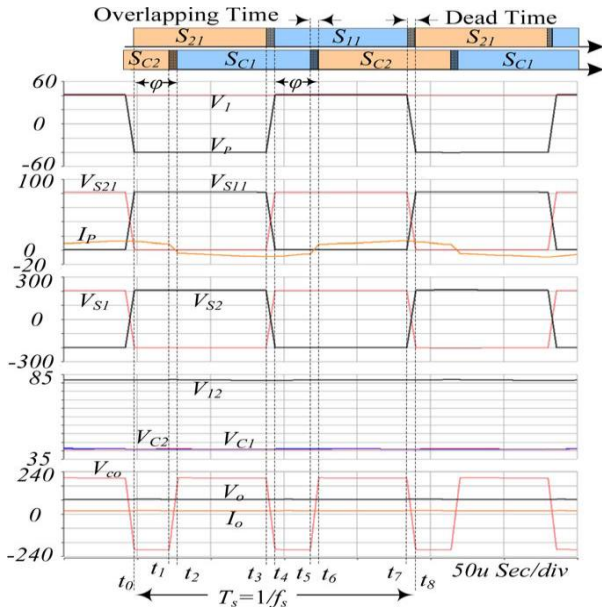   c) reducing the size and volume of the converter.

Fig.2: Waveforms and switching intervals for SISO converter.

III. OPERATION PRINCIPLES AND ANALYSIS OF THE PROPOSED CONVERTER

A. Steady State and Dynamic Analysis of Single-Input Single-Output Converter

For a better understanding of the steady state and dynamic analysis of the converter, only one of the input ports (the first one shown in Fig. 1) is studied. Therefore, the converter circuit is a combination of a HFIL transformer, a half-bridge boost converter and a cycloconverter, the input source (FC), and the output filter (L_f and C_f). The simulation results of key waveforms for a specific operating point are illustrated in Fig. 2, where the energy is transferred from the first input port to the output port. The switching period ($T_s = 1/f_s$) is equal to the interval from t_0 to t_8. This switching interval is divided to eight intervals, as listed in Table I.

In the proposed topology, the input source (V_1) is doubled across the dc capacitors C_1 and C_2 by the boost converter, which operates with the duty cycle equal to 50%. It is assumed that $C_1 = C_2 = C$. The voltages of dc capacitors ($V_{C1} + V_{C2}$)

TABLE I
SWITCHING INTERVALS

Interval	From-To	Description
1	t_0-t_1	D_{11}, S_{C2} : on
2	t_1-t_2	D_{11}, S_{C1}, S_{C2}: on
3	t_2-t_3	S_{11}, S_{C1} :on
4	t_3-t_4	C_{r11}, C_{r21}, transformer resonant, S_{C1} , S_{11} : on
5	t_4-t_5	D_{21}, S_{C1} : on
6	t_5-t_6	D_{21}, S_{C1}, S_{C2}: on
7	t_6-t_7	S_{21}, S_{C2} : on
8	t_7-t_8	C_{r11}, C_{r21}, transformer resonant, , S_{21}, S_{C2} : on

remain almost constant and approximately equal ($V_{C1} \simeq V_{C2}$), therefore, the dc link voltage V_{12} is determined by the following:

$$V_{12} = V_{C1} + V_{C2} = 2V_1 . \quad (1)$$

The dc link voltage in steady-state operation remains constant with small fluctuations. To avoid the short-circuit conditions, the switches S_{11} and S_{21} do not conduct simultaneously, therefore, each switch has a square-wave ac voltage with a dead time between them. The square-wave voltages, named V_{s11} and V_{s21}, are equal in amplitude, as shown in Fig. 2, and have a duty cycle of about 50%. Therefore, the voltage of primary winding V_p is a high-frequency bipolar square-wave ac voltage with duty cycle equal to 50%. Through HFIL transformer, the voltage is boosted again as follows:

$$V_{s1} = V_{s2} = V_p \times n \quad (2)$$

where n is equal to N_{s1}/N_p, and $N_{s1} = N_{s2}$. The average voltage of the output is regulated by the phase shift (ϕ) of cycloconverter switches (S_{C1} and S_{C2}) with respect to the half-bridge switches (S_{11} and S_{21}). According to Fig. 2, the amplitude of the output voltage is regulated by phase shift ϕ. The voltage of cycloconverter is a square waveform, such that its average determines the instantaneous voltage value of the output. These instantaneous average voltage levels of the output change according to the reference voltage (i.e., ac sinusoidal voltage with a frequency of 50/60 Hz) by controlling the phase shift ϕ. The current waveforms of primary side of transformer (I_p) is depicted in Fig. 2, to indicate the conduction of half-bridge switches and their body diodes.

The intervals 2, 4, 6, and 8 can be eliminated to simplify the modelling of the circuit. Then, the simplified circuit has four intervals, i.e., 1, 3, 5, and 7. Four equivalent circuits of these intervals from secondary side viewpoint are shown in Fig. 3. In this figure, the total inductor value is determined by the following:

$$L_t = L_M + L_f + L_s \quad (3)$$

where $L_s = L_{s1} = L_{s2}$ is the value of snubber inductors, L_f is the value of the output filtering inductor, and L_M is the value of transformer leakage inductor. r_1 and r_t model the switching losses in input and output ports, respectively.

In this paper, an FC with $m = 40$ cells in series, is used, whose voltage can be defined as follows [20]:

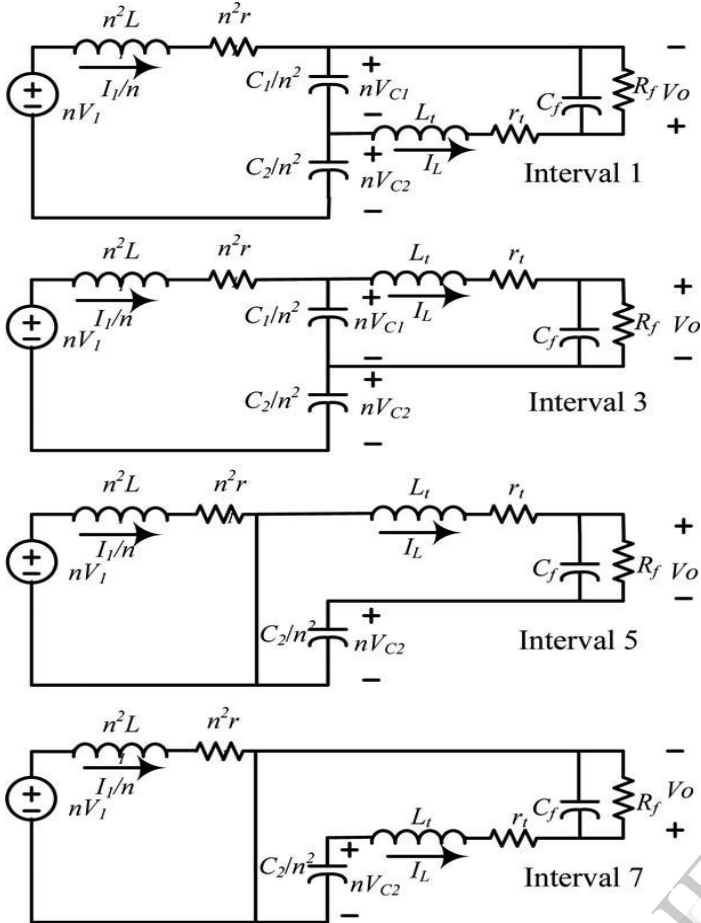$$V_1 = V_{FC} = m(E_o - b(T)\ln(I_1) - R(T)I_1 - k(T)e_{zI_1}) \quad (4)$$

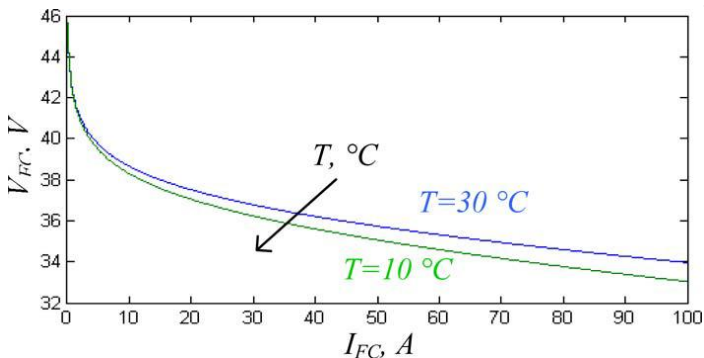Fig. 3. Equivalent circuits of operating intervals.

Fig. 4. Relationship between voltage and current of FC at different temperatures.

where

$E_o = 1.05$ is open circuit voltage;

$z = 8 \times 10^{-3}$ is a constant;

I_1 is the current of FC;

T is the temperature in $^\circ$C; and

$b = 4.01 \times 10^{-2} - 1.4 \times 10^{-4} T$, $R = 4.77 \times 10^{-4} - 3.32 \times 10^{-6} T$,

and $k = 3.3 \times 10^{-3} - 8.2 \times 10^{-5} T$ represents the coefficients that depend on the temperature. Then, the relationship between

$V_1 = V_{FC}$ and $I_{FC} = I_1$ at different temperatures can be represented in Fig. 4, which shows, decreasing at temperature results decreasing voltage.

With linearization of (4), we have

$$V_1 = V_{FC} = m(E_o - (4.01 \times 10^{-2} - 1.4 \times 10^{-4}T)$$
$$\times \left(2.4 + \frac{I_1}{30}\right) - (4.77 \times 10^{-4} - 3.32 \times 10^{-6}T)I_1$$
$$- (3.3 \times 10^{-3} - 8.2 \times 10^{-5}T)(1 + 0.008I_1)$$

$$= m\ (-0.09954 + E_o + i(-0.00184 + 8.64 \times 10^{-6}T) + 0.000418T). \quad (5)$$

In this paper, the state-space-averaging method is used, and general equations for both steady state (i.e., dc) and dynamic performance (i.e., ac) are obtained. Each interval can be represented by a linear circuit, as shown in Fig. 3. The corresponding sets of state-space equations for the four switched intervals are given as follows, (6), as shown at the bottom of the page, where X is the state-space vector, Y is the output vector, and U is the input vector. The total number of energy-storage elements determines the order of the system. Based on the state-space-averaging method, the state-space description of the four linear circuits can be replaced by a single state-space description, which represents the behaviour of the circuit for all periods. Summing the equations for four intervals results in the following linear continuous system:

$$X' = \frac{\varphi}{2\pi}(A_1X + B_1U) + \frac{\pi - \varphi}{2\pi}(A_2X + B_2U)$$
$$+ \frac{\varphi}{2\pi}(A_3X + B_3U) + \frac{\pi - \varphi}{2\pi}(A_4X + B_4U)$$
$$Y = \frac{\varphi}{2\pi}(C_1^T X) + \frac{\pi - \varphi}{2\pi}(C_2^T X) + \frac{\varphi}{2\pi}(C_3^T X)$$
$$+ \frac{\pi - \varphi}{2\pi}(C_4^T X). \quad (7)$$

This model is an averaged model over a single period. Based on the following assumptions:

$$A = \frac{\varphi}{2\pi}A_1 + \frac{\pi - \varphi}{2\pi}A_2 + \frac{\varphi}{2\pi}A_3 + \frac{\pi - \varphi}{2\pi}A_4$$
$$B = \frac{\varphi}{2\pi}B_1 + \frac{\pi - \varphi}{2\pi}B_2 + \frac{\varphi}{2\pi}B_3 + \frac{\pi - \varphi}{2\pi}B_4$$
$$C^T = \frac{\varphi}{2\pi}C_1^T + \frac{\pi - \varphi}{2\pi}C_2^T + \frac{\varphi}{2\pi}C_3^T + \frac{\pi - \varphi}{2\pi}C_4^T. \quad (8)$$

The equations of state-space-averaging model are obtained as follow:

$$X' = AX + BU$$
$$Y = C^T X \quad (9)$$

where the state-space variables and the input vector are defined as follows:

$$X = \begin{bmatrix} i_1 \\ v_{12} \\ i_L \\ v_o \end{bmatrix} \qquad U = [V_1] \qquad (10)$$

where $V_{12} = V_{c1} + V_{c2}$. By using *Kirchhoff 's* voltage and current laws and (5), the state-space-averaged equations of this
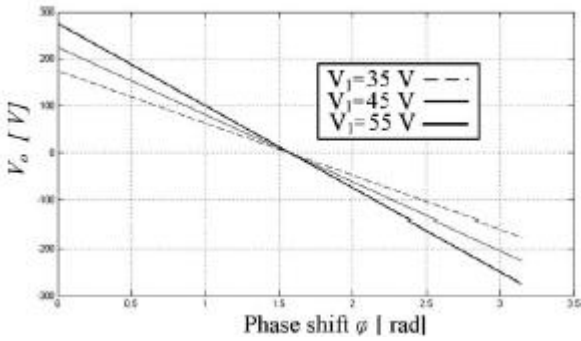

Fig. 5. Variations of V_o versus ϕ.

converter are presented by the following:

$$\begin{bmatrix} i_1' \\ v_{12}' \\ i_L' \\ v_o' \end{bmatrix} = A \cdot \begin{bmatrix} i_1 \\ v_{12} \\ i_L \\ v_o \end{bmatrix} + B$$
$$\cdot (-0.09954 + E_O + 0.000418T)m \qquad (11)$$

where, (12) and (13), as shown at the bottom of the page. Using the equation $X = -A^{-1}BU$ and $Y = -C_T A^{-1}BU$, the dc part of steady-state equation can be written as follows,(14), as shown at the bottom of the page.

It is assumed that $r_1 = r_t = 0$. The last row of (14) presents the relation between V_o and E_1 as a function of ϕ. Fig. 5 depicts the variation of the output voltage against phase shift ϕ for three different values of the input voltage and $T = 30 °C$. This figure shows how the output voltage (V_o) changes with ϕ from positive to negative, and increasing the phase shift decrease the output
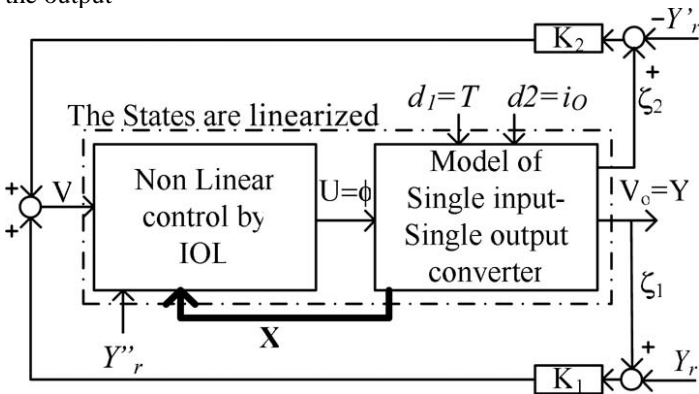

Fig. 6. Overall control block diagram of SISO converter.

magnitude. V_o crosses zero at $\phi = 1.6$ rad, and its minimum amount is at $\phi = 3.2$ rad. It is obvious that the slope of V_o variation can be changed by changing the input voltage.

Therefore, to have a proper controller, it is reasonable to set the desired dc link voltage to two times of the voltage of maximum power operating point. Therefore, maximum utilization of the input source is achieved, and the boost converter operates at duty cycle of 50%. For a two and higher number of input ports converter, the value of dc link voltage indicates the amount of the current that can be provided by the first input, and the other input ports inject the rest of the output current. Fig. 6 shows how the phase shift can be controlled in such a way to have a desired output voltage and dc link voltage.

1) Nonlinear Control of Single-Input Single-Output Converter Based on Input–Output Linearization: In this section, a single-input single-output (SISO) dynamic nonlinear model of the SISO converter is derived from (11)–(13), and then, it is used to design a nonlinear controller by using IOL [23]. The purpose of this section is regulating *Vo* to desired value with phase shift. Then, phase shift is the input of the system model. By reordering (11)–(13), the state equations are rewritten as follows:

$$\begin{bmatrix} x_1' \\ x_2' \\ x_3' \\ x_4' \end{bmatrix} = f(x) + g(x)u + p_1(x)d_1 + p_2(x)d_2, \quad Y = h(x)$$
$$(15)$$

where, (16), as shown at the bottom of the page, where $d \subset R_k$ is the $k = 2$ dimensional disturbance vector, and it will not be used in controller. $x \subset R_n$ is the $n = 4$ dimensional statespace vector ($n = 4$ is total number of energy-storage elements in SISO converter), $u \subset R_m$ is the $m = 1$ dimensional input vector, $y \subset R_n$ is the $m = 1$ dimensional output vector, $h(x)$ is m dimensional smooth vector field, $f(x)$ is n dimensional smooth vector field, $g(x)$ is n dimensional smooth vector field for input i, and $p_1(x)$ and $p_2(x)$ are n dimensional smooth vector fields related to the first and second disturbances (d_1 and d_2). With changing equilibrium point to $X = 0$, the SISO nonlinear system is defined as follows, (17), as shown at the bottom of the page.

IOL for SISO systems is obtained as follows. Firstly, the output (y) is differentiated until the input appears. The number of derivatives required for that r is called the relative degree of output .In this system, r is chosen to be 2. These derivatives may be expressed as follow:

$$Y^{(r)} = L_f^r h(x) + L_g \left(L_f^{r-1} h(x) \right) u \qquad (18)$$

where $L_f h = \nabla h \cdot f$ is a Lie derivative. In this system, (18) is as follow:

$$\begin{bmatrix} h(x) \\ L_f h(x) \end{bmatrix} = \begin{bmatrix} x_4 \\ \dfrac{1}{C_f} x_3 \end{bmatrix} . \qquad (19)$$

Then, we define a new coordinate as follows:

$$Z = T(x) = \begin{bmatrix} h(x) \\ L_f h(x) \\ x_1 \\ x_2 \end{bmatrix} = \begin{bmatrix} \xi_1 \\ \xi_2 \\ \eta_1 \\ \eta_2 \end{bmatrix} = \begin{bmatrix} x_4 \\ \dfrac{1}{C_f} x_3 \\ x_1 \\ x_2 \end{bmatrix} . \qquad (20)$$

Then, the state space of new coordinate, at the systems equilibrium point can be defined as follows, (21-1) and (21-2), as shown at the bottom of the page. In (21-1), ξ_2 will be used to define the control law, and (21-2) is called zero dynamics. If $\eta\_$ is asymptotically stable at point that is indicated by the following:

$$Z^* = \{ x \in R^4 | \xi_1 = \xi_2 = 0 \} \text{ and}$$

$$u(x) = u^*(x) = -\left. \frac{\xi_2' f(x)}{\xi_2' g(x)} \right|_{x=z^*} \qquad (21\text{-}3)$$

then, the system is called minimum phase, and it is necessary in IOL. In this system, (21-2) at point Z and $u*(x)$ is as follow, which is stable and called minimum phase, as shown (22) at the bottom of the page.

To ensure that ξ_1 is adjusted to the desired value of Y_r, the stabilizing controller is designed by linear-control theory using the pole-placement strategy. The new control inputs are given by

$$\begin{bmatrix} e_1 \\ e_2 \end{bmatrix} = \begin{bmatrix} \xi_1 - y_r \\ \xi_2 - y_r' \end{bmatrix} \Rightarrow \begin{bmatrix} e_1' \\ e_2' \end{bmatrix} = \begin{bmatrix} \xi_2 - y_r' \\ \xi_2' - y_r'' \end{bmatrix} . \qquad (23)$$

Then, (21-1) with these new control inputs can be written as follow:

$$\begin{bmatrix} e_1' \\ e_2' \end{bmatrix} = \begin{bmatrix} e_2 \\ \dfrac{1}{C_f} \left(\dfrac{n}{2L_t} x_2 - \dfrac{r_t}{L_t} x_3 - \dfrac{1}{L_t} x_4 \right) - \left(\dfrac{n}{\pi L_t C_f} x_2 \right) u - y_r'' \end{bmatrix}$$

$$= \begin{bmatrix} e_2 \\ v \end{bmatrix} = \begin{bmatrix} e_2 \\ k_1 e_1 + k_2 e_2 \end{bmatrix} \qquad (24)$$

where v is control law. To have a stable controller and have left side poles, the coefficients of K_1 and K_2 should have negative value. Fig. 6 shows how the phase shift can be controlled in such a way to have a desired output voltage with nonlinear control by IOL.

B. Double-Input Single-Output Converter

In this section, it is assumed that the converter has two input ports and one output port. The first input is an FC that should always be in the system, and the second input is a lead acid battery. It is a suitable choice for storage because, not only it shows fast response time to load changes, but also it is cheap and widely available. Fig. 7(a) and (b) illustrate the waveforms of the discharging and charging modes, respectively. It must be mentioned that, if the energy is transferred from battery to dc link, then, it is in discharging mode and vice versa. The current waveform of the primary side transformer (I_p), the current of first input port (I_1), the current of second input port (I_2), duty cycle of first input port (D_1), and duty cycle of second input port (D_2) are plotted in both Fig. 7(a) and (b). The switching frequency of both ports is almost equal to f_s.
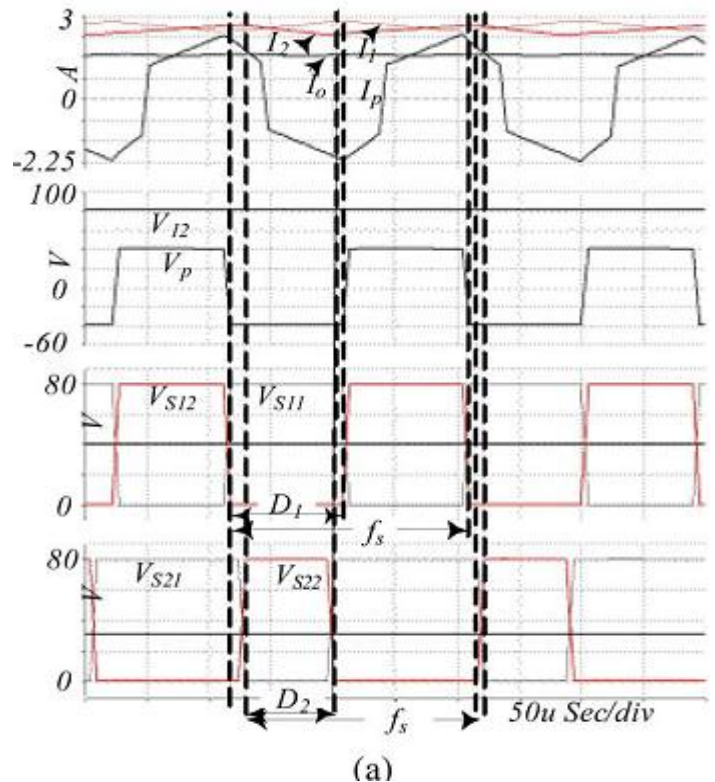
The ith input port can be modeled by using the assumption that the voltage source for dc link is constant. In Fig. 1, port 2 is like a boost converter connected to a dc voltage. Then, then simplified circuits of two intervals can be modeled, as shown in Fig. 8, where r_2 represents the switching losses and E_m, R_{ob}, C_b, and R_b are the parameters of battery model. This modelling method can be applied to other input ports, because the voltage of the dc link is kept constant by the first input port. Therefore, the other input ports can be adjusted considering the constant dc link voltage.

The parameters of battery model, as a function of state of charge (SOC) and θ can be computed as follows in [21] and [22]:

$$E_m = E_{mo} - k_c \theta (1 - \text{SOC}) \qquad (25)$$

$$R_{0b} = R_{oo} [1 + A_0 (1 - \text{SOC})] \qquad (26)$$

$$R_b = -R_{10} \ln(\text{SOC}) \qquad (27)$$
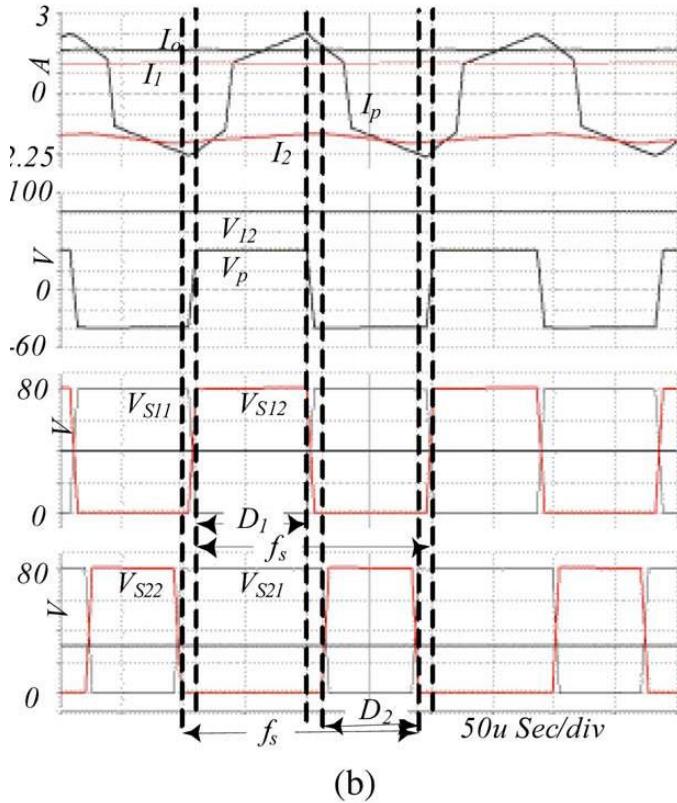

(a)

(b)

Fig. 7. Waveforms of double-input single-output converter (a) discharging (b) charging modes.

$$C_b = \frac{\tau_1}{R_b} \quad (28)$$

where

E_m is the open-circuit voltage in volts;

$E_{m0} = 31.5$ is the open-circuit voltage at full charge in volts;

$K_c = 0.009$ is a constant in volts/K;

θ is electrolyte temperature in K;

SOC is the battery state of charge;

R_{Ob} and R_b are resistances in ohm;

$R_{OO} = 0.12$ is the value of R_O at SOC $= 1$ in ohms;

$A_O = -0.0948$ and $R_{10} = 0.031$ are constants;

C_1 is a capacitance in farads; and

τ_1 is a time constant in seconds.

As shown in Fig. 8, this circuit has two intervals. The state space- averaged equations, using (25)–(28), are as follows:

$$\begin{bmatrix} i_2' \\ V_{C_b}' \end{bmatrix} = \begin{bmatrix} -\dfrac{R_{Ob} + r_2}{L_2} & \dfrac{-1}{L_2} \\ \dfrac{1}{C_b} & \dfrac{-1}{C_b R_b} \end{bmatrix} \begin{bmatrix} i_2 \\ V_{C_b} \end{bmatrix}$$
$$+ \begin{bmatrix} \dfrac{1}{L_2} & \dfrac{-D_2}{L_2} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} E_m \\ V_{12} \end{bmatrix}. \quad (29)$$
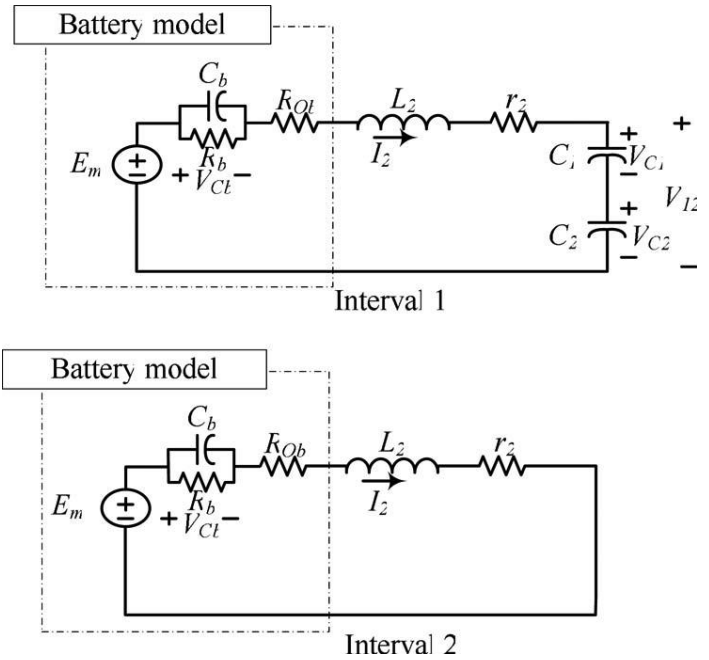

Fig. 8. Equivalent circuits of operating intervals: interval 1, S_{12} in on; interval 2, S_{22} in on.

In (29), r_2 and L_2 are switching loss resistance and the inductor of the second input port, respectively.

The dc term of steady-state equation is as follows:

$$\begin{bmatrix} i_2 \\ V_{C_b} \end{bmatrix} = \begin{bmatrix} \dfrac{E_m - D_2 V_{12}}{r_2 + R_b + R_{Ob}} \\ \dfrac{R_b(E_m - D_2 V_{12})}{r_2 + R_b + R_{Ob}} \end{bmatrix}. \quad (30)$$

As shown in Fig. 7, a phase shift of $180°$ results in the reduction of the current stress across the dc link capacitor and continuous dc link current. As a result, the size of capacitors is reduced too. For the second and other input ports, the dc link has the role of voltage source for transferring power between ith ($i = 2, 3, . . .,)$ port and dc link. Therefore, when the load increases, the voltage of dc link begins to reduce. At this time, the second and third input ports try to increase the voltage by injecting current. In the case of reduction of the voltage of dc link, the other ports try to absorb current to regulate the dc link voltage. The injection and absorption of current can be adjusted by changing the duty cycle. For example in Fig. 7, the duty cycle D_2 has been changed, but the duty cycle of first input port is kept constant (e.g., 50%). The variation of the duty cycle (D_2) in the second boost converter allows the second input port to be used as a source with variable voltage magnitude. In Fig. 7(a), $r_2 > -(R_b + R_{Ob})$ and the duty cycle D_2 is smaller than E_m/V_{12}, therefore, the second port injects current and starts discharging.

In Fig. 7(b), $r_2 > -(R_b + R_{Ob})$ and the duty cycles D_2 is bigger than E_m/V_{12}, therefore, the second port absorbs current and starts charging. Therefore, the second boost converter has a

bidirectional characteristic suitable for batteries. If D_2 is equal to E_m/V_{12}, then i_2 will be equal to zero.

1) Nonlinear Control of Double-Input Single-Output Converter Based on Input-Output Linearization: Like Section III-A-1, in this section, an SISO dynamic nonlinear model of the double-input single-output converter is derived from (29), and then, it is used to design a nonlinear controller by using IOL [23]. The purpose of this section is regulating I_2 to desired value with D_2. Then, D_2 will be the input of nonlinear dynamic
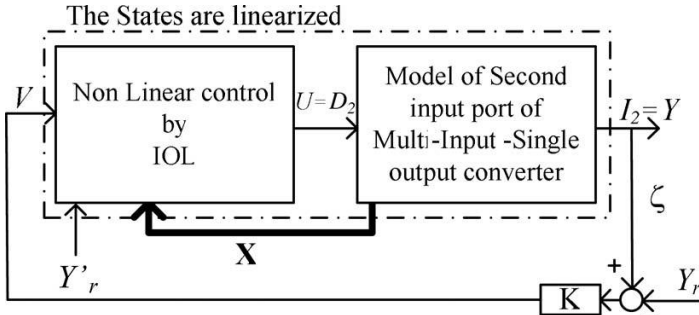

Fig. 9. Current control block diagram of double-input single-output converter.

equation. By reordering (29), the state-space equations will be as follows:

$$\begin{bmatrix} x_1' \\ x_2' \end{bmatrix} = f(x) + g(x)u, \quad Y = h(x) \tag{31}$$

Where,

$$\begin{bmatrix} x_1 \\ x_2 \end{bmatrix} = \begin{bmatrix} i_2 \\ v_{12} \end{bmatrix} \quad u = D_2$$

$$f(x) = \begin{bmatrix} -\dfrac{R_{ob}+r_2}{L_2}x_1 - \dfrac{1}{L_2}x_2 + \dfrac{E_m}{L_2} \\ \dfrac{1}{C_b}x_1 - \dfrac{1}{C_bR_b}x_2 \end{bmatrix}$$

$$g(x) = \begin{bmatrix} \dfrac{-V_{12}}{L_2} \\ 0 \end{bmatrix} \quad h(x) = i_2 \tag{32}$$

where $x \subset R_2$ is the $n = 2$ dimensional state-space vector ($n = 2$ is total number of energy storage elements in double input single-output converter), $u \subset R_m$ is the $m = 1$ dimensional input vector, $y \subset R_m$ is the $m = 1$ dimensional output vector, $h(x)$ is m dimensional smooth vector field, $f(x)$ is n dimensional smooth vector field, and $g(x)$ is n dimensional smooth vector field. With changing equilibrium point to $X = 0$, the SISO nonlinear system is defined as follows:

$$\begin{bmatrix} x_1' \\ x_2' \end{bmatrix} = \begin{bmatrix} \dfrac{-R_{ob}-r_2}{L_2}x_1 - \dfrac{1}{L_2}x_2 \\ \dfrac{1}{C_b}x_1 - \dfrac{1}{C_bR_b}x_2 \end{bmatrix} + \begin{bmatrix} \dfrac{-V_{12}}{L_2} \\ 0 \end{bmatrix}u, \quad y = x_1. \tag{33}$$

The relative degree of output, which is $r = 1$ in this system. Then, we define a new coordinate as follow:

$$Z = T(x) = \begin{bmatrix} h(x) \\ x_2 \end{bmatrix} = \begin{bmatrix} \xi \\ \eta \end{bmatrix}. \tag{34}$$

The state space of new coordinate at the systems equilibrium point can be defined as follows:

$$\xi' = \left(\dfrac{-R_{ob}-r_2}{L_2}\xi - \dfrac{1}{L_2}x_2 + \dfrac{E_m}{L_2} \right) + \dfrac{-V_{12}}{L_2}u. \tag{35-1}$$

$$\eta' = x_2' = \dfrac{1}{C_b}x_1 - \dfrac{1}{C_bR_b}x_2. \tag{35-2}$$

In (35-1), ξ_- will be used to define the control law and (35-2) is called zero dynamics. Again like previous, if η_- is symptotically stable at point indicated by the following:

$$Z^* = \{x \in R^4 | \xi = 0\} \quad \text{and} \quad u(x) = u^*(x)$$

$$= -\dfrac{\xi' f(x)}{\xi' g(x)}\bigg|_{x=z^*} \tag{35-3}$$

then the system is called minimum phase. In this system, (35-2) at point Z_* and $u_*(u)$ is as follow, which is stable and called minimum phase:

$$x_2' = -\dfrac{1}{R_bC_b}x_2. \tag{36}$$

To ensure that ξ is adjusted to the desired value of Y_r, the stabilizing controller is designed by linear-control theory using the pole-placement strategy. The new control input is given by

$$e = \xi - y_r \Rightarrow e' = \xi' - y_r'. \tag{37}$$

Then, (35-1) with this new control input can be written as follow:

$$e' = \left(\dfrac{-R_{ob}-r_2}{L_2}\xi - \dfrac{1}{L_2}x_2 + \dfrac{E_m}{L_2} \right) + \dfrac{-V_{12}}{L_2}u - y_r'$$

$$= v = ke \tag{38}$$

where v is control law. To have a stable controller and have left side poles, the coefficient of K should have a negative value. Fig. 9 shows how the duty cycle can be controlled in such a way to have a desired output current with nonlinear control by IOL.

The ESS is a battery with its voltage-time and energy-time curves. The rated power of ESS is P_2, and the full power
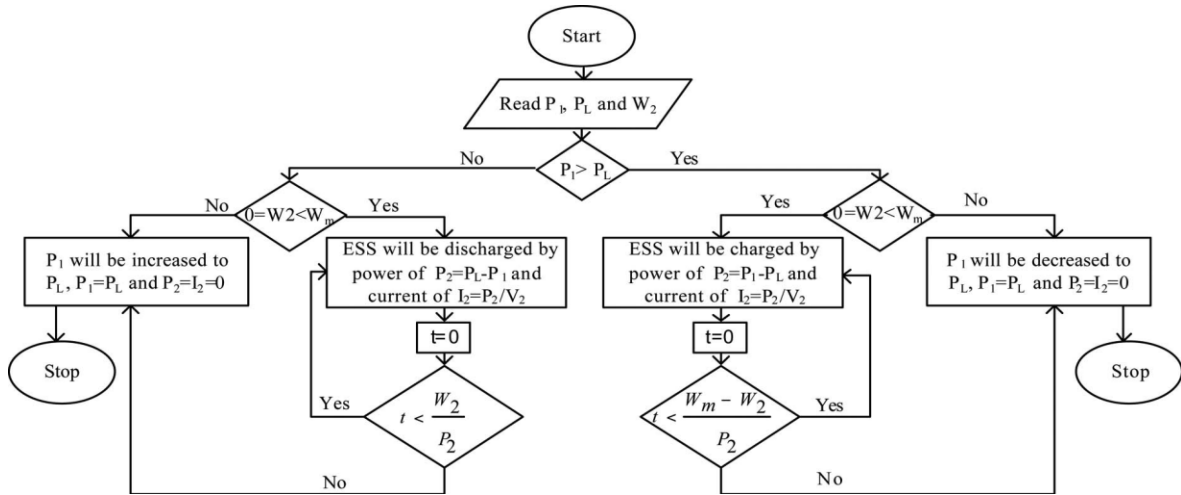
Fig. 10. Algorithm of I_2 determination.

operation duration time is t seconds, then, the energy capacity is $W_m = P_2 t$. The reference current of the second input port for a ESS can be determined by the algorithm shown in Fig. 10, where P_1 is the rated power of first input port, P_L is the power of load, and W_2, I_2, and V_2 are the energy, current, and voltage of ESS, respectively.

For $N + 1$ port converter, which has N input ports and one output port, the controller block diagram for ith input, can be developed like Fig. 9. The value of output voltage (V_o) determines the value of the current generated by the first input, and V_o is used to control ϕ. The current of other ports can be controlled by their duty cycles. It should be noted that in this topology, the first input source has to be always connected and operate as a voltage source. The other ports operate as current sources to provide the required dc link voltage.

IV. MEASUREMENT AND SIMULATION RESULTS
Energy management of proposed converter under different operating conditions will be studied in this section. The rating and parameters of three port (double-input single-output) converter, given in Table II, have been used in the simulations and building the prototype. The first port uses a dc source with magnitude of 42 V, to model an FC. The second port uses 40-mF, 30-V capacitor as a storage element. The output voltage is regulated to 110 V and 60 Hz. As shown in Fig. 11, a
.
The proposed double-input single-output system has been simulated to evaluate its response to changes, such as variations of load resistance, as well as charging and discharging operating conditions. The simulation of operating conditions has been carried out for 6 s to study the energy management of the proposed converter. As shown in Fig. 12, the operating conditions have been divided into four stages as follows:

TABLE II
THREE-PORT CONVERTER PARAMETERS

Converter parameters	Value
Switching frequency, f_S	15800 Hz
L_1, L_2	5 mH
L_f	5 mH
L_{S1}, L_{S2}	10 μH
L_M	60 μH
C_1, C_2	100 μF
C_f	4 μF
First input voltage, V_1	40 V FC
Second input voltage, V_2	30 V Battery
Output ac voltage, V_O	110 V, AC, 60Hz
winding ratio, N	$N_{S1}/N_P = N_{S2}/N_P = 5$

Stage one (0 < t < 1.5 s): In this stage, the power of the load is about 140 W, and the load (P_o) is supplied only by first input port (P_1), and the second input port power (P_2) remains almost zero. As a result, the current of first port (I_1) is about 3.5 A, and current of second port (I_2) is almost zero during this operating condition.

Stage two (1.5 < t < 3 s): The second stage is a discharging operating condition. The second port supplies a part of load power, which is about 40 W, and the rest of the load power is provided by the first port (i.e., $P_1 = 100$ W). Therefore, the current of first port (I_1) is reduced to 2.3 A, and the current of second port (I_2) is increased to about 1.2 A.

Fig. 12. Simulation results of four operating conditions.

Stage three (3 < t < 4.5 s): In the third stage, the effect of load power variations has been studied by increasing the load resistance (decreasing the load power to 30 W). It is obvious that

P_1 decreases, to satisfy the load power, and then, it forces the second port to decrease its power to almost zero.

Fig. 13. Experimental results (X-axis: 500 ms/div) (a) V_1 (Y -axis: 50 v/div) and V_2 , (b) V_{12} (Y -axis: 50 v/div), and (c) I_1 and I_2 (Y -axis: 1A/div).

In this situation, the current of first port (I_1) is reduced to 0.9 A, and the current of second port (I_2) is equal to zero.
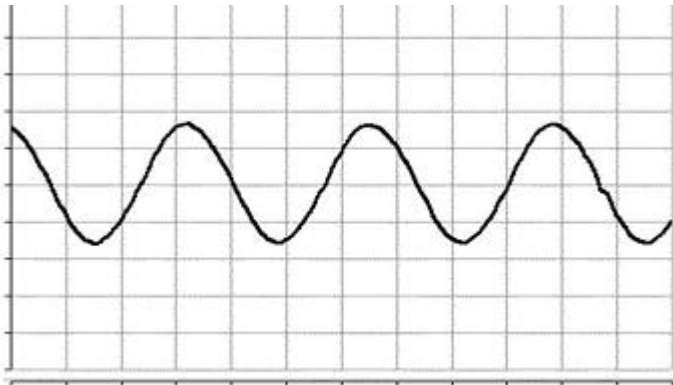

Fig. 14. Output voltage (a) simulated (Y -axis: 100 v/div) and

Stage four (4.5 < t < 6 s): The capability of the converter to supply the load and inject the active power to the storage element (second input port) has been studied in this stage. This stage is called the charging operating mode. In this stage, P_1 increases to 55 W, therefore, it can supply the load power of about 30 W, and inject the extra power to the storage capacitor by using the second-port boost converter.

It should be mentioned that with variation of load current (I_o) and input currents (I_1 and I_2), the voltage of dc link voltage (V_{12}) and output voltage (V_o) remain constant in four stages. The output voltage is set to 110 V, 60 Hz, and the V_{12} is about 80 V.

Fig. 13 shows the experimental results of the input ports voltages (V_1 and V_2), dc link voltage (V_{12}) and input ports currents (I_1 and I_2) for the same operating conditions, as presented in Fig. 12. The waveforms have a good agreement with simulation results.

As it can be seen in the Fig. 13, the voltage across the dc link is almost constant during all operating conditions, and it is two times greater than the first input port voltage [see Fig. 13(a)]. Fig. 14 shows the simulated and measured output voltage V_o , which have a good agreement with each other.

Fig. 15. Measured waveforms (X-axis: 20 μs/div) (a) Voltage across the switches (S_{11} , S_{21}) (Y -axis: 50 v/div), (b) voltage across the switches (S_{12} , S_{22}) (Y -axis: 50 v/div), (c) transformer primary voltage (Y -axis: 20 v/div) (V_p), and (d) transformer secondary winding voltages (V_{S1} , V_{S2}) (Y -axis: 100 v/div).

The measurement results for switching operating condition are given in Fig. 15. The voltage across the switches S_{11} and S_{21}, voltage across the switches S_{12} and S_{22}, transformer primary voltage V_p , and transformer secondary winding voltages V_{S1} and V_{S2} have been shown in the Fig. 15(a)–(d), respectively.

As shown in Fig. 15(a), the duty cycle of the first input port is 50% but the duty cycle of the other port, as shown in Fig. 15(b), depends on its current. Transformer primary voltage (V_p) has square waveforms with duty cycle of 50% [shown in Fig. 15(c)] and has the amplitude of the half of dc link voltage (V_{12}). As shown in Fig. 15(d), it is obvious that the secondary windings voltages (V_{S1} and V_{S2}) are five times bigger than the primary voltage.

V. CONCLUSION

In this paper, a new low cost and small-size topology for direct dc–ac conversion has been proposed and studied. To improve the dynamic performance, a control strategy has been suggested. This control strategy is simple and based on phase shift (PS) control technique. The proposed converter presents bi-directional power- flow capability and it is very suitable for DG applications. The input-boost inverters satisfy the requirements of DGs, such as PV and FC systems, and increase the voltage level at the input of HFIT, as well as decrease the input current ripple. Also, a reduction in the count of devices and circuits is obtained. As a result, the cost, size, and volume of the converter are reduced. The reduced number of the conversion steps results in higher power efficiency for the proposed converter

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