Multi-Level Inverter for Power Quality Improvement in Renewable Power Generation System

S. Naresh Kumar*, S. Naresh Sivakanth **, K. Siva Kumar ***
* (M.Tech, Department of Electrical Engg, GLBC College, Kadapa)
** (Assistant Professor, Department of Electrical Engg, GLBC college Kadapa)
*** (Associate Professor, Department of Electrical Engg, GLBC college, Kadapa)

***ABSTRACT*— Multilevel inverter can effectively reduce the voltage distortions of each switching operation to reduce the switching loss and increase power efficiency. The multilevel inverter has been aroused due to its advantages of better power efficiency, lower switching harmonics, and a smaller filter inductor compared with the conventional half-bridge and full-bridge inverters. A five-level inverter is developed and applied for introducing the real power of the renewable power into the grid. This five-level inverter consists of two dc capacitors, a dual-buck converter, a full-bridge inverter, and an inductor filter.**

The five-level inverter generates an output voltage with five levels and applies in the output stage of the renewable power generation system to produce a sinusoidal current in phase with the utility vol tage to inject into the grid. The power electronic switches of the dual-buck converter are switched in high frequency to generate a three-level voltage and balance the two input dc voltages. The electronic switches of the full-bridge inverter are switched in low frequency synchronous to the utility to convert the output voltage of the dual-buck converter to a five-level ac voltage. It shows that this developed renewable power generation system reaches the expected results in performance. The performance of the Five Level Inverter for the renewable power generation system is studied through extensive simulations using MATLAB.

***Index Terms*—** Harmonic distortion, inverters, power electronics.

I. INTRODUCTION

THE conventional single-phase inverter topologies for grid connection include half-bridge and full bridge. The Half-bridge inverter is configured by one capacitor arm and one power electronic arm. The dc bus voltage of the half-bridge inverter must be higher than double of the peak voltage of the output ac voltage. The output ac voltage of the half-bridge inverter is two levels. The voltage jump of each switching is the dc bus voltage of the inverter. The full-bridge inverter is configured by two power electronic arms. The popular modulation strategies for the full-bridge inverter are bipolar modulation and unipolar modulation.

The dc bus voltage of the full-bridge inverter must be higher than the peak voltage of the output ac voltage. The output ac voltage of the full-bridge inverter is two levels if the bipolar modulation is used and three levels if the unipolar modulation is used. The voltage jump of each switching is double the dc bus voltage of the inverter if the bipolar modulation is used, and it is the dc bus voltage of the inverter if the unipolar modulation is used. All power electronic switches operate in high switching frequency in both half-bridge and full bridge inverters. The switching operation will result in switching loss. The loss of power electronic switch includes the switching loss and the conduction loss. The conduction loss depends on the handling power of power electronic switch. The switching loss is proportional to the switching frequency, voltage jump of each switching, and the current of the power electronic switches. The power efficiency can be advanced if the switching loss of the dc–ac inverter is reduced. Multilevel inverter can effectively reduce the voltage jump of each switching operation to reduce the switching loss and increase power efficiency. The number of power electronic switches used in the multilevel inverter is larger than that used in the conventional half-bridge and full-bridge inverters. Moreover, its control circuit is more complicated. Thus, both the performance and complexity should be considered in designing the multilevel inverter. However, interest in the multilevel inverter has been aroused due to its advantages of better power efficiency, lower switching harmonics, and a smaller filter inductor compared with the conventional half-bridge and full-bridge inverters. The conventional single-phase multilevel inverter topologies include the diode-clamped, the flying capacitor, and the cascade H-bridge types, as shown in Fig. 1. Fig. 1(a) shows the basic configuration of a diode-clamped multilevel inverter. As can be seen, it is configured by two dc capacitors, two diodes, and four power electronic switches. Two diodes are used to conduct the current loop, and four power electronic switches are used to control the voltage levels. The output voltage of the basic diode-clamped multilevel inverter has three levels.

The voltage difference of each level is Vdc/2 (the voltage on a capacitor). Since the voltages of two dc capacitors are used to form the voltage level of the multilevel inverter, the voltages of these two dc capacitors must be controlled to be equal.

The controller for balancing these two dc capaacitors is very important in operating the diode-clamped multilevel inverter, and it is very hard under the light load. If the five-level output voltage is expected, extra two diodes and four power electronic switches are required. Fig. 1(b) shows the circuit configuration of a basic flying capacitor multilevel inverter. As can be seen, it is configured by three dc capacitors and four power electronic switches. The voltage on each dc capacitor is controlled to be $V_{dc}/2$, and the output voltage of the basic flying capacitor multilevel inverter has three levels. The voltage difference of each level is also $V_{dc}/2$ (the voltage on a dc capacitor). These three dc capacitors must be controlled for maintaining their voltages to be $V_{dc}/2$ in the charge and discharge processes. Therefore, its control circuit is more complicated. If five-level output voltage is required, an extra dc capacitor and four power electronic switches are required. Fig. 1(c) shows the circuit configuration of the basic cascade H-bridge multilevel inverter. As can be seen, it is configured by two full-bridge inverters connected in cascade. The dc bus voltage of each full-bridge inverter is $V_{dc}/2$, and the output voltage of each full-bridge inverter can be controlled to be $V_{dc}/2$, 0, and $-V_{dc}/2$. Thus, the voltage levels of the output voltage of the cascade full-bridge multilevel inverter are V_{dc}, $V_{dc}/2$, 0, $-V_{dc}/2$, and $-V_{dc}$.

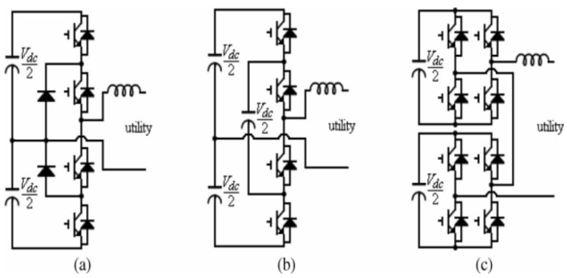


Fig. 1. Circuit configuration of conventional single-phase multilevel inverter.
(a) Diode clamped. (b) Flying capacitor. (c) Cascade H-bridge.

This topology has advantages of fewer components being required compared with other multilevel inverters under the output voltage with the same levels, and its hardware circuit can be modularized because the configuration of each full bridge is the same. However, this topology has the disadvantages that two independent dc voltage sources are required.

II. CIRCUIT CONFIGURATION

Fig. 2 shows the circuit configuration of the five-level inverter applied to a photovoltaic power generation system. As can be seen, it is consists of a solar cell array, a dc–dc converter, a five-level inverter, two switches, and a digital signal processor (DSP)-based controller. Switches SW1 and SW2 are placed between the five-level inverter and the utility, and they are used to disconnect the photovoltaic power generation system from the utility when islanding operation occurs. The load is placed between switches $SW1$ and $SW2$. The output of the solar cell array is connected to the input port of the dc–dc converter.

The output port of the dc–dc converter is connected to the five-level inverter. The dc–dc converter is a boost converter, and it performs the functions of maximum power point tracking (MPPT) and boosting up the o/p voltage of the arrays of solar cells. This inverter of five levels is configured by the two dc capacitors, a dual buck converter, a full-bridge inverter and an inductor filter. This dual-buck converter is configured by two buck converters. These two dc capacitors perform the function as energy buffers between the dc–dc converter and the five-level inverter. The dual-buck converter output is connected to the full-bridge type inverter to convert the voltage of dc into ac voltage. An inductor is placed in series at the output of the full bridge inverter to form as a filter inductor for filtering out of the high-frequency switching harmonic generated from the dual-buck converter.

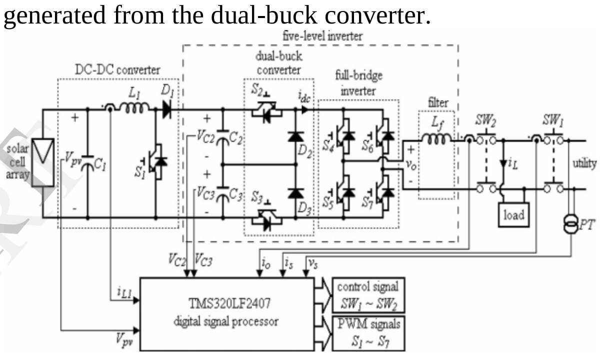


Fig. 2. Circuit configuration of the developed photovoltaic power generation system.

III. OPERATION PRINCIPLE OF FIVE-LEVEL INVERTER

The operation of the five-level inverter can be classified into eight modes. Modes 1–4 describe the operation of the positive half-cycle, and modes 5–8 are for the negative half-cycle. Considering operation modes 1–8, the full-bridge converter converts the dc o/p voltage of the dual-buck converter of three levels to an ac output voltage with five levels which are Vdc, Vdc/2, 0, $-V$dc/2, and $-V$dc. The operation of the power electronic switches S2 and S3 should guarantee that the output voltage of the dual-buck converter to be higher than the absolute of the uti lity voltage. The obtained waveforms of output voltage of five-level inverter and utility voltage are shown in Fig. 3.

Due to the operation of this full-bridge inverter, the obtained voltage and current in the dc side of full-bridge inverter are their absolute values of the utility voltage and the output current of the five level inverter. When the absolute of this utility voltage is lower than Vdc/2, the output voltage of the dual-buck converter should be changed between the values Vdc/2 and 0. Accordingly, the power electronics of five-level inverter is operated between the modes of 1 or 2 and mode 3 during the positive half-cycle.

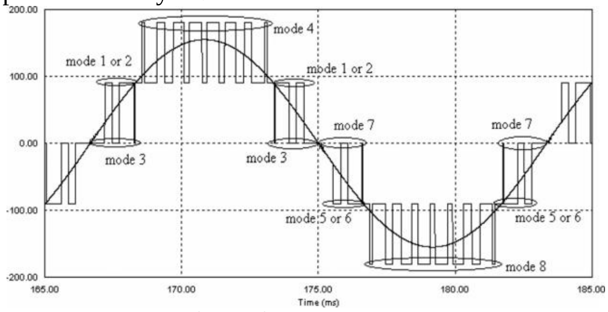


Fig. 3. Waveforms of output voltage and utility voltage.

On opposite to this, the power electronic switches of the Five-level inverter are switched between modes of 5 or 6 and mode 7 during the operation of negative half-cycle. One of the power electronic switches S2 and S3 is in the OPEN state and the other is switched in high frequency during one PWM period.

IV. VOLTAGE BALANCE OF FIVE-LEVEL INVERTER

Balancing or controlling the voltages of dc capacitors is very important to control the multilevel inverter. The voltage balancing of dc capacitor volt ages *VC*2 and *VC*3 can be controlled by the power electronic switches *S*2 and *S*3 easily. When the absolute of the utility voltage is lower than *V*dc/2, one power electronic switch which is either *S*2 or *S*3 is switched in high frequency and the other is still in the OFF state. Which power electronic switch is switched in high frequency depends on the dc capacitor voltages *VC*2 and *VC*3. If the dc capacitor voltage *VC*2 is more than dc capacitor voltage *VC*3, power electronic switch *S*2 is switched in high frequency. In this situation, the voltage source *VCx* in Fig. 4(a) is *VC*2, and *C*2 will be discharged. Thus, the dc capacitor voltages *VC*2 decreases and *VC*3 does not change. On the contrary, power electro nic switch *S*3 is switched in high frequency when voltage *VC*3 is more than voltage *VC*2. In this situation, the voltage source *VCx* in Fig. 4(a) is *VC*3. Thus, the dc capacitor voltages *VC*3 decreases and *VC*2 does not change. In this way, the voltage balancing of *C*2 and *C*3 can be achieved. When the absolute of the utility voltage is more than the *V*dc/2, one power electronic switch either *S*2 or *S*3 is switched in high frequency and the other is still in the ON state. Which power electronic switch is switched in high frequency depends upon the dc capacitor voltages *VC*2 and *VC*3. If dc capacitor voltage *VC*2 is more than dc capacitor voltage *VC*3, the power electronic switch *S*3 is switched in high frequency. The voltage source *VCx* in Fig. 4(b) is dc capacitor voltage *VC*2.

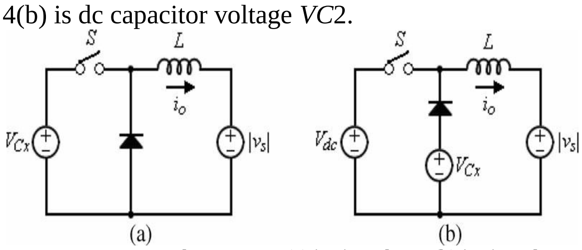


Fig.4. Equivalent circuit: (a) |vs |< Vdc /2. (b) |vs |> Vdc /2.

When the power electronic switch *S*3 is in ON state, both the capacitors *C*2 and *C*3 are discharged. However, only *C*2 supplies the power when the power electronic switch *S*3 is OFF. Thus, the *C*2 will discharge power higher than that of *C*3. On the contrary, the power electronic switch *S*2 is switched in high frequency when dc capacitor voltage *VC*3 is more than dc capacitor voltage *VC*2. The voltage source *VCx* in Fig. 4(b) is dc capacitor voltage *VC*3. When the power electronic switch *S*2 is turned ON, both capacitors *C*2 and *C*3 are discharged. However, only *C*3 supplies the power when the power electronic switch *S*2 is turned OFF. Thus, *C*3 will discharge more power than that of *C*2. In this way, the voltage balancing of *C*2 and *C*3 can be achieved. As mentioned earlier, the balancing operation of power electronic switches *S*2 and *S*3 can be summarized as Table I.

The vol tages of capacitors *C*2 and *C*3 can be easily balanced when compared with the conventional multi-level inverter.

TABLE I
ON/OFF STATE OF *S*2 AND *S*3

		$\lvert v_s\rvert<V_{dc}/2$	$\lvert v_s\rvert>V_{dc}/2$
$V_{C2}>V_{C3}$	S_2	PWM	on
	S_3	off	PWM
$V_{C2}<V_{C3}$	S_2	off	PWM
	S_3	PWM	on

V. CONTROL & SIMULATION BLOCK DIAGRAM

The developed photovoltaic power generation system consists of a dc–dc power converter and the five-level inverter. The five-level inverter performs the operation of converting the dc power into the high-quality 'ac' power and injecting into the utility, also balancing of two dc capacitor voltages *VC*2 and *VC*3 and detecting the islanding operation. The dc–dc converter boosts the output voltage of the solar cell array and performs the MPPT to extract the maximum output power of the solar cell array. To verify the performance of the photovoltaic power generation system using the five-level inverter, a prototype based on the DSP controller of TMS320LF2407 A is developed and tested. The main parameters of the prototype are listed in Table II. The solar cell array consists of two strings, and each string contains eight solar modules connected in series. The capacity of solar cell array is 1.2 kW. So, the circuit configuration of the developed photovoltaic power generation system shown in Fig. 2 must be changed to Fig. 6. The switching operations of the replaced power electronic switches are complementary to those of power electronic switches *S*2 and *S*3, respectively. Accordingly, the five level inverter can supply active power and reactive power simultaneously.

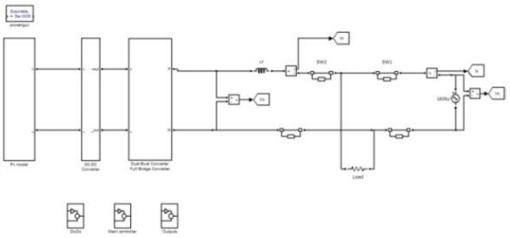
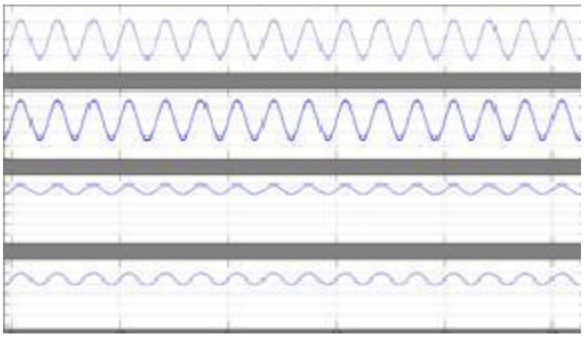


Fig.5.Simulation Control circuit diagram for Five Level Inverter for Renewable Power Generation System.

VI. SIMULATION RESULTS

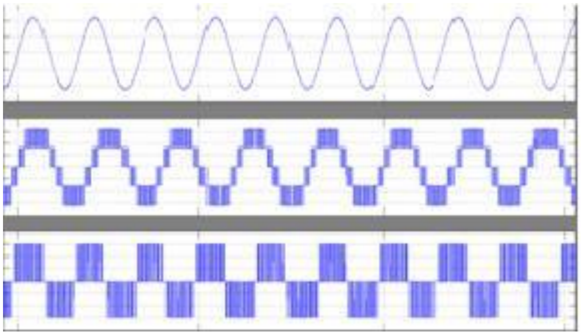
The performance of the photovoltaic power generation system using the five-level inverter proposed control system was evaluated with a detailed simulation model using the MATLAB/Simulink SimPowerSystems.

Results of the five-level inverter:-



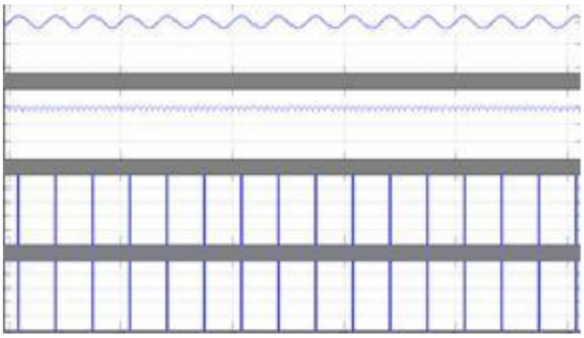
(a) Utility voltage. (b) Output current of the five-level inverter. (c) DC capacitor voltage VC_2. (d) DC capacitor voltage VC_3.

Results of the five-level inverter:-



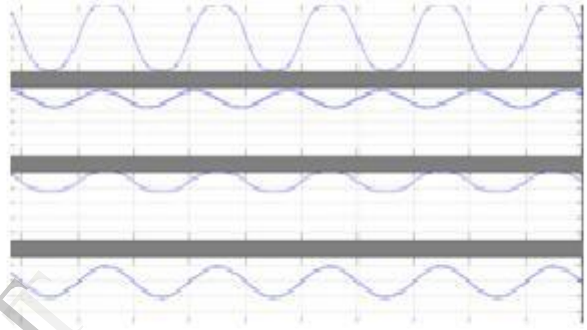
(a) Utility voltage. (b) Output voltage of the full-bridge inverter. (c) Output voltage of the dual buck converter

Results of the full-bridge inverter of the five-level inverter:-



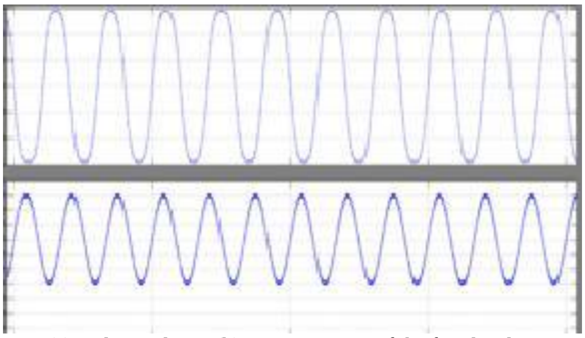
(a) Output current of the full-bridge inverter *io*. (b) Input current of the full bridge inverter *i*dc . (c) Driver signal of *S*4. (d) Driver signal of *S*5.

Results for the dc–dc converter of the developed photovoltaic power generation system:-



(a) Voltage ripple of dc capacitor C_2. (b) Voltage ripple of dc capacitor C_3. (c) Output voltage ripple of solar cell array. (d) Inductor current ripple of dc–dc converter.

Results for the developed photovoltaic power generation system under the distorted utility voltage:-



(a) Utility Voltage. (b) Output current of the five-level inverter.

VII. CONCLUSION

A photovoltaic power generation system with a five-level inverter is developed in this paper. The five-level inverter can perform the functions of regulating the dc bus voltage, converting solar power to ac power with sinusoidal current and in phase with the utility voltage, balancing the two dc capacitor voltages, and detecting islanding operation. This developed Five-Level reduces the Total Harmonic Distortion there by reducing the harmonics and hence improving the power quality of the system. The experimental results verify the developed photovoltaic power generation system, and thus the five-level inverter achieves the expected performance.

VIII. REFERENCES

[1] D. Puyal, L. A. Barragan, J. Acero, J. M. Burdio, and I. Millan, "An FPGA-based digital modulator for full- or half-bridge inverter control," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1479–1483, Sep. 2006.
[2] O. Lopez, F. D. Freijedo, A. G. Yepes, P. Fernandez-Comesaa, J. Malvar, R. Teodorescu, and J. Doval-Gandoy, "Eliminating ground current in a transformerless photovoltaic application," *IEEE Trans. Energy Convers.*, vol. 25, no. 1, pp. 140–147, Mar. 2010.
[3] B. R. Lin and C. L. Huang, "Implementation of a Shunt-series compensator for nonlinear and voltage sensitive load," in *Proc. IEEE Power Electron. Motion Control Conf.*, 2006, pp. 1–5.
[4] U. S. Selamogullari, D. A. Torrey, and S. Salon, "A systems approach for a stand-alone residential fuel cell power inverter design," *IEEE Trans. Energy Convers.*, vol. 25, no. 3, pp. 741–749, Sep. 2010.
[5] J.Gafford,M.Mazzola, J. Robbins, and G. Molen, "Amulti-kilowatt highfrequency ac-link inverter for conversion of low-voltage dc to utility power voltages," in *Proc. IEEE Power Electron. Spec. Conf.*, 2008, pp. 3707– 3712.
[6] T. H. Ai, J. F. Chen, and T. J. Liang, "A random switching method for HPWM full-bridge inverter," *IEEE Trans. Ind. Electron.*, vol. 49, no. 3, pp. 595–597, Jun. 2002.
[7] C. Y. Chen, Y. H. Lin, J. F. Chen, and R. L. Lin, "Design and implementation of DSP-based voltage frequency conversion system," in *Proc. Int. Symp. Comput. Commun. Control Autom.*, May 2010, pp. 435–438.
[8] M. Chithra and S. G. B. Dasan, "Analysis of cascaded H bridge multilevel inverters with photovoltaic arrays," in *Proc. Int. Conf. Emerging Trends Elect. Comput. Technol.*, Mar. 2011, pp. 442–447.
[9] N. Yousefpoor, S. H. Fathi, N. Farokhnia, and S. H. Sadeghi, "Application of OHSW technique in cascaded multi-level inverter with adjustable dc sources," in *Proc. Int. Conf. Electric Power Energy Convers. Syst.*, 2009, pp. 1–6.

IX. AUTHOR'S PROFILE

S.Naresh Kumar was born in Nandyal, A.P, India. He received the B.Tech (Electrical and Electronics Engineering) degree from the Madina engineering college, Kadapa in 2010: and Pursuing M.Tech (Electrical Power Systems) from the Global Engg college.

S.Naresh Siva Kanth was born in Kadapa, A.P, India. He received M.Tech (electrical power system) degree from Sree Vidyanikethan Engg college, Tirupati and B.Tech (electrical and electronics engineering) from Madina Engg college, Kadapa. Presently working as Asst.Proff in Global Engg college.

Mr.K.Siva Kumar, pursuing Ph.D from JNTUA, Anantapur. He received Post graduate from JNTUH, Hyderabad and graduate (EEE) from NBKR Institute of Science and Technology, Vakadu, Nellore District, affiliated to Sri Venkateswara University, Tirupathi. Presently working as an Associate Professor & Head of Department, Electrical and Electronics Engineering, Global College of Engineering and Technology, Andhra Pradesh, Kadapa.