International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 1 Issue 5, July - 2012

Multilevel Inverter For PV System Employing MPPT Technique

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Abstract

This paper presents a single-phase five-level PV inverter topology with dual reference modulation technique. Two reference signals identical to each other with an offset equivalent to the amplitude of the triangular carrier signals were used to generate PWM signals. Maximum Power Point Tracking (MPPT) is implementation in solar array power system with direct control method. The incremental conductance algorithm is used to track the MPP, as it performs better control under rapidly changing atmospheric condition. The Total Harmonic Distortion (THD) produced by the inverter is reduced. The proposed system is verified through simulation.

Keywords: Photovoltaic system, Maximum power point tracking (MPPT), Incremental Conductance (IncCond), PWM Multilevel Inverter

1. Introduction

The demand for renewable energy has increased significantly over the years because of shortage of fossil fuels and greenhouse effect. Among various types of renewable energy sources, solar energy and wind energy have become very popular and demanding due to advancement in power electronics techniques. Photovoltaic (PV) sources are used today in many applications as they have the advantages of being maintenance and pollution free. Solar-electric-energy demand has grown consistently by 20%–25% per annum over the past 20 years, which is mainly due to the decreasing costs and prices [1].

PV Inverter is used to convert dc power obtained from PV modules into ac power to be fed into the load. Improving the output waveform and performance of the inverter reduces its respective harmonic content and, hence the size of the filter used and the level of electromagnetic interference (EMI) generated by switching operation of the inverter [2]. In recent years, multilevel inverters have become more attractive for researchers and manufacturers due to their advantages over conventional three-level pulse width-modulated (PWM) inverters. They offer improved output waveforms, smaller filter size, lower EMI, lower total harmonic distortion (THD) [3]–[4].

The three common topologies for multilevel inverters are
1) Diode clamped (neutral clamped)
2) Capacitor clamped (flying capacitors) and
3) Cascaded H-bridge inverter

Several modulation and control strategies have been developed for multilevel inverters like multilevel sinusoidal (PWM), multilevel selective harmonic elimination, and space-vector modulation [3]. A typical single-phase three-level inverter adopts full-bridge configuration by using approximate sinusoidal modulation technique as the power circuits. The output voltage has zero, positive (+Vdc), and negative (−Vdc) supply dc voltage. The harmonic components of the output voltage are determined by the carrier frequency and switching functions. Therefore, their harmonic reduction is limited to a certain degree [4].

To overcome this limitation, this paper presents a five-level PWM inverter whose output voltage can be represented in the following five levels: zero, +Vdc/2, Vdc, −Vdc/2, and−Vdc. As the number of output levels increases, the harmonic content can be reduced. This inverter topology uses two reference signals, instead of one reference signal, to generate PWM signals for the switches. Both the reference signals Vref1 andVref2 are identical to each other, except for an offset value equivalent to the amplitude of the carrier signal Vcarrier. Because the inverter is used in a PV system, a proportional–integral (PI) current control scheme is employed to keep the output current sinusoidal and to have high dynamic performance under rapidly changing atmospheric conditions and to maintain the power factor at near unity. Simulation results are presented to validate the proposed inverter configuration.

2. Methodology

PV Model

The use of equivalent electric circuits makes it possible to model characteristics of a PV cell. The equations are implemented in MATLAB programs for simulations. The below fig 1.1 shows mathematical model of solar cell. It is used to vary the input voltage according to variation in temperature. The Mathematical model of solar cell is design based on the following equations.

Short circuit current at working conditions,
Isc=Isck*(1+(a*(Tak-Tref))

Reverse saturation current at reference temperature,

Iok=Isck/(exp(Vock/Vt)-1)

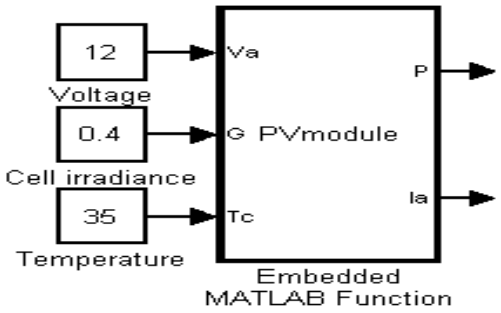

Fig 1.1 Mathematical model of Solar cell

Output current of the cell,
Ia=Iph-Io*(exp((Vc+Ia*Rs)/Vtc)-1)
Output power of the cell,
P=Va*Ia
Where,
Isc = short circuit current
Isck = short circuit current at reference temperature
Tak = Cell temperature in Kelvin
Tref = Reference Temperature(25 C) in Kelvin
Iok = Reverse saturation current at reference temperature
Vt = Thermal potential at reference temperature
Iph = photo current of the solar cell
Io = Reverse saturation current at working temperature
Vc = cell voltage per cell
Ia = output current of the cell
Rs = Series Resistance of the cell
Vtc = Thermal potential at working temperature

Five-level inverterTopology

The proposed inverter topology consists of a PV array, five-level H-bridge inverter and load as shown in fig1.2 The PV array generates DC supply through solar energy. The DC supply is applied to the five-level inverter through DC bus capacitor. The five-level inverter is used for conversion of DC to AC voltage. The AC voltage is connected to the load through the filtering inductor. The injected current must be sinusoidal with low harmonic distortion.

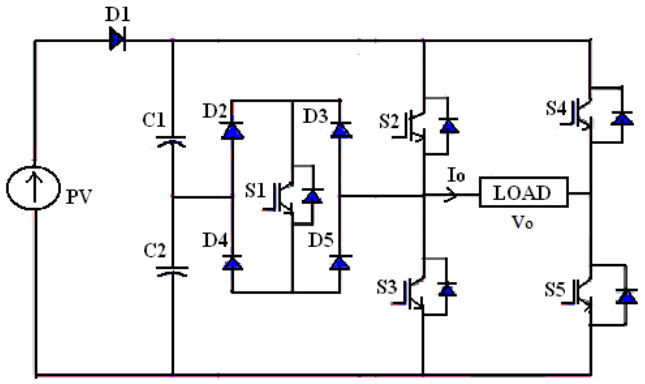

fig 1.2 single phase five level inverter

3. MPPT

Tracking the maximum power point of a photovoltaic array is usually an essential part of a PV system. As such many MPP tracking (MPPT) methods have been developed and implemented. Fig. 1.3 shows the characteristic power curve for a PV array. The problem considered by MPPT techniques is to automatically find the voltage V_{MPP} or current I_{MPP} at which a PV array should operate to obtain the maximum power output P_{MPP} under a given temperature and irradiance.
The various MPP tracking (MPPT) methods are

1. Hill climbing method
2. Perturb and observe (P&O) method
3. Incremental conductance method
4. Constant voltage method
5. Short-Circuit Current method

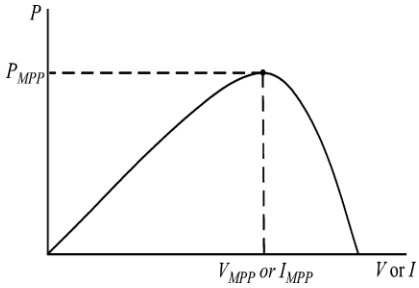

Fig 1.3 Characteristic PV array power curve

Incremental Conductance Algorithm

The incremental conductance method is based on the fact that the slope of the PV array power curve is zero at the MPP, positive on the left of the MPP, and negative on the right, as given by

dp/dv=0 at MPP
dp/dv>0 left of MPP
dp/dv<0 right of MPP

where,
dp=change in power ; dv=change in voltage

As power (P) =IV,

dp/dv=d(IV)/dv
dp/dv=I+v dI/dv
dp/dv=I+v ΔI/ΔV

above equation can be written as,

ΔI/ΔV= -I/V, at MPP
ΔI/ΔV>-I/V, left of MPP
ΔI/ΔV< -I/V, right of MPP

The MPP can thus be tracked by comparing the instantaneous conductance (I/V) as shown in the flowchart. Vref is the reference voltage at which the PV array is forced to operate. At the MPP, Vref equals to Vmpp. Once the MPP is reached, the operation of the PV array is maintained at this point unless a change in ΔI is noted, indicating a change in atmospheric conditions and the MPP. The algorithm decrements or increments Vref to track the new MPP.

The increment size determines how fast the MPP is tracked. Fast tracking can be achieved with bigger increments but the system might not operate exactly at the MPP and oscillate about it instead; so there is a tradeoff. In [5] and [6], a method is proposed that brings the operating point of the PV array close to the MPP in a first stage and then uses IncCond to exactly track the MPP in a second stage. By proper control of the power converter, the initial operating point is set to match a load resistance proportional to the ratio of the open-circuit voltage (Voc) to the short-circuit current (Isc) of the pv array. This two stage alternative also ensures that the real mpp is tracked in case of multiple local maxima. In [7], a linear function is used to divide the I-V plane into two areas, one containing all the possible MPPs under changing atmospheric conditions. The operating point is brought into this area and the Incremental Conductance is used to reach the MPP. Incremental Conductance technique is to use the instantaneous conductance and the incremental conductance to generate an error signal

$$e=I/V + dI/dV$$

From above equation, e goes to zero at the MPP. A simple proportional integral (PI) control can then be used to drive e to zero

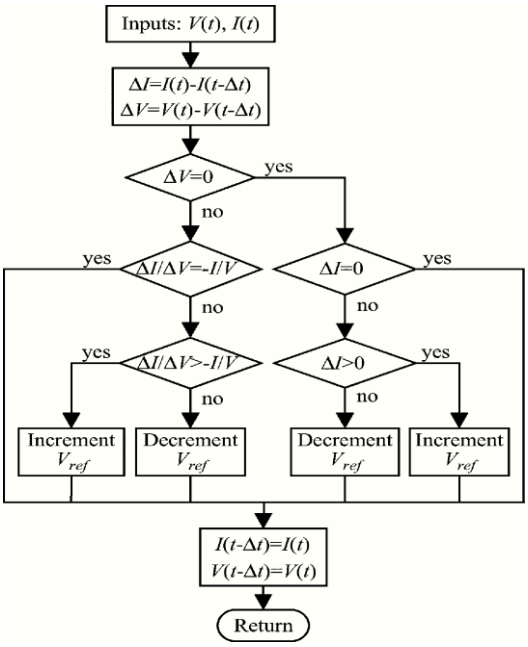

Fig 1.4 Incremental Conductance algorithm with direct control

4. Operational Principle of Proposed Inverter

A. Single phase five level inverter with control algorithm is implemented:

The principle of operation of the proposed inverter is shown in fig 1.5. to generate five-level output voltage, i.e., (0, +Vdc/2, +Vdc, -Vdc/2 and –Vdc). An auxiliary circuit which consists of four diodes and a switch S1 is used between the dc-bus capacitors and the full-bridge inverter. Proper switching control of the auxiliary circuit can generate half level of PV supply voltage, i.e., (+Vdc/2, -Vdc/2) [4]. Two reference signals Vref1 and vref2 will take turns to be compared with the carrier signal at a time. If Vref1 exceeds the peak amplitude of the carrier signal Vcarrier, Vref2 will be compared with the carrier signal until it reaches zero. At this point onward, Vref1 takes over the comparison process until it exceeds Vcarrier. This will lead to a switching pattern, as shown in fig 1.7 and 1.8. Switches s1-s3 will be switching at the rate of the carrier signal frequency, whereas s4 and s5 will operate at a frequency equivalent to the fundamental frequency. Following table 1 illustrates the level of Vinv during s1-s5 switch on and off.

S1	S2	S3	S4	S5	Vinv
ON	OFF	OFF	OFF	ON	Vpv/2 (positive)
OFF	ON	OFF	OFF	ON	Vpv (positive)
OFF	OFF (or) ON	OFF (or) ON	ON (or) OFF	ON (or) OFF	zero
ON	OFF	OFF	ON	OFF	Vpv/2 (negative)
OFF	OFF	ON	ON	OFF	Vpv (negative)

Table 1 (Inverter output voltage during S1-S5)

The proposed single-phase five-level inverter involves various steps of operation. The configuration and the principle of operation of the proposed inverter is given below. voltage produced by the arrays is known as Varrays. The voltage across the dc-bus capacitors is known as photovoltaic voltage.

B. Modes of operation:

The proposed single-phase five-level inverter involves steps of operation. The five level PWM inverter is shown in fig 1.6.

Maximum positive output (+vdc):
Switch 1 is ON, connecting the load positive terminal to Vdc,

and switch 5 is ON, connecting the load negative terminal to ground. All other Switches are OFF; the voltage applied to the load terminal is Vdc.

Half-level positive output (vdc/2):
The auxiliary switch, switch 1 is ON, connecting the load positive terminal through D2 and D5, and Switch 5 is ON, connecting the load negative terminal to ground. All other controlled swiches are OFF; the voltage applied to the load terminals is Vdc/2.

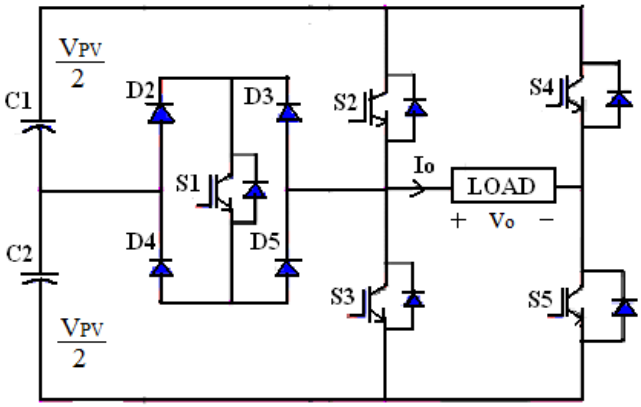

Fig 1.6 proposed single–phase five level PWM inverter

Zero output voltage:
The two main switches 3 and 5 are ON, short-circuiting the load. All other controlled switches are OFF; or the main switch 2 and 4 are ON, short circuiting the load. All other controlled switches are OFF; the voltage applied to the load terminals is zero.

Half-level negative output (-vdc/2):
The auxiliary switch, switch 1 is ON, connecting the load positive terminal through D4 and D3, and Switch 4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is -Vdc/2.

Maximum negative output (-vdc) :
Switch 4 is ON, connecting the load negative terminal to Vdc, and switch 3 is ON, connecting the load positive terminal to ground. All other Switches are OFF; the voltage applied to the load terminal is (-Vdc).

Switching patterns of the proposed single phase five-level PWM inverter

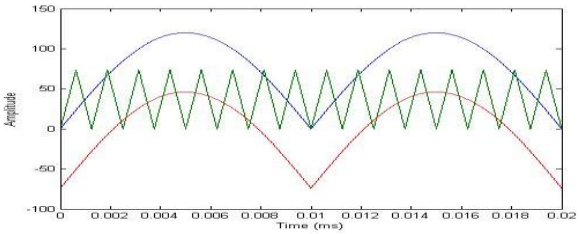

Fig 1.7 carrier and reference signals

The pulse generation for different switches by carrier with two reference signal as shown in fig 1.7.

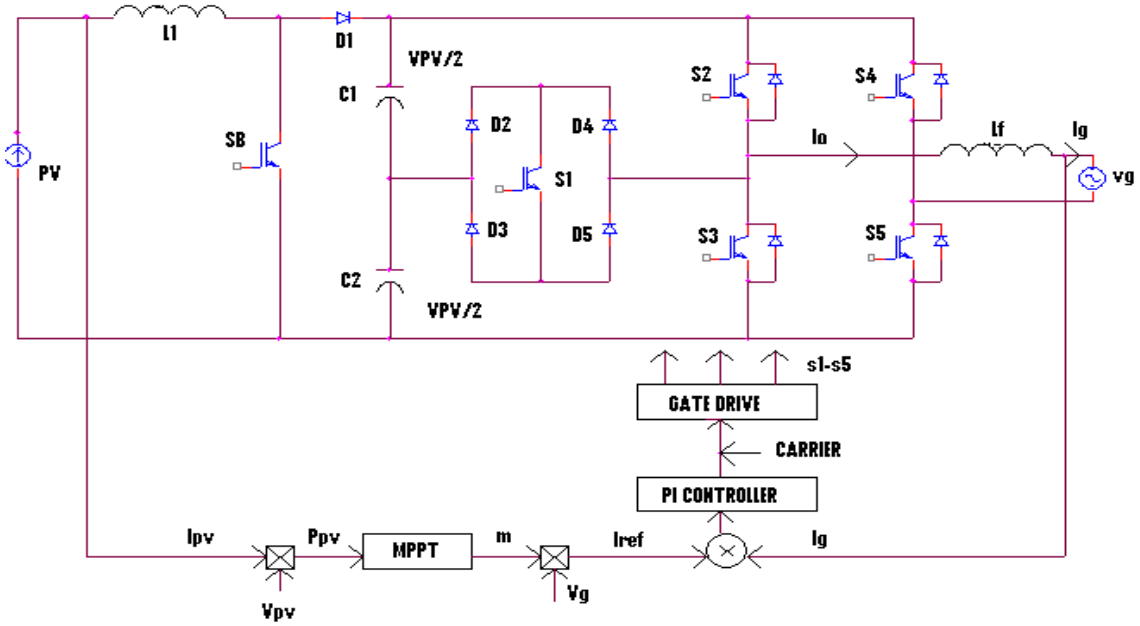

Fig 1.5 Five-level inverter with control algorithm implemented

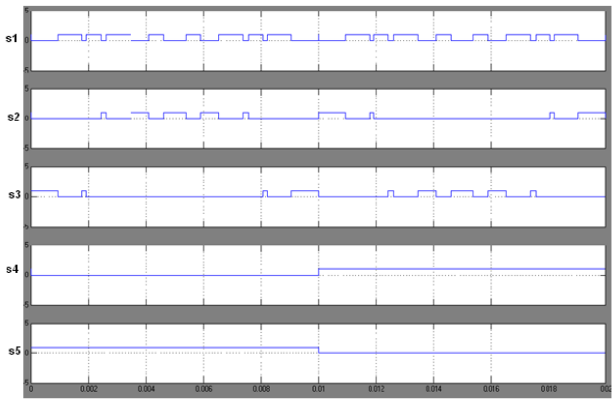

Fig 1.8 Switching pattern for the single-phase five-level inverter

5. Simulation Circuit and Result

The simulation circuit for proposed single-phase five-level inverter topology is shown in Fig1.9. Simulations were performed by using MATLAB SIMULINK and it also helps to confirm the PWM switching strategy. Fig 1.7 and 1.8 shows the PWM switching strategy used in this paper. It consists of two reference signals are compared with the triangular carrier signal to produce PWM switching signals for switches S1-S5. The inverter adopts a full-bridge configuration with an auxiliary circuit. PV arrays are connected to the inverter via a dc–dc boost converter.

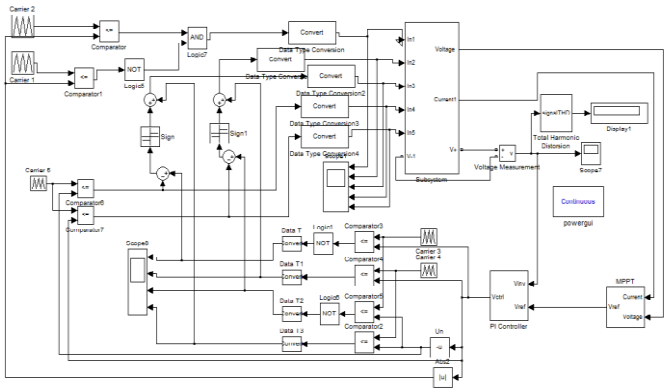

Fig 1.9 overall simulation circuit

The dc–dc boost converter is used to step up inverter output voltage to ensure power flow from the PV arrays into the load. A filtering inductance Lf is used to filter the current injected into the load. The injected current must be sinusoidal with low harmonic distortion. In order to generate sinusoidal current, sinusoidal PWM is obtained by comparing a high-frequency carrier with a low-frequency sinusoidal, which is the modulating or reference signal. The carrier has a constant period; therefore, the switches have constant switching frequency. The switching instant is determined from the crossing of the carrier and modulating signal.

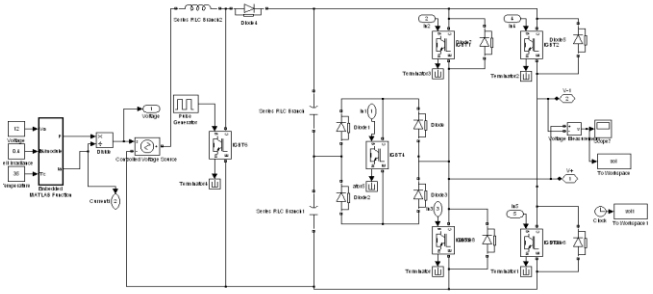

Fig. 1.10 power circuit

Simulation Results

The simulated Inverter output voltage (Vinv) for $0.5 \leq M \leq 1$. is shown in fig 1.11. This output was observed from single phase five-level inverter.

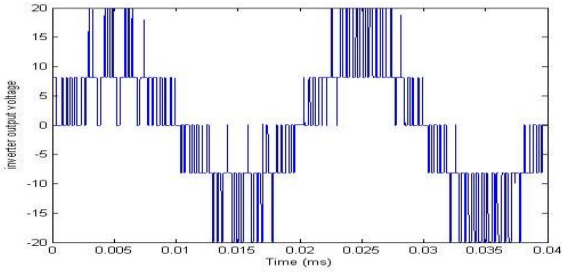

Fig 1.11 inverter ouput voltage

The Total Harmonic Distortion is shown in fig 1.12. and the harmonics are reduced to 10.37%

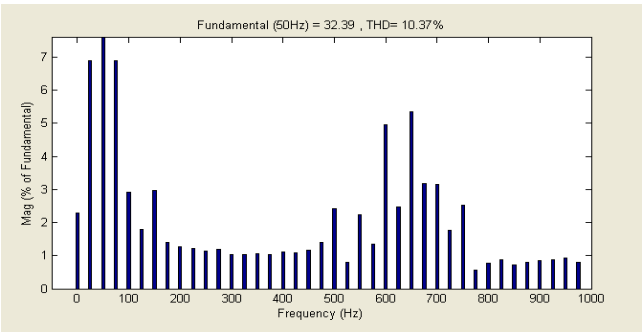

Fig 1.12 THD result of the proposed multilevel PV inverter voltage

Specifications

PV MODULE CHARACTERISTICS

Max Power	: 75w
Short Circuit Current, Isc	: 4.8A
MPPT Current, Imppt	: 4.4A
Open Circuit Voltage, Voc	: 21.7V
MPPT Voltage, Vmppt	: 17.0V

6. Hardware Description

In order to assess the performance of the proposed MPPT based PV power system, as shown in fig.1.13 is designed . In this prototype, module consists of PV panel, boost converter and five-level inverter (MOSFET IRFZ44), MOSFET Driver circuit and PIC microcontroller. Control algorithm is implemented in PIC Microcontroller, to maintain constant Inverter output voltage.

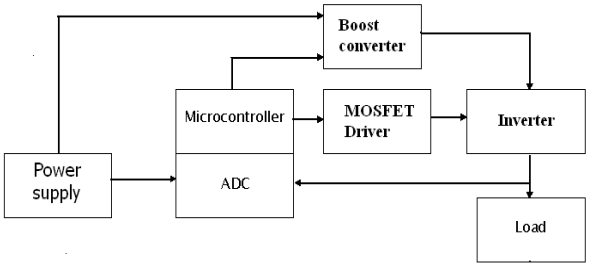

Fig. 1.13. Block diagram of the Prototype

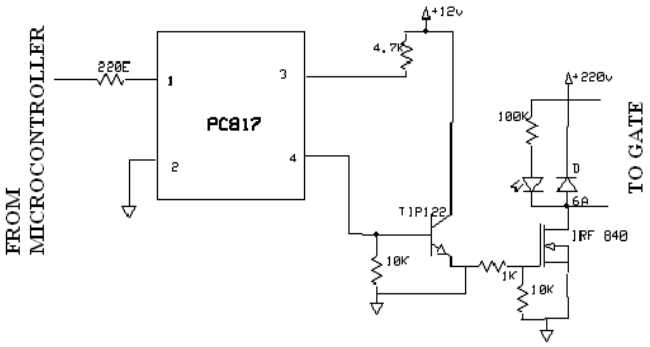

fig.1.14 MOSFET driver circuit

PC817 optocoupler consists of LED and photo diode. TIP 122 is a NPN transistor its collector is connected with the +12V and Emitter is connected with the ground. It is placed between optocoupler and FET because signal from optocoupler is not sufficient to run a FET. This drive is suitable for high current applications. MOSFET driver circuit is shown in fig.1.14. PIC microcontroller is the first RISC based microcontroller fabricated in CMOS (complimentary metal oxide semiconductor) that uses separate bus for instruction and data allowing simultaneous access of program and data memory. The main advantage of CMOS and RISC combination is low power consumption resulting in a very small chip size with a small pin count. Flash technology is used in PIC16F877, so that data is retained even when the power is switched off. Easy programming and Erasing are other features of PIC 16F877.

7. Conclusion

This paper presented a single phase multilevel inverter for PV application. It utilizes two reference signals and a carrier signal to generate PWM switching signals. The circuit topology, modulation law and operational principle of the proposed inverter were analyzed in detail. Simulation results indicate that the THD of the five-level inverter is much lesser than that of the conventional three-level inverter.

ACKNOWLEDGMENT

The authors thank the Management of Vickram College of Engineering for providing infrastructure to implement the project.

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International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278 - 0181

(ESRSA Publication)

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