Multiple Single Input Change Test Vectors and Its Application Over Built In Self Testing

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Abstract

This concept gives the generation of well advanced test pattern generation (TPG) for the built in self test techniques. This method generates multiple single input change (MSIC) vectors, so that each vector to the scan chains is of a single input change (SIC) ,thus when there are multiple scan chains, there occurs the generation of MSIC vectors. For the MSIC vector generation, the use of the devices such as the Reconfigurable Johnsons Counter and Scalable SIC Counter is being used. As a result, the sequences of minimum transitions have been obtained. Both the test per clock and test per scan are flexible to the Scalable SIC Counter for the vector generation. This method save the test power and give a better fault coverage without an increase in the test length. The analysis results in a low input transition and uniform pattern distribution.

Keywords: Built In Self Test (BIST), Single Input Change (SIC), Test Pattern Generator (TPG), Low Power.

1. Introduction

The circuit under test (CUT) is introduced with an on chip test hardware to give the BIST to reduce the complexity in VLSI testing. It uses the principle of linear feedback shift register (LFSR). The CUT suffers from high switching activity due to the pseudorandom test pattern generated by the LFSR. This also leads to power loss. The LFSR is also required to produce long pseudorandom sequences to have high fault coverage. There is a chance of damaging the circuit and decrease the product yield and life time.
The switching activity during each shift from one scan cell to another is being decreased. The paper has got the following merits

a. Minimum transition: The vectors are of SIC to each scan chain to minimize the transition also to minimize the transition and also to lower the test power.
b. Uniform pattern distribution: The test patterns are distributed uniformly to each and every scan chains at every clock.
c. Pattern uniqueness: No vectors are being repeated.
d. Low hardware by extra TPG'S: The hardware to implement the TPG's are very low.

2. Proposed MSIC-TPG

This is the TPG of converting a SIC vector of low transition for a number of scan chains in a unique manner, a SIC generates, a clock and a control block.

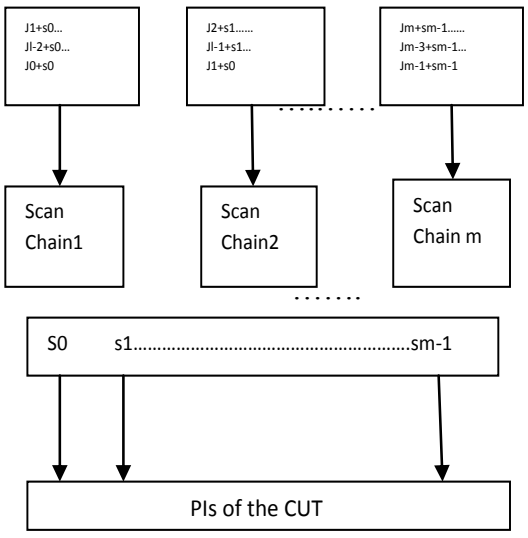

Figure 1. Symbolic representation of MSIC Patterns

3. MSIC Vector Generation Through Reconfigurable Johnsons Counter and Scalable SIC Counter

The given work mainly consists of a test pattern generation method given by a Reconfigurable Johnson Counter. The following methods are the way to generate the test vectors in a Reconfigurable Johnsons Counter:

a. Initialization
b. Circular shift register
c. Normal mode

3.1. Method of Test Pattern Generation

Consider there are 'm' primary inputs (PI's) and 'M' scan chain has 'l' scan cells. The vectors $S(t)=S_0(t)S_1(t)S_2(t)\ldots\ldots\ldots\ldots S_{m-1}(t)$ are the ones generated by an m-bit LFSR. Here, the bit of LFSR is known to be a seed. The Johnson Counter releases get XORed with $S=S_0\ S_1\ S_2\ldots\ldots\ldots\ldots\ldots S_{M-1}$ and the result is $X_1X_{l+1}X_{2l+1}\ldots X_{(M-1)l+1}$ gets shifted to the chains. During 2nd clock cycle, $J=J_0J_1J_2\ldots\ldots..J_{l-1}$ is circularly shifted in the form of $J=J_{l-1}\ J_0\ J_1\ J_2\ \ldots\ldots\ldots J_{l-2}$, again XORed with $S=S_0S_1S_2\ldots\ldots S_{M-1}$. The resultant vectors $X_{2xl+2}\ X_{2l+2}\ldots..X_{(M-1)l+2}$ is shifted to 'M' scan chains. The chains are loaded after 'l' clocks in a unique way. Since the Reconfigurable Johnsons Counter can generate the codewords through the circular shift, the counter is circular Johnson Counter is called as a linear sequential decompressor.

3.2. Reconfigurable Johnson Counter

For smaller scan length, a Reconfigurable Johnson Counter is developed to generate a SIC sequence in the time domain. It is SIC Generator with three operation modes:

a. Initialization mode: When RJ mode= '1' and Init='0', the counter will be initialized to all zero states by clocking CLK2 more than 1 times.
b. Circular shift register mode: When RJ=Init='1', each stage of the Johnson Counter will output a Johnson codeword by clocking CLK2 1 time.
c. Normal mode: RJ mode='0', the Reconfigurable Johnson Counter will generate 2l unique SIC vectors by clocking CLK2 2l times.

3.2.1. Limitations. The above work has an ability to do the testing of a small range of circuits. The large test bit range is generated by the scalable SIC Counter. It has also the merit of overcoming the delay of testing.

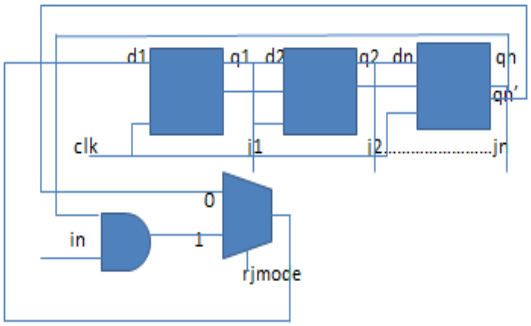

Figure 2. SIC Generators. a. Reconfigurable Johnson Counter

3.3. Scalable SIC Counter

When the scan chain number 'M' is smaller than scan chain length 'l', a counter known as the Scalable SIC Counter is being developed. It consists of a k-bit adder and a subtractor with a clocking SE signal, and a k-bit subtractor with a clocking SE signal along with a shift register, both clocked by CLK2. Also contains 'k' multiplexers. The SE signals enables the k-bit adder to generate the number of 1s (0s) towards the shift register to be filled. The output waveform of the counter is to be shown in the simulated result. The three operation modes are shown below:

a. If SE=0, the adder count is stored to the subtractor. But when SE=1, the k-bit subtractor contents reduces to all zeros gradually.
b. When SE=1, the subtractor contents are decreased, but not to all zeros.
c. The needed 1s and 0s are shifted to the register by clocking CLK2l times and the unique codewords are applied to the chains.

The full design, ISCAS'89S13 with scan length as 64. 6 D-flip flops are meant each for the adder as well as the subtractor, 10 for a 10-bit shift register meant for the 10 scan chains, 19 combinational logic gate along with 6 multiplexers to build the Scalable SIC Counter. In total, there are 204 gates. To implement a 64-bit Johnson Counter, it requires the 64 D-flip flops of 428 gates. The MSIC-TPG overhead is reduced by a Scalable SIC Counter.

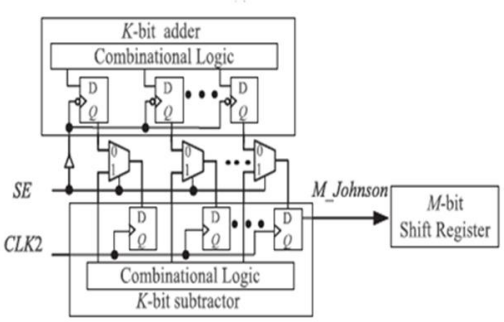

Figure 2. b. Scalable SIC Counter

4. MSIC –TPG for Test pet clock

The inputs of the XOR gate tapped from a seed generator and Johnson Counter outputs. The XOR gate output is fed into the PI's of CUT. The testing undergoes the following methods:

a. When a clock is given for one time from the CLK1, the seed generator generates a new seed.
b. Similarly the Johnson Counter also generates a new vector by a clock CLK2.
c. Repeating the above step until a 2l number of Johnson vectors are produced.
d. Repeat for an expected fault coverage.

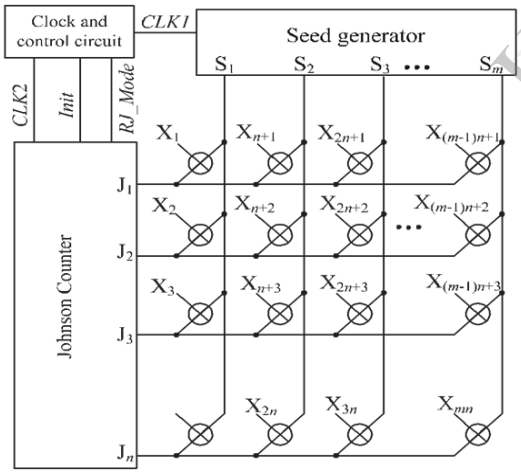

Figure 3. MSIC-TPGs for test per clock.

5. MSIC-TPG For Test per Scan

The XOR gate input is from the seed generator and also from the SIC Counter and their output are Given below is the test procedure:

a. A new seed is generated by the seed generator.
b. When RJ mode is '0', then the Johnson Counter will operate in a normal mode to generate the vector by giving a clock CLK2.
c. After that, both the RJ mode and the Init is set to '1', so that a circular shift register mode is being activated for producing 'l' codewords by clocking CLK2 l times.
d. Repeat for 2l vector generation for an expected fault coverage.

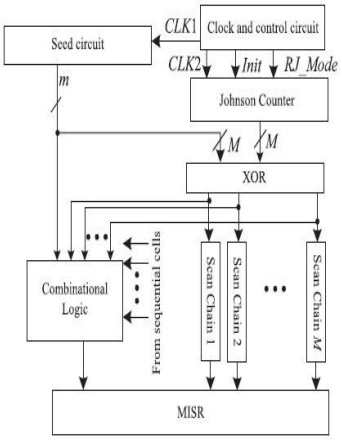

Figure 4. MSIC-TPGs for test per scan

6. MSIC Sequences Properties

6.1. Reduction in Switching Activity

'M' unique sequences are applied to the 'M' PIs of CUT in the test per clock. Where as in the test per scan, the CUT's PIs are kept unchanged during the shifting and for each transition, the codewords are not greater than '2'. A higher reduction ratios are shown when the methods given in the references [] and [] have been compared.

6.2. MSIC Pattern Uniform Distribution

The repetition of the input patterns indicates the non-uniformity. It can result in low fault coverage if there is an absence of the patterns which is only capable of detecting the particular fault coverage. Uniformity is meant for high fault coverage. The initial seed has less impact on this kind of uniform distribution.

6.3. Test Length and Fault Coverage Relationship

Initial test vector is related to the test length of a conventional LFSR. To achieve a full fault coverage, it depends upon the initial vector in conventional LFSR TPGs. The fault model available is a stuck at fault model. There are two types of LFSR sequences such as the best case and the worst case LFSR sequences. The growth rate of

fault coverage with the MSIC sequence is close to that with the LFSR in the best case. The uniform distribution of MSIC pattern alleviates the depending relationship between the TPG's initial state and the test patterns.

7. Simulation Result

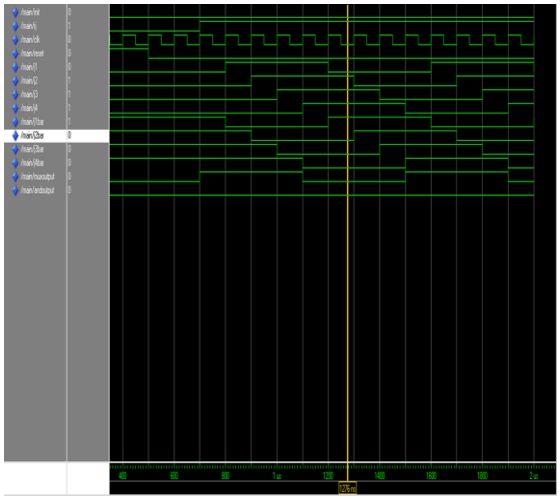

Figure 5. a. Simulation result of Reconfigurable Johnson Counter.

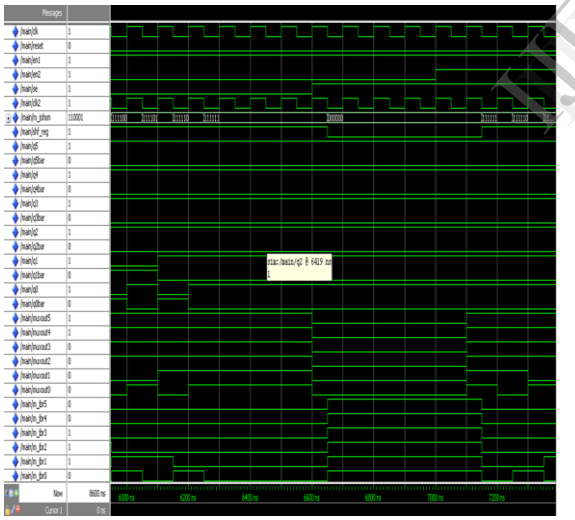

Figure 5. b. Simulation result of Scalable SIC Counter.

8. Result Analysis

The comparison of the estimated power of a 4-bit LFSR is done with that of the 4-bit Reconfigurable Johnson Counter. In the same way, a 6-bit LFSR is being compared with a 6-bit Scalable SIC Counter on the basis of its power and thermal energy. The table representing the above mentioned concept is showed below.

	4-bit LFSR	4-bit Reconfigurable Johnson Counter	6-bit LFSR	6-bit Scalable SIC Counter
Total Estimated Power (mW)	113	107	234	208
Estimated Juncction Temperature (^{0}C)	27	27	29	28
Ambicat Temperature (^{0}C)	25	25	25	25
Case Temperature (^{0}C)	27	27	28	28

Table 1. Result Comparison

9. Conclusion

This paper is based on a low power test pattern generation that is implemented easily by the hardware. The results showed that the MSIC had the uniform distribution, low input transition density. A flexible test per scan and test per clock schemes can be developed with the combinations of Reconfigurable Johnson and Scalable SIC Counters.

In future work, the seed generator is being replaced by the CMOS Parallel Counter. It works under the principle of a look ahead logic. In a look ahead logic, there occurs a generation of the partial product in the TPG. As a result, there is maximum time conversation and no delay for the switching activity.

10. References

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