Nano-scale Silicon MOSFETs

Comparison at 45 nm and 180 nm technology

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Abstract- ***As CMOS technology dimensions are being aggressively scaled to reach a limit where device performance must be assessed against fundamental limits, nanoscale device modelling is needed to provide innovative new MOS devices as well as to understand the limits of the scaling process. This paper describes advanced modelling of nanoscale MOSFETs from the viewpoint of device physics, which consists of three parts ±gate, source/drain, and channel modelling.***
At the same time, there has been concurrent scaling of supply voltage in concert with device dimensions to keep power manageable and in order to meet reliability requirements. For logic devices, increased power consumption is a big concern with increases in clock speed. The reduction of the supply voltage is the most effective method to reduce the power. However, reduced drive current for high speed circuit operation offsets gains due to power reduction.
In this paper, we will compare Nano-scale Silicon MOSFETs at 45 nm and 180 nm technology.

Keywords [2] ***Ballistic transport; Charge carrier mobility; double gate MOSFETs; semiconductor device modelling; scattering; and quantum effect; Monte Carlo simulations; parasitic capacitances; FinFET.***

I. INTRODUCTION

To improve the performance, continuous CMOS scaling has been the main driving factor of silicon technology. Prospects of the scaling beyond the 2001 ITRS [1] projections, i.e., into the sub 10 nm region, are of primary importance for future electronics. Several important theoretical studies of nanoscale double-gate MOSFETs have been published; however most of them cannot be used for predictions of device performance below 10 nm. A study of MOSFET with double gate gives the highest value of V-I characteristics under the ballistic conditions i.e. the ballistic mode is the ultimate goal to be achieved for small channel device when the scattering effects are eliminated. The model approaches and the device dimensions are driving in parallel to support the semiconductor technology as a trade-off between accuracy and simplicity is taking place. Extracted model describes current-voltage characteristics from linear to saturation operating regions with single V-I expression and guarantees the continuities of Vds - Ids and their derivative throughout voltage bias conditions including the thermal effect [2]. In Figure 1 shows a generic planer style of double gate n-MOSFET that is been used for this work. The channel region is controlled by two symmetrical gates at top and bottom. Recently, a more general approach based on one equilibrium Greenôs functions was used to calculate some characteristics of nanoscale MOSFETs [3], [4], [5].

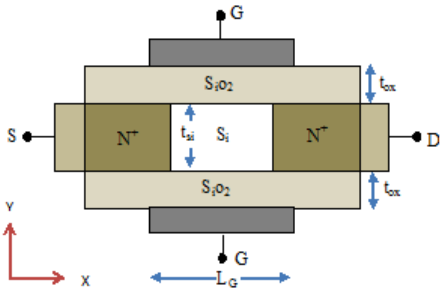

Figure 1. Schematic representation of symmetrical Double Gate MOSFET used as the model device in this paper

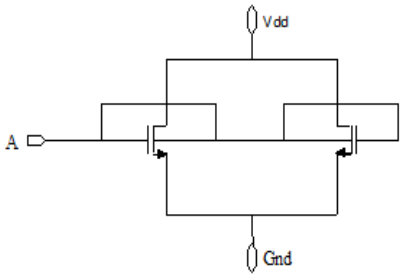

Figure 2. Schematics of double gate n-MOSFET

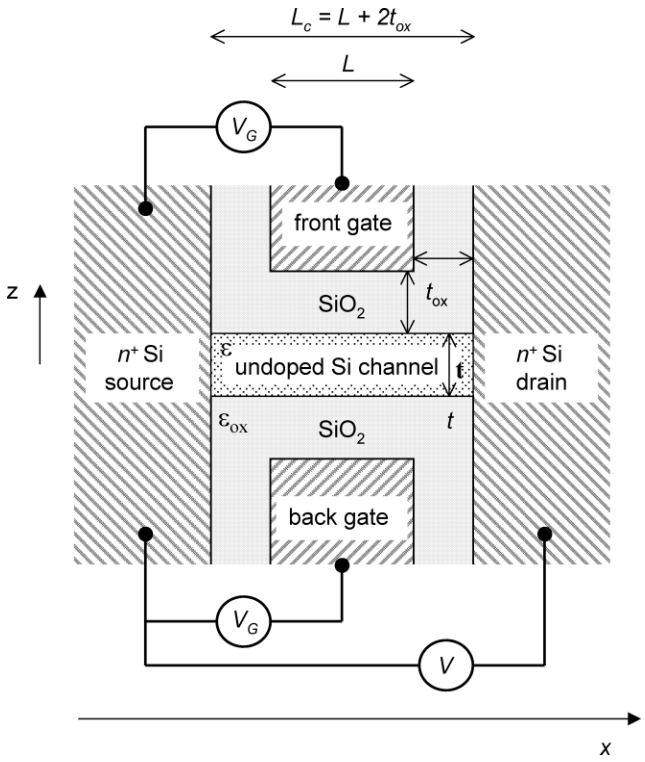

Fig. 3. A simple model of double-gate MOSFETs with ultrathin intrinsic channel. Notice the difference between the gate length L and channel length Lc.

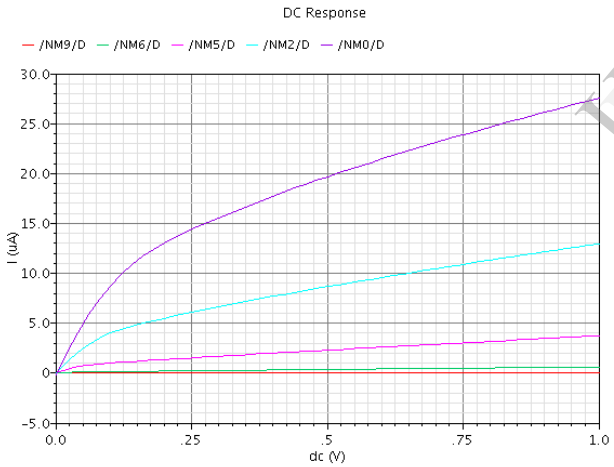

Figure 4.V-I characteristics of double gate n-MOSFET at 45 nm Technology.

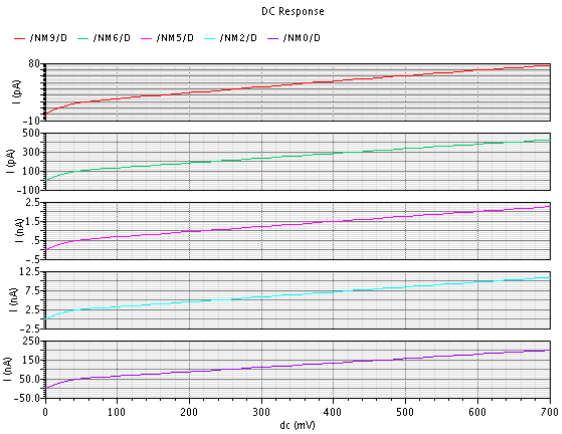

Figure 5.V-I characteristics of double gate n-MOSFET at 180 nm Technology.

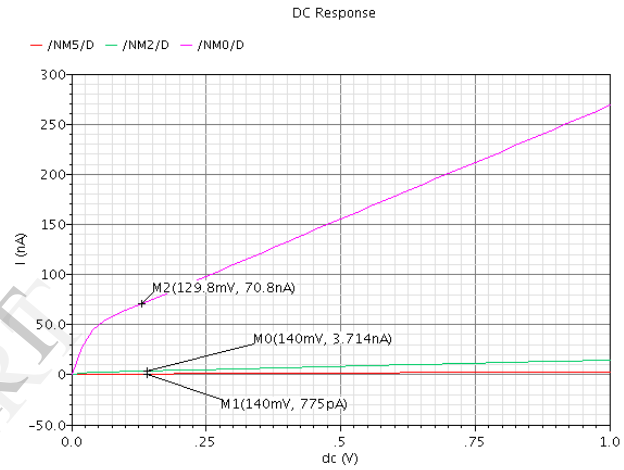

Figure 6. V-I characteristics of double gate n-MOSFET on different voltages0.1v, 0.2v and 0.36v proposed at 45 nm technology

The V-I characteristics results is very much limited in the nanoscale range, because of the extracted parameters are the extent value of the device performance. The channel potential of the transistor controlled the carrier transmission. Carrier with lower energies can travel from source to drain only by tunnelling quantum mechanically through the channel potential barrier. Natori and others [6] have developed models for ballistic transistor in n-channel MOSFETs.

II. HISTORY OF COMPACT MODELING AND FUTURECHALLENGES

Semiconductor device models come in many fundamental forms, from being purely data-driven, such as table look-up models, to being based on extremely detailed physics, such as numerical Monte Carlo simulations. The latter are too computationally burdensome for circuit simulation, the former can be useful when no physically-based model for a device

exists or for speeding up simulations, but do not provide a basis for practical circuit design; they do not naturally scalability, temperature dependence, encompasses geometric statistical variability(including mismatch),or retargeting compact models aim to include enough of the fundamental physics of device operation to enable simulation of these aspects of device behaviour, yet to be computationally efficient.

III. MODELING FOR EMERGING PHYSICAL EFFECTS

This section presents modelling techniques for new physical effects at 45nm and below.

A. Proximity Effects

A reality of dense, state-of-the-art CMOS technologies is that the electrical performance of an individual circuit element does not just depend on its own geometry: The adjacent environment affects the behaviour of a device. Historically this first became apparent in parasitic capacitances, where adjacent structures affected the fringe and coupling capacitances of a device. More recently it has become well-known that adjacent isolation and well edges have a significant effect on device performance. To incorporate all details of proximity in modelling device performance is unrealistic; evaluation of complex layouts shows that 10ôs to 100ôs of layout/adjacency details affect the electrical behaviour of one device. The industry has therefore moved to an approach where three geometric moments are calculated from layout and passed as instance parameters to a model, and the compact model then adjusts parameters such as V_{TH} and mobility appropriately [7][8]. This is a good example of where the complexity of the situation has meant that a deliberate choice was made to not include n_{th} order physics as it would have been impractical. Nevertheless, there are still some significant oversights in modelling well proximity effects (WPE). [9] Shows that well proximity can induce significant (up to 8%) asymmetry in current from source-drain reversal, yet this is not encompassed by existing models, and adding modelling of this asymmetry is not being pursued at present.

B. Non-Classical Materials and Structures

A high-*k* gate dielectric and metal gate structure has been adopted for IC production at the 45nm technology node. High *k* dielectrics help reduce gate leakage and allow more aggressive scaling of gate dielectrics than silicon oxide, while the metal gate is necessary to tune the threshold voltage. However, introduction of high-*k* dielectrics comes at the expense of transistor reliability. Consequences include a larger amount of NBTI and faster degradation of the drain current. Additional compact models need to be developed to account for this instability and to support the design for reliability.

Beyond the 32nm technology generation, more radical solutions will be vital to meet the scaling criteria of off-state leakage. The FinFET, or the double-gate device (DG), is considered as the most promising technology of choice [10]. Fig. 4 shows the structure of a FinFET device. FinFETs are electro statically more robust than bulk CMOS transistors since two gates are used to control the channel. At the 32nm node, it may improve the ON/OFF current ratio by more than 100% [11]. Extensive research has been conducted to understand the underlying physics. Yet a compact model for DG devices, akin to BSIM and PSP for bulk CMOS transistors, has not been standardized. As noted above, this is an active area of compact modeling research at present.

IV. CARRIER TRANSPORT

The transport of the carrier through the semi-conductor channel can be thought of as a motion of a person in a crowded place. If there are a lot of people (scattering centres) to collide with, then the average velocity of the person (carrier) is less; whereas, if the density of people (scattering centre) is less, the average velocity can be very high. In a semiconductor channel, scattering is mainly due to the presence of impurity atoms, lattice vibrations of the atoms, surface scattering and other crystal defects.

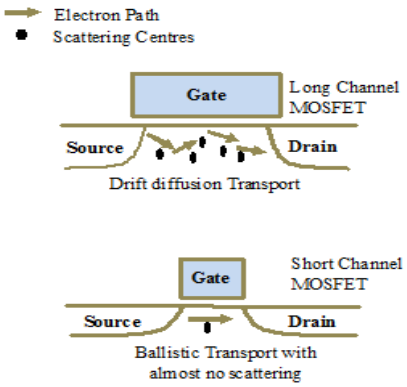

Figure 7.Carrier Transport in a long and a ballistic MOSFET.

V. MOBILITY VERSUS DRAIN CURRENT RELATION

The effective mobility of inversion layer carriers is an important parameter in traditional theories of MOSFETs. Simple expressions developed from a scattering theory of the MOSFET provide a quantitative relation between the long channel mobility and the short channel drain current.
Scattering theory of the MOSFET is used to develop a simple, quantitative expression that relates the linear and saturated drain currents of a nanoscale MOSFET as [12],

$$I_{Dlin} = WC_{ox}\frac{V_T}{2kBT/q}[1 - r_{lin}](V_{GS} - V_T)V_{DS}$$

$$I_{Dsat} = WC_{ox}V_T\left[\frac{1-r_{sat}}{1+r_{sat}}\right](V_{GS} - V_T)$$

Where, VT and r are the unidirectional thermal velocity and channel backscattering coefficient. These expressions assume to be non degenerate carrier statistics. In the linear and saturation regions,

$$r_{lin} = \frac{L}{L+\lambda_0}$$

$$r_{sat} = \frac{\ell}{\ell+\lambda_0}$$

Where ə₀ = is the near-equilibrium mean-free-path for backscattering, L the channel length and ă a critical length for backscattering under high bias conditions. In the expressions, ə₀ is deduced from the measured carrier mobility in a corresponding long channel MOSFET where mobility is a well-defined parameter. The low and high ə₀ drain currents of a nanoscale MOSFET are directly related to ə₀. The critical distance ă is roughly the distance for the first $2K_BT/q$ of potential drop in the channel, typically a small portion of the physical channel length L.

VI. DISCUSSION

The observed double gate n-MOSFET is accomplished with the virtuoso tool of cadence. Spectra simulator of cadence is used for simulation of the output. The simulations are performed using the 45 nm and 180 nm technology.

Technology	Average Power	Leakage Current	Leakage Power
45 nm	46.18×10^{-6}	5.17×10^{-6}	3.619×10^{-6}
180 nm	163.2×10^{-3}	1.51×10^{-3}	11.9×10^{-3}

VII. CONCLUSION

Numerical simulation-aided study with optimal 45 nm and180 nm double gate n-MOSFET device is presented. In ultimately scaled technology, CMOS circuit leakage power would be significantly reduced by double gate n-MOSFET devices. Due to many factors involved such as, the carrier transport in the channel with velocity overshoot and the quantum mechanical as well as scattering effects are dominate in nanoscale transistor characteristics.

The study showed that the scattering effect and the quantum effects in the low drain field which intern plays an important role for controlling the V-I characteristics.

We had compared a nanoscale ówell-temperedô MOSFET with channel length of 45 nm and 180 nm technology on the basis of Average power, leakage current and Leakage power and illustrate that in the tabular form.

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