

Network Design Using Aflawlessagent Based Management Method

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Abstract:As of today's network architecture the complexity is very high and the usage of cores in each chip is very large and hence these factors are becoming an important issue to maintain the reliability factors. The agent based architecture proposed here will maintain the performance and reliability of the network based chips and this architecture proposed here will have higher tolerance towards the faulty links and router. To utilize the best possible available resources the fault information is classified and enlightened among the neighboring units. The designed architecture has only small extra hardware architecture.

Keyword:*Soc, links, router, Agent based management method, CMP, clusture, cell agent.*

I. INTRODUCTION

The network on chip is found to be more reliable when used with Chip Multi-Processors (CMP) which have been designed and used to overcome the intrinsic design challenges in order to handle the large processing requirements. CMPs units may include hundreds of Intellectual Property (IP) cores, processing elements and embedded memory blocks to communicate with each other.

When the number of nodes in the network increases the reliability, power consumption and thermal issues becomes an important factor. The reliability aspect of the network is the crucial consideration to be made. This aspect includes the proposed agent-based management structure and a routing method which is exploited to tolerate permanent faults in the nodes and links by using an agent. So the fault tolerances against permanent faults are also considered since a considerable amount of device failures may occur in both manufacturing and operational phases. To tolerate permanent faults many fault-tolerant routing algorithms have been designed so far. However, because of the size of CMPs and network architecture, we only consider distributed and scalable routing algorithms. The agent-based architecture consists of agents in a hierarchical structure, which is especially suitable for large CMPs. This structure where the agents in each level of hierarchy have the same tasks to gather, manage and distribute the fault information among the neighboring units.

The Mesh network topological structure is used to evenly distribute the fault information and make sure the information is made to reach each and every node. So the appropriate information of the fault information will be sent to the direct and indirect neighbor nodes through the agents to be used in the routing process. This way, a scalable and fault-aware routing algorithm is achieved with higher performance compared to methods without agent-based management.

II. RELATED WORK AND CONTRIBUTIONS

Warsaw, in May 24-26, 2012. explained the complexity of evolving integrated circuits and the number of cores in each chip increase, reliability aspects are becoming an important issue in complex chip designs. The on-chip network architecture that incorporates a novel agent-based management method to enhance the reliability and performance of network-based Chip Multi-Processor (CMP) and System-on-Chip (SoC) are designed against faulty links and routers. In addition, to utilize the fault information required for the routing process in a scalable manner, we classify the fault information to be exploited in the proposed distributed and hierarchical management structure. The experimental results show that the proposed architecture incurs only a small hardware overhead [1].

“O. Cesariow, MODERN SYSTEM-ON-A-CHIP (SoC) design shows a clear trend toward integration of multiple processor cores. The SoC system driver section of the International Technology Roadmap for Semiconductors (<http://public.itrs.net>) predicts that the number of processor cores in a typical SOC will increase fourfold per technology node to match the corresponding applications' processing demands. Typical multiprocessor SoC (MPSoC) applications, such as network processors, multimedia hubs, and baseband telecommunications circuits, have particularly tight time-to-market and performance constraints that demand a very efficient design cycle [2].

C. Feng, Z. Lu, A. Jantsch, J. Li and M. Zhang, has proposed its known to everyone knows, developments in semiconductor technology have made very complex large scale System-on-Chip (SoCs) design available. Usually, in a System-on-Chip, interconnection between different Intellectual Property (IP) cores is achieved by means of shared bus architectures. However, nowadays each new

SOC generation integrates more processing elements, more features and more new functionalities. With this increasing complexity, the system maybe needs extremely high capability in computation and communication. So, it is obvious that, use of shared bus architectures will affect performance of the overall system. In order to solve these problems, they have two different communication operations. Firstly, NIs can collect the data from all kinds of elements that are attached to them, packetize, add the header and tail information and send the processed packet into the attached router. Secondly, they receive the packets from the attached router. Network on Chip (NOC) is one solution for designing communication among components in the SOC circuits with several billion transistors that will reach the market in approximately 5-10 years from now. One reason for a new communication strategy is that it is too costly to use one global synchronous clock in a circuit, since it will take several clock pulses just for a signal to travel across the chip [3].

“M. Valinataj, S. Mohammadi, and S. Safari Currently, the manufacturing process of complex systems such as network-based Systems-on-Chip incurs a considerable amount of failures. This paper presents a class of very low cost routing algorithms to increase the yield and to tolerate permanent faulty links in Networks-on-Chip. These new algorithms are fault tolerant through dynamic reconfiguration when the regular topology is altered by faulty links. Also, the proposed algorithms are the reconfigurable extensions of deterministic routing algorithms and their deadlock freeness is obtained by prohibiting a few turns. To demonstrate the effectiveness of the proposed routing algorithms, the performance, power consumption, and area overheads are evaluated through appropriate simulations and syntheses [4].

M. Valinataj, S. Mohammadi, J. Plosila, P. Liljeberg, and H. Tenhunen, As everyone knows, developments in semiconductor technology have made very complex large scale System-on-Chip (SoCs) design available. Usually, in a System-on-Chip, interconnection between different Intellectual Property (IP) cores is achieved by means of shared bus architectures. However, nowadays each new SOC generation integrates more processing elements, more features and more new functionalities. With this increasing complexity, the system maybe needs extremely high capability in computation and communication. So, it is obvious that, use of shared bus architectures will affect performance of the overall system [5].

P. Rantala, J. Isoaho and H. Tenhunen, Here a novel agent-based reconfiguring concept for futures network-on-chip (NoC) systems is introduced. The necessary properties to increase architecture level fault tolerance are introduced. The system control is modeled as multi-level agent hierarchy that is able to increase application fault-tolerance and performance with autonomous reactions of agents. The

agent technology adds a system level intelligence level to the traditional NoC system design. The architecture and functions of this system are described on conceptual level. Communication and reconfiguring data flows are presented as study cases. Principles of reconfiguration of a NoC on faulty environment are demonstrated and simulated. Probability of reconfiguration success is measured with different latency requirements and amount of redundancy by Monte Carlo simulations. The effect of network topology in reconfiguration of a faulty mesh was also under research in the simulations [6].

W. Yin on-chip point-to-point distributed interconnection networks or Networks on a Chip (NOCs) have been proposed. Unlike the shared bus architectures, the key communication method in NOC architecture is to implement interconnections of different IP cores using on chip packet-switched networks. NOCs are composed of three components: Routers (switches), Links and Network Interfaces (NI). Routers are the switching elements that are responsible for forwarding data packets from one router to another one. Links are the connection parts between different routers, and they are usually bidirectional. Network Interfaces are the wrapper between the router and processing element (PE) [7].

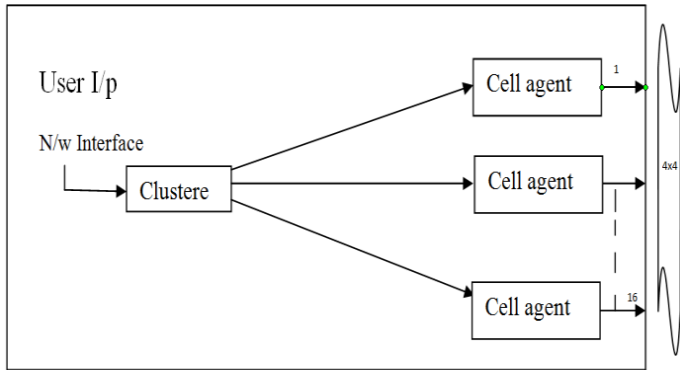
L. Guang, B. Yang, J. Plosila, K. Latif, and H. Tenhunen and p. Rantala, j. isoaho proposed a case study for hierarchical agent monitoring design approach, which provides a high level abstraction for designing monitoring functions on massively parallel and distributed systems. The case study features hierarchical power monitoring on NoC platforms, where each level of agents perform specific monitoring operations based on their granularity. The monitoring hierarchy and operations are specified by a formal language for consistent and non-ambiguous system design. Various benchmarks are mapped onto NoC's, running with hierarchical power monitoring agents. Quantitative evaluations are performed in terms of energy efficiency, communication latency, and silicon overhead [8][9].

A. Kohler, G. Schley, and M. Radetzki, Here The structural redundancy inherent to on-chip interconnection networks [networks on chip (NoC)] can be exploited by adaptive routing algorithms in order to provide connectivity even if network components are out of service due to faults, which will appear at an increasing rate with future chip technology nodes. This paper is based on a new, fine-grained functional fault model and a corresponding distributed fault diagnosis method that facilitate determining the fault status of individual NoC switches and their adjacent communication links. The network fault-tolerance assume switches to be either available or fully out of service, we present a novel adaptive routing algorithm that employs the remaining functionality of partly defective switches. [10].

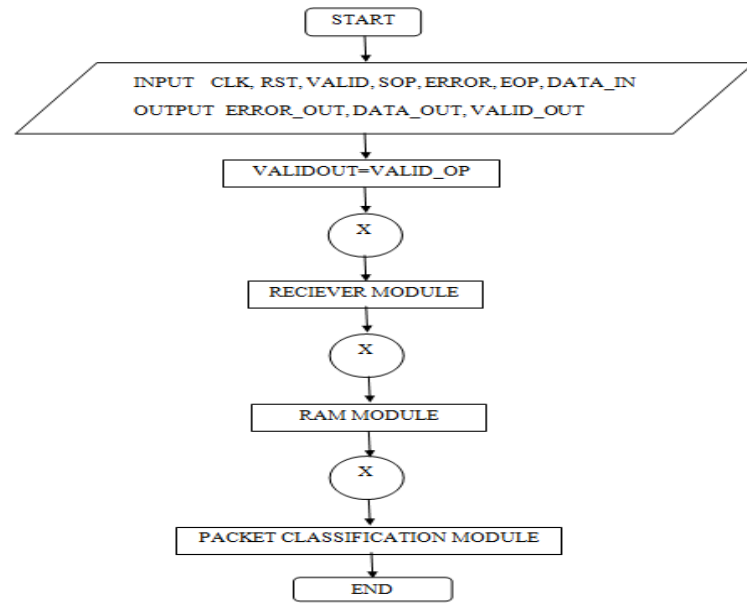
III. SYSTEM DESIGN

A clusture module receives the data from network interface units and using a receiver module and it is processed and classified according to its address specified. For this RAM and packet classification modules are used. In the cell agent all the information regarding the neighboring cell is made available and a test agent method makes sure of this operation and the control register is used to finalize the o/p.

Over all modules:

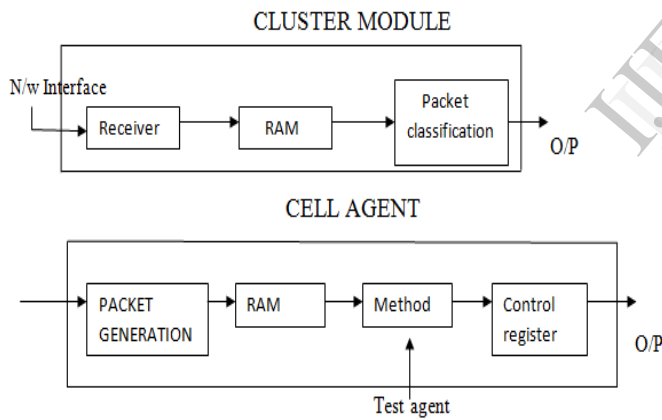


1. Flow chart of clusture module:

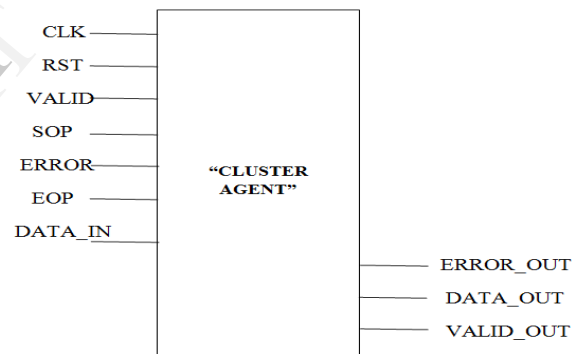


2. DESIGN OF OVERALL CLUSTURE AGENT

IV. IMPLEMENTATION DESIGN

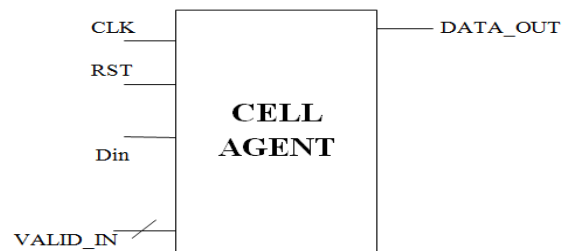


The clusture module consists of the Receiver, RAM, Packet classification units in it.

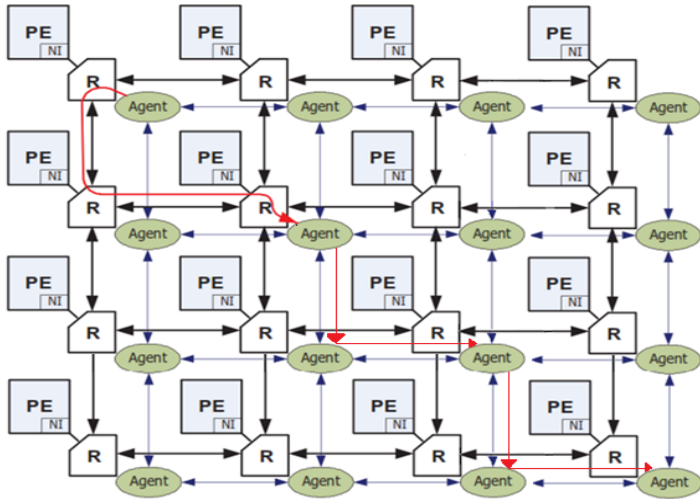


Clusture agent is the combination of receiver, RAM, and packet classification, which forms the clusture module. The cluster module is used as a processing element in a network architecture which is then used with the cell agents or router module to form the overall 4x4 architecture.

3. CELL AGENT COMPLETE MODULE



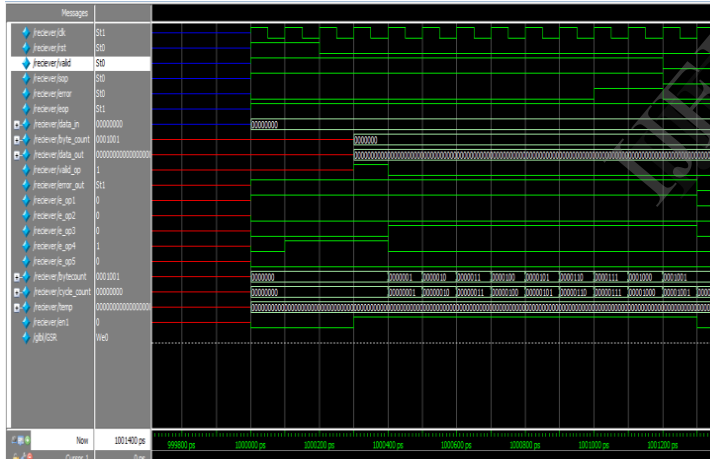
The complete 4x4 architecture can be seen below as shown where total of 16 modules can be developed.



This 4x4 architecture is used in network to route the packets from one point to the destination point. Here the reliability is maintained to the best possible extent and the faulty units are completely avoided by information regarding the neighboring unit status.

V. SIMULATION RESULTS

1. Clusture module.



The result can be seen for various values of Data_in for the respective selection of VALID, LDA, ERROR and RST respectively.

Condition 1: Only when RST is low further operation continuous..

Condition 2: Valid is an active LOW pin.

Condition 3: EOP is an active high pin

Condition 4: Byte count will keep the record of how many no of counts generated.

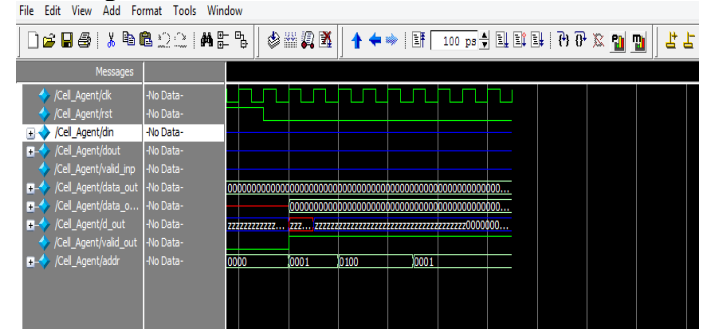
Condition 5: when the above conditions are met the data given at the input will be available at the output.

Practically the data from network is processed to the output i.e., it reaches the intended destination only.

The result is developed based on the using Xilinx for writing code and simulating and modelsim a free student

edition Output simulator.

2. Cell agent



The result can be seen for various values of Data_in for the respective selection of Rst, Addr, Data_in, Data_out, and Valid.

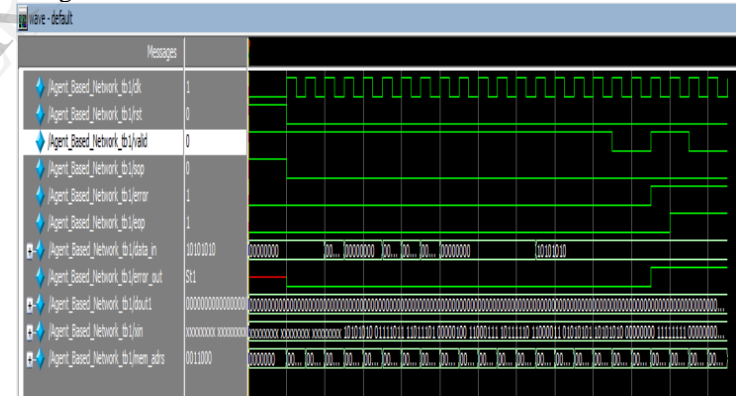
Condition 1: Only when RST is low further operation continuous..

Condition 2: Valid is an active LOW pin.

Condition 3: Addr is an activation pin which decides the routing

If Addr=4'd2 then valid will be made high else the valid is low and hence there by the normal routing operation takes place.

3. Agent based network



The final result is dependent on the Source data which is inputted and finally getting it to the destination irrespective of the status of the processing elements and make sure to take the shortest path.

VI. CONCLUSION

The scalable agent-based management architecture for fault-tolerant NoC-based CMPs is proposed. To exploit the proposed agent-based architecture for the fault-tolerant routing process, different types of required fault information are classified to be distributed in the network. Each level of agent hierarchy manages and distributes a specific type of fault information. This way, a higher performance can be achieved in the networks of different sizes. Here, we will investigate the agents in different levels of hierarchy with a

more efficient management process with higher architecture. In addition, the fault information will be classified and managed which will be useful for the routing process in the neighbor clusters.

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