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Novel Approach For Current Amplification With Low Power Dissipation

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Abstract—**This work provides a basic scheme for current amplification. A very weak input current can be made capable of controlling a strong output current. The proposed scheme can be effectively used in the design of current mode circuits for sensor applications. It is about a 5-transistor circuit performing current amplification. Current amplification is done 1000 times.**

INTRODUCTION

Many sensors are current based in which the sensing unit converts physical variables into current signals. Sensing units integrated in silicon VLSI circuits usually have a low sensitivity due to the limitation of fabrication process and/or that of sensing space. The sensing units can thus deliver very weak signal currents to the electronic circuit units integrated in the sensors. Therefore the circuit units should be designed to be able to respond to small current variations. Also to be integrated easily into the sensor space the structure of the circuit units needs to be simple and space efficient.

Current amplification is among the most commonly used in current detections in sensor circuits. Basic current operations, such as current triggering or comparison, can be implemented in a current amplifier if it has a very high gain over a well tuned narrow input current range. One of the simplest way to amplify a current is to use a MOS current mirror with unequal transistor aspect ratios, if the current gain does not have to be high. A high gain current amplification may be obtained in a circuit composed of transimpedance and transcoductance amplifier [1] and the quality and complexity of these amplifiers determine the performance of the current amplifier. If they are based on conventional OTAs, the current amplifier circuit will be much more complex than the current mirror based ones, and a higher gain is obtained at the expense of more space, more power dissipation, and perhaps lower speed. Another approach to implementing a high gain current amplification is to use back gate (bulk) of MOS transistors [2][3], and the high gain usually results from the exponential characteristics of the devices in the weak inversion mode. Thus the output current of an amplification unit needs to be low enough for the transistor to be driven in the weak inversion region.

Aiming at achieving high sensitivity low power and high speed of current of current amplification in a very simple circuit structure a current mirror like scheme for high current gain is proposed in this paper. Based on this scheme different current amplifiers could be designed.

DESCRIPTION

Principle

In fig 1 circuit diagram of classical current amplification circuit is shown in current amplification is done 600 times. A MOS current amplifier is used in this amplification circuit. This circuit has been simulated with the transistor model of a 0.18 µm technology.

As shown in fig 2 N1 MOS is connected with the PMOS. Gate of N1 MOS and gate of N2 MOS are connected. Here output current is measured at the drain of N2 MOS. Current source is connected between source of PMOS and V_{dd}. Here input is provided by the current source. Gate of N1 MOS is connected with the source of PMOS. Gate of PMOS is connected with the source of N1 MOS and these two are connected with the ground. Source of N2 MOS is also connected with the ground. Here W/L ratio is not same for all NMOS [6].

In figure 3 four NMOS are interconnected. In this circuit gate of N1 MOS and gate of N2 MOS are connected. Gate and source of N1 MOS are connected with each other. I_2 is the current at the drain of N2 MOS. Drain of N3 MOS is connected with the source of N2 MOS. Gate of N3 MOS and gate of N4 MOS are connected with each other. Source of N4 MOS, source of N3 MOS and source of N1 MOS is connected to ground. I_3 is the current at the drain of N4 MOS [4].

Our proposed circuit is shown in the fig 4. The current amplification circuit comprises a first NMOS transistor having gate, drain, and source. Drain of first NMOS is connected to the drain of PMOS. Source of PMOS is connected to current source and current source is connected to V_{dd}. And gate of first NMOS is connected to gate of second NMOS. Gate and drain of first NMOS are not connected .

Drain of second NMOS is connected to resistance and resistance is connected to V_{dd}. Source of second NMOS is

connected to drain of third NMOS. Gate of third NMOS is connected to gate of fourth NMOS. Drain of fourth NMOS is connected to resistor and this resistor is connected to V_{dd}.

Gate of PMOS, source of first NMOS, source of third NMOS, source of fourth NMOS are all connected to ground. All V_{dd} have the same value. If the value of the input current is changed then output of the circuit will also change. If the parameter of the device of the circuit changes then output of the circuit will also change. At the given value of input current circuit will behave as current amplification circuit.

I_1 is the current which is measure at the drain of NMOS 1. I_2 is the current at the drain of NMOS 2. I_3 is the current at the drain of NMOS 3. I_4 is the current at the drain of NMOS 4.

In the proposed circuit W/L ratio of all the NMOS is same. Proposed circuit work as current amplification circuit in the very low value of current and dissipates very low power.

In the current amplification circuit the cascoded PMOS-NMOS structure is used to make the non linear mode of the NMOS depend on the input current. In the waveform shown in the figure current i_1 , i_2 , i_3 , i_4 are shown. This graph shown the current on the cadence platform.

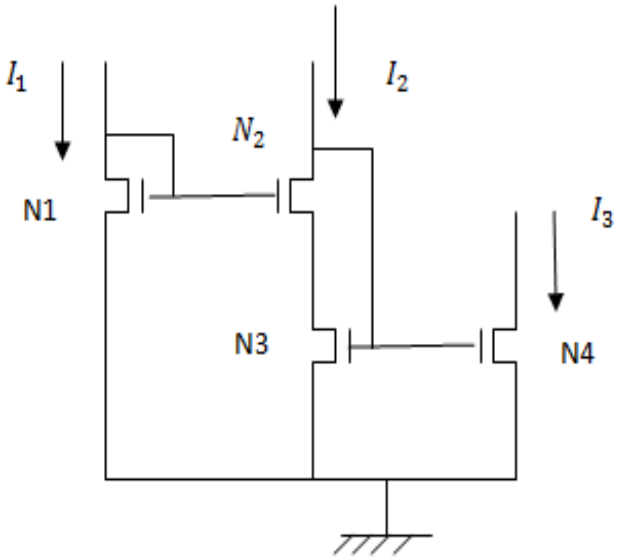

Fig.3. Current amplification circuit in which drain and gate are connected. [4]

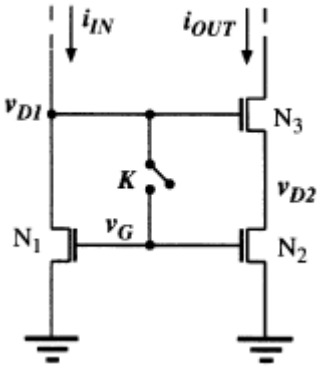

Fig 1 shows current amplifier in which current gain is 600 times [5]

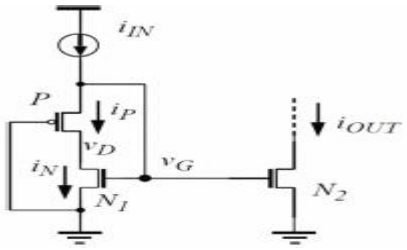

Fig.2. current amplification circuit [6]

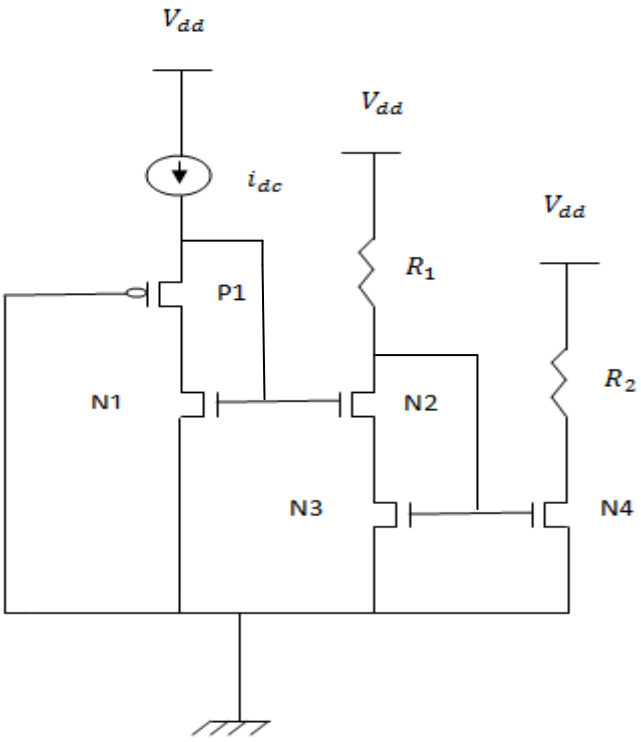

Fig.4. Proposed current amplification circuit.

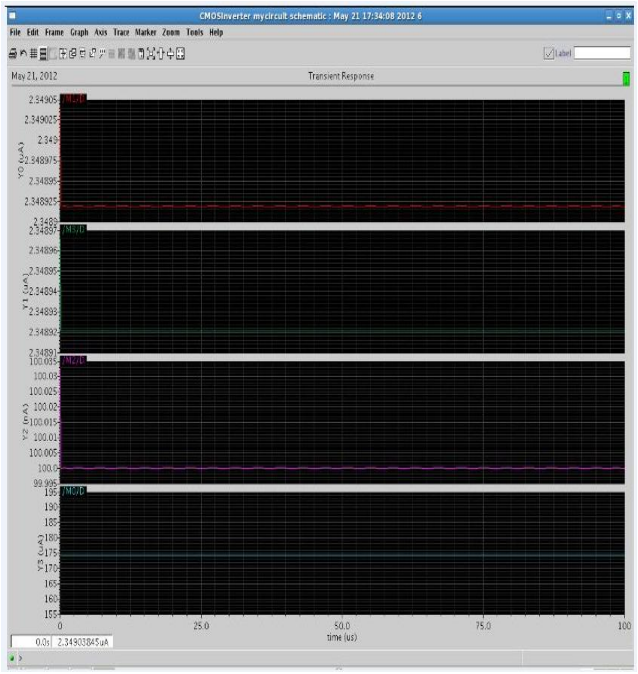

Fig 5:output waveform in cadence

Table

Parameter	Value
V_{dd}	1.8 V
R_1	100 Ω
R_2	100 Ω
i_1	100 nA
i_2	2.3 µA
i_3	2.34 µA
i_4	174.37 µA
Stop time	100 µs
Total power	318.137 µW

RESULT

The current source i_{dc} have value 100 nA. Supply voltage V_{dd} is 1.8 V. Value of R_1 and R_2 resistance is 100 Ω . The circuit has been simulated with 0.18 µm technology. Here i_2 is equal to 2.3 µA. Value of i_3 current is 2.34 µA. Value of i_4 current is 174.37 µA. Current is amplified 1000 times. Input current is 100 nA and output current is 174.37 µA. Width of PMOS is 240 nm and length is 180 nm. Width of all NMOS is 240 nm and length is 180 nm. The circuit is expected to behave as current amplification circuit. The circuit is implemented on the cadence. Here stop time is taken as 100 µs. Analysis is done in moderate mode in cadence. And total power dissipated by the circuit is 318.137 µW. Output waveform shown in the fig 5. Table shows the value of different parameter.

CONCLUSION

In this paper, a basic scheme of current amplifications has been proposed. With this scheme, the nonlinearity of devices can be easily explored to realize useful current operations. Based on this scheme, a series of current amplifiers can be designed. These current amplifier circuits feature simple structure, and capability of operating with very weak currents, which makes the circuits suitable for sensor applications. The amplification gain can be made very high and/or adaptive to the input current. The proposed scheme can also be used to design other current operation units such as current triggers or comparators.

REFERENCES

[1] E. Bruun. “Contant bandwidth current mode operational amplifiers,” Electronics Letters, vol. 27 , No. 18, Aug. 1991 , pp 1673-1674.

[2] R. Fried and C.C. Enz, “CMOS parametric current amplifier,” Electronics Letters, vol. 32 no. 14, July 4, 1996, pp 1249-1250.

[3] T. Serrano-Gotarredona and B. Linares-Barranco, “7-decade tuning CMOS OTA-C sinusoidal VCO,” Electronics Letters, vol. 34, no. 17, July 1998, pp 1621-1622.

[4] F. Kronmueller and P. Zehnich, “Operational transconductance amplifier with a non-linear current mirror for improved slew rate,” US patent 6414522 B1 ,July 2002.

[5] C. Wang, “A simple scheme of current amplification for sensor applications,”in Proc. IEEE International Conference on Eletronic Devices and Solid State Circuits, Dec. 2005, Hong Kong, pp. 647-650.

[6] C. Wang, “Non linear current mirrors for analog and mixed signal processing,” Circuits and Systems (MWSCAS), 2011 IEEE 54th International Midwest Symposium September 2011, Seoul pp 1-4.