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Novel Approach for Designing of HRPX and HMPE based Reverse Converter for Enhanced Speed and Area

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***Abstract*— The Reverse converter is the key component in the Residue number based arithmetic systems. The Residue number system provides high speed applications. Hence it can be applied to vast number of fields. The electronic systems will operate with the digital number systems. To facilitate Residue arithmetic we need conversion mechanism in between the two systems. To achieve this we employ forward and reverse converters. This paper presents a new kind of design parallel prefix called HRPX and HMPE which facilities better trade off with compared to the carry propagate adders in the earlier systems. I have designed this converter using Verilog HDL and This RTL description is synthesized in Xilinx ISE14.7**

Keywords—Forward converter, Modulo airthematic,Hybrid parallel prefix network, BEClogic

I.INTRODUCTION

The residue number system will impact all digital systems with its high speed feature. The residue number arithmetic operations are performed in parallel and that are almost carry free. The residue number systems usually employed in applications like Digital signal processing and cryptography. To facilitate this high speed feature to all digital system we need a conversion mechanism in between the digital and residues. The converters plays major role during this issue. There are two conversions as binary to residue vice versa. The forward will convert binary number system to the residue number later the required operation will be performed on the residues then after getting required result. The result again has to convert back to the digital number system. This is accomplished with the reverse converter. To employ the usage of Residue number system in the hardware we need to include these converters. The design of forward converter is simple and l fast. The design of reverse converter is complex and needs longer delay. To avoid this longer delay and system complexity we aimed at designing of the efficient reverse converters. In the process we followed two approaches introducing new formulas which make design simple and introducing new formulae's such that existed formulas will be simplified to make simple design. This approach is allowing us to use conventional adders such as ripple carry adder, carry look ahead adder, and carry save adder and parallel prefix adders. Among all adders presented having least performance in terms of area, delay and complexity. The Ripple carry adders having simple design but when the number of bits is increasing which in turn produce longer propagation delay. The parallel prefix adders having high speed but they are area and power inefficient. In this project we have designed the Hybrid parallel prefix network which having good trade-off in between the area and delay. They are described in detail in subsequent chapters.

II.LITERATURE REVIEW

The Residue number system obviously will have forward and reverse conversion policies, residue arithmetic units are the key components for this system. The reverse converter design is non modular process and it is more complex. To make design feasible we have to concentrate on the two prime concerns are moduli set selection and way of converting algorithm, Selecting two elements will yields efficient design. In addition to them the selection hardware modules are also impacts the converter design such as if we select an ripple carry adder which is having huge delay, if we choose parallel prefix adders which having huge area and power consumption which degrades the performance of the converter. To perform conversion earlier we introduced few converters are Converter with carry save adder lags in speed. The carry propagate adder based converter is presented here which is less complex. The number of residues is increasing the carry has to propagate from one stage to another stage to compute the sum which in turn induces delay. To improve the speed high speed parallel prefix adder's converter are introduced. These will produce the carry at the proceeding stage such that it will directly compute the sum from the carry results which are obtained in previous stage. These adders will require more power and more area with compared to previous converters. So we need a converter such that optimizes needs minimum area and good amount of speed. We have introduced new parallel prefix converters which are efficient in area with compared to the prefix adders and speed efficient with compared to the Carry propagate adders based converter. We are designing a converter which is optimized in area and speed with compared to the existing converters.

III. NOVEL PARALLEL PREFIX COMPONENTS

The Reverse converters which are designed with RCA already have discussed that having the effect when there is the growth in number of residues which complicates the speed. To improve the performance introduced parallel prefix adders which in turns increase the speed but when number of operands is increasing, there is a logarithmic growth in the number of prefix levels computation which in turn increases the area and power. The reverse converter normally several adders and in the one is prominent which required at the last stage in the converter used for binary representation. The adders which are usually have large number of bits, this adders parameters and performance will shows major effect on the whole converter performance. This should be carefully designed. We can keep one of the operand applying for this adder is as constant such that decrease the computation effect of this class of converter. We may deduce one lemma

Lemma: this proposes that one of the operand that is applying for the CPA4in the converter is always constant and that equals to one's which are of 2n+1 bits

We can prove this by considering Ripple carry adder in converter actually which performs subtraction of 4n+1 bits operands those are named P, T from the block diagram of the converters. This will also produce result S.

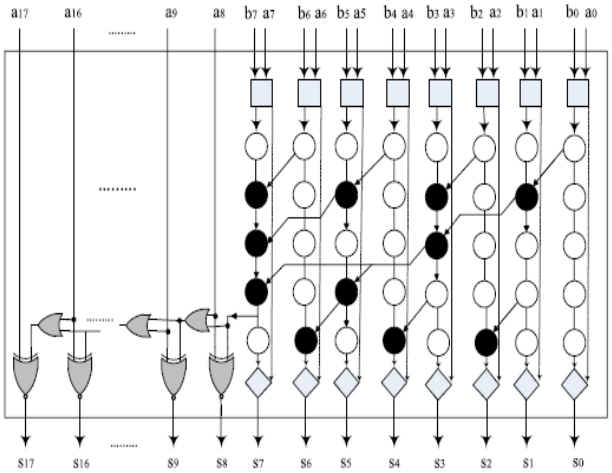

Fig 3.1 HRPX Module

$S=P-T$

This can be performed by the making one's compliment and adding one such that we can apply it to the adder as below

$S=P+\overline{T}+1$

The P,T are the operands with 4n+1 and 2n+1 bits binary vectors. Hence we can represent as

$$P=\underbrace{P4n, P4n-1\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots P0}_{4n+1}$$

$$T=\underbrace{11\ldots\ldots 1\ T2n, \overline{T2n-1}\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots T0}$$

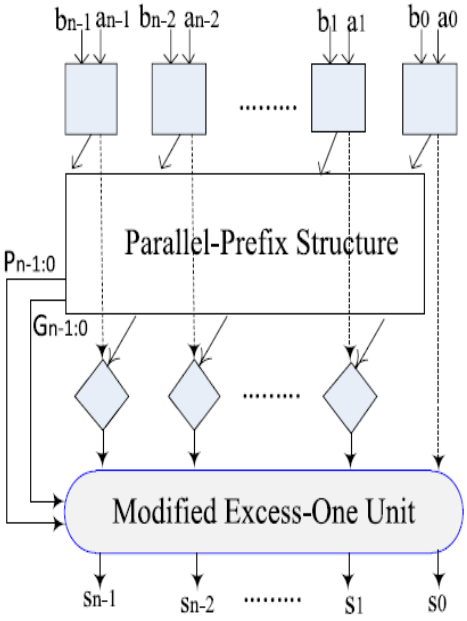

Fig 3.2 HMPE Module

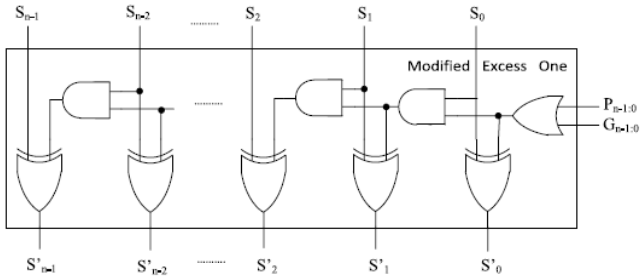

Fig 3.3 Modified Excess one unit

There are 2n+1 number of ones in the T which ha re almost equal to the half of the number in the 4n+1 bits. The above lemma suggested that it is having two operations one is addition of P and T then the result has to beaded with sequence of 2n 1's. The first part of the 2n+1bit addition will be performed by the any parallel prefix structure and other part of the addition is performed by the RCA network with simple modification to avoid carry propagation. The modification is XNOR /or network of full adder because of the constant operand. The HRPX architecture used to perform 4n+1 bit addition as above. It consists of 2n+1 bit addition by the preferred prefix network followed by the XOR/OR network. Here we can ignore carry propagation network such that speed achievable.

The Reverse converter also contain second modulo addition which is normally accomplished with the Carry propagate adder with end around the carry of 2n-1 bit addition. This adder will have dual representation for zeros. The actual converter will only have one zero representation for zero. To avoid this we have to use an extra logic which

in turns increases the delay of the network. The binary excess one network will be used to achieve single representation. We can use prefix network to increase the speed but increases the area and power due to the recursive approach for generating generate and propagate signals and also require one more prefix network to generate carry signals and one adder network to compute sum. Because of the second prefix network area and power are increasing. In proposed model we will avoid summing unit we use modified excess one unit in conjunction with the prefix network resulted structure is called Hybrid modular parallel prefix excess one adder (HMPE). The HMPE network will have two modules as prefix network and excess one adder. The prefix network which will have two inputs and compute addition that will be conditionally incremented by using modified excess one network based on the control signals.

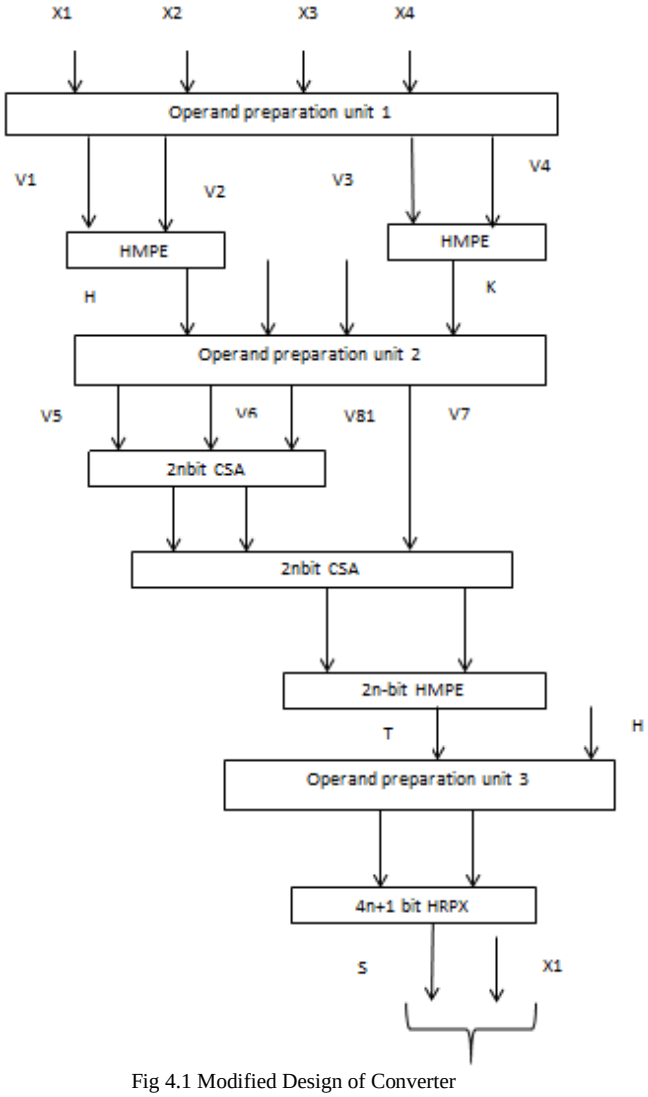

Fig 4.1 Modified Design of Converter

IV.REVERSE CONVERTER DESIGN

Before describing about the proposed converter we will have a glance on the existing converters. There are several converters for different moduli sets which can be classified into three types. Set of tree carry save adders together forms first category. Set of a carry save trees and carry propagate adders will together with a last stage adder-sub tractor will form second category, the third type of converters are of moduli set which are more than bits 2n and 2n+1 bits. In this proposed method we have designed the second method of converter by HRPX and HMPE modules instead of the Carry propagate adder End around carry in the algorithm.

In this project we have aimed at reducing speed and area such that we are selecting the modules such that adjusting the tradeoff between the area and speed. The carry propagate adder with end around carry which performs 2n+1 addition are replaced with the HMPE modules. The adder and sub tractor which performs 4n+1 bit subtraction also done by the large bit CPA is also replace HRPX module. Now this design makes efficient improvement in area and speed.

V.SIMULATION RESULTS

In this paper we are presenting the new approach for designing of reverse converter using Hybrid parallel prefix modular excess one adder and Hybrid modular parallel prefix adder for subtraction at the final stage. In this project we have considered the value of n=4 for that we designed the complete converter for existing converter using carry propagate adder with End around carry and Carry save adder model ,The proposed converter with Novel adders are designed using Verilog Hardware description language. Then that RTL description is synthesized in Xilinx ISE 14.7. The Description is simulated in Modelsim 6.3.The synthesis reports given for the Zynq family FPGA reports as area is represented in terms of LUTS and Speed is specified by the delay of the combinational path is presented. Then it is also simulated by for certain values of residue inputs are x1, x2, x3, x4 and the final value we will get in terms of the Binary value is represented as X. The synthesis reports are proving that proposed converter having better trade of between area and speed of the converter.

For testing the converter we gave inputs as
X1= 4'b1000= $(8)_{10}$
X2= 8'b000001001= $(9)_{10}$
X3=4'b1010= $(10)^{10}$
X4=4'b1010 and Result is X= $(589195)_{10}$

Table5.1 Comparison of area and Delay

Parameter	Existing converter	Proposed Converter
Delay(ns)	11.166	10.976
Number of LUT slices	163	124

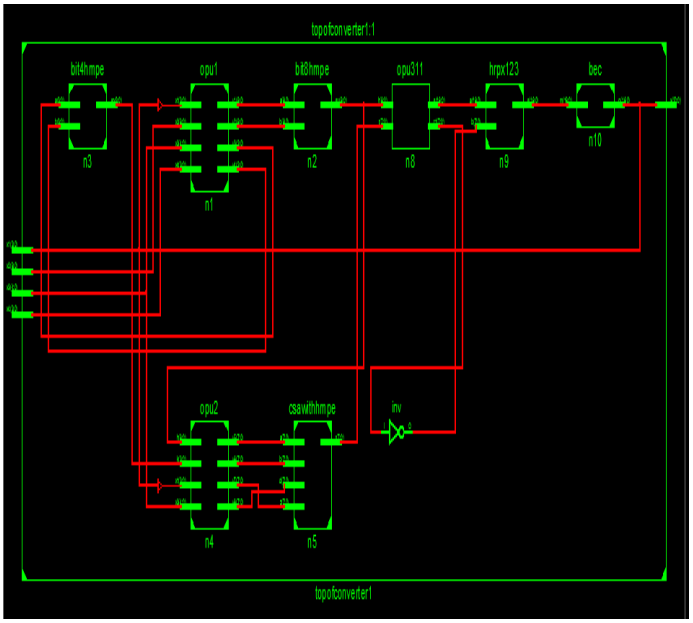

Fig 5.1 RTL schematic of the Modified converter

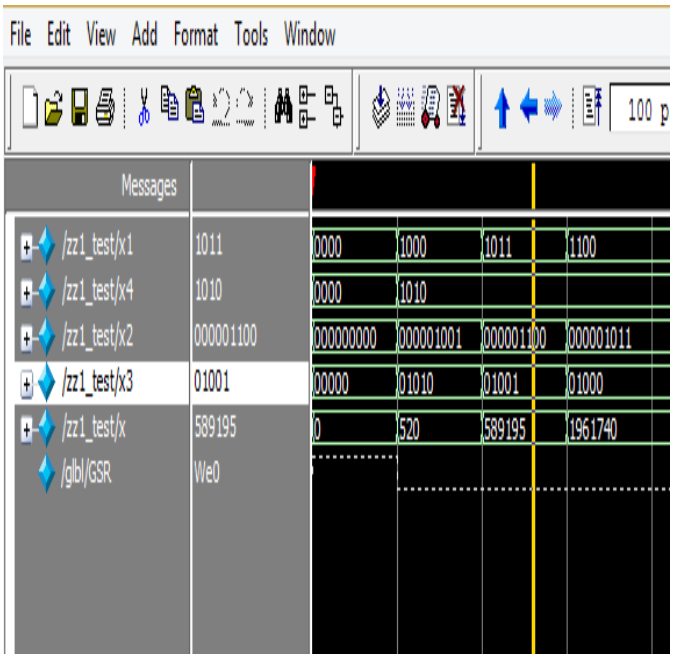

Fig 5.2 Simulation waveforms for converter

VI.CONCLUSION

The Residue number system which will increase the speed of arithmetic units, for that we have to use forward and reverse converters. The proposed converter is aimed to make trade of between the area and speed of the comparator for enhanced performance. To design this converter we introduce the new hybrid adder components which will enhance the performance. The proposed converter is RTL description is written Verilog HDL. The description is synthesized and simulated in Xilinx ISE14.7 and simulated in Model sim 6.3. The synthesis reports obtained are proving that proposed converter has better trade between the areas and speed with compared to the existing converter

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