Optimization for Transmission Gate Master Slave Scan Flip Flop

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***Abstract*— Delay faults are frequently encountered in nanometer technologies. Therefore, it is critical to detect these faults during manufacturing process. Testing for a delay fault requires the application of a pair of test vectors in an at-speed manner. To maximize the delay fault detection capability, it is desired that the vectors in this pair are independent. Independent vector pairs cannot always be applied to a circuit implemented with standard scan design approaches. The work attempted to design various architectures of such scan flops along with its control circuits as standard cells. Three architectures of scan flops with various scan options will be chosen. Such as Transmission Gate Master Slave, C^{2}MOS, TSPCR based Scan Flops. Thus the Scan flip-flop standard cell based on the transmission gate with master-slave structure is optimized.**

The design of scan flops will be carried out in 180nm technology satisfying delay constraints like hold time, setup time and maximum operating frequency and at the same time it will be ensured that the design meets the power constraints. Simulations demonstrate is used in UMC 180nm tech library in cadence tools and that our design is more robust to process.

***Index Terms* —Transmission Gate Master Slave (TGMS), Clocked CMOS (C^{2}MOS), True Single Phase Clock Register (TSPCR) based Scan Flops.**

1.1 INTRODUCTION

Standard Cell comes from Semi-custom IC Technology. The Designers are provided with library of predesigned cells. These chosen cells has to be placed and connect between them, result is obtained in masks. The masks are sent to the fabrication plant to produce ICs.

Scan flip flop is described as the combination of Multiplexer and flip flop which is used for testing logic elements and functions with various scan test vectors. The flip-flop designs with timing constraints are necessary to further action.

A flip-flop is controlled by one or two control signal or clock signal Clock devices are especially designed for synchronous systems and therefore ignore is inputs except at the transition of the clock signal. This causes the flip-flop to either change Or retain their output signals at the transition. Some flip-flops change output on the raising edge of the clock others on the falling edge.

A universal flip-flop with the best performance, lowest power consumption, and highest robustness against Noise would be an ideal component to be included in cell libraries. However, it will be shown in this Paper [6], that Increasing the performance of flip-flops generally involves significant power and robustness trade-offs. Therefore, a set of different latches and flip-flops with different performances are essential to limit the use of more power consuming and noise-sensitive elements only for smaller portion of the chips with performance-critical units. This eliminates global and unnecessary increase in power consumption as well as robustness degradations, which would result in overall decrease in noise margin requiring extra careful and time consuming design.

The goal of this work is to find a small set (ideally the smallest set) of scan flip-flop topologies to be included in a library covering a wide range of Timing and power-performance targets. Our strategy has been to first explore the capabilities of conventional and simpler transmission-gate (TG) based scan flip-flop topologies, before including other types of scan flip-flops. Among a large number of scan flip-flops that have been proposed in the past, we have selected some of the widely used and/or referred topologies.

Three scan flip-flops we have incorporated in our initial benchmark including static and dynamic edge-triggered mater-slave. In contrast to, a wide power-performance space for each of the three scan flip-flops has been explored [5]. By sizing, useful operating ranges of the flip-flops have been identified. The design-space exploration not only enables a true comparison, but also it reveals potentially large overlaps in operating range of the flip-flops. This in turn provides an opportunity to reduce the number of different circuit topologies in a scan flip-flop library.The idea for this Paper is to explore the timing constraints and propagation delay for different structure of scan flip-flops. This will give us a good understanding of different structures and make the decisions easier for the designers.

Finally TGMS Scan flop have been optimized with respect to Timing constraints among these three

flops then it has to be incorporated to the standard cell library in the proper manner and design procedure have been given.

1.2 TIMING AND DELAY DEFINITIONS FOR FLIP-FLOPS

The performance of a flip-flop is qualified by three important timings and delays: propagation delay (Clock-to-Output), setup time and hold time. They reflect in the system level performance of the flip-flops. Setup time & hold time define the relationship between the clock and input data

1.2.1. Propagation delay

Propagation delay (Clock-to-Output) is the time delay after arrival of clock's active edge that output is considered stable. Clock-to-Output equals the time it takes for the output to change after the occurrence of the clock edge.

Usually propagation delay differs for low-high transitions and high-low transitions.

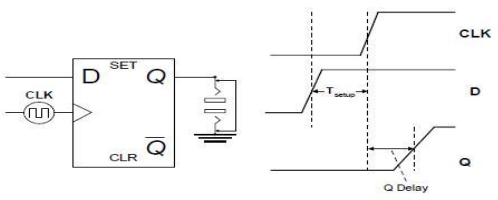
1.2.2. Setup time

The minimum setup time is the smallest time interval for which data must remain stable on a data output before it is latched in by an active transition on an appropriate control input. For a D flip-flop, this is the time period for which the data input D must be maintained before the arrival of the active level of the clock input CLK. Setup time is measured from the clock transition relative to the input data transition. Figure 1.1 shows the input/output waveforms of a D flip-flop to describe this concept.

The minimum setup time measurement is carried out by the following steps. First, let the data signal transit to a desired level at some point. After a long enough period of time is past, the clock transition is asserted. This time period is called *reference setup*. The propagation delay from clock to output transition is measured as a *reference delay*. Then, the data signal is changed to approach the clock active edge which should be fixed after the reference delay is obtained [7].The time difference between the changing data signal and the active clock edge is called T_{setup}. The data value must remain stable around the time clock signal changes value to ensure that the flip-flop retains the proper value.

Fig1.1.A Positive –Edge Triggered D Flip-flop and its input/output

1.2.3. Hold time



Flip-flop design requires the state of the input to be held for some time after the clock edge. The time after the clock edge that the input has to remain stable is called the hold time. Basically hold time can be negative meaning that data can be changed even before clock edge and still previous value will be stored. For a positive-edge D flip-flop, the minimum hold time is the period of time after the active edge of clock input during which the D input must be held constant. Figure 1.2. Shows the hold time measurement for a positive-edge triggered D flip-flop. The measurement methodology is the same as that for minimum setup time measurement.

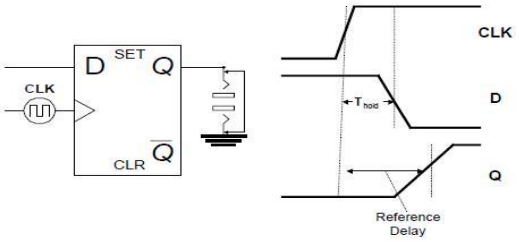


Fig1. 2. The Hold Time measurement for DFF

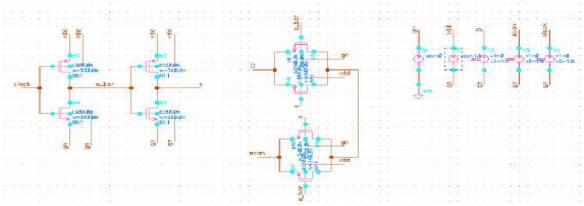
In these definitions, propagation delay, setup time and hold time are considered as independent variables. However what happens in reality shows that these parameters are not independent from each other. For instance, propagation delay is strongly related to the data arrival time. When data arrival time is very close to clock edge, the Clock-to-Output delay increases drastically. In this case flip-flop is very close to function incorrectly or to enter an unstable operation point called metastability.

SCAN FLIP-FLOP'S TOPOLOGIES

Many Scan flip-flop topologies have been proposed in the past. For our comparative study, some of widely used and/or referred topologies in our initial benchmark have been selected. Two static master-slave flip-flops and one Dynamic flip-flop are included in our test bench. Figure 2.1 shows the static positive edge triggered transmission-gate based multiplexer.

2. TRANSMISSION GATE MASTER SLAVE D FLIP FLOP

Transmission gate b ased multiplexer schematiic



Simulation waveform

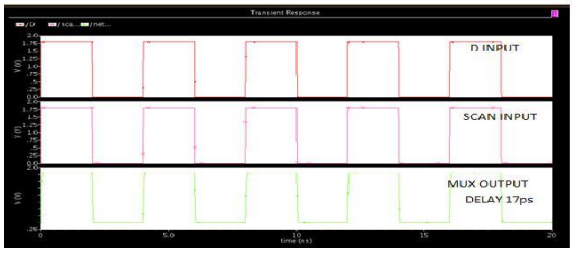


Fig.2.2 Simulation result of 2:1 Multiplexer using TG

Thus the Simulation result shows that 2:1 multiplexer takes 17ps to provide the output. The output must be one of the given two inputs. This Switching activity is very fast comparing to other architecture multiplexers. It produces the output very fast with few Pico seconds. Clock speed is 4ns (i.e.) 250 $M_{HZ.}$

Transmission Gate based D-flip flop schematic

A Flip-Flop can be designed as a latch pair, where one is transparent-high, and the transparent-low. Master-Slave Flip-Flops based on transmission gates are the best when energy is the main concern. The edge-triggered flip-flop is built from two D-type level-triggered latches. Both latches are enabled with opposite polarity of the clock signal: The second (or slave) latch is controlled by the clock signal, while the first (or master) latch is enabled by the positive clock.

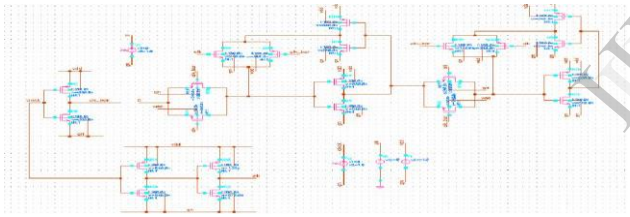
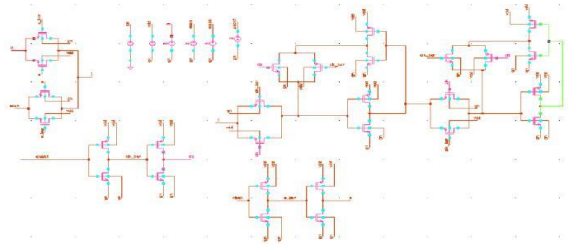


Figure 2.3 Transmission gate flip-flop (TGMS)

In this TGFF, we use the transmission gates for both master and slave latches as shown in fig.2.3. It is one of the fastest classical structures. Its main advantage is the short direct path and the low power feedback. The large load on the clock will greatly affect the total power consumption of the flip-flop. This flip-flop is the transmission gate flip-flop; it has a fully static master-slave structure, which is constructed by cascading two identical pass gate latches and provides a short clock to output latency. It has a poor data to output latency because of the positive setup time. Moreover, it is sensitive to clock signal slopes and data feed through. This adds another concern when using it [1].



Simulation waveform

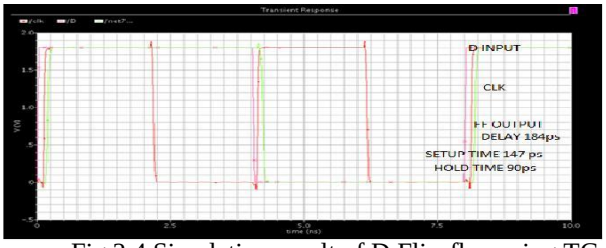


Fig.2.4 Simulation result of D Flip-flop using TG

Thus the Simulation result shows that DFF takes 184ps clock to Q delay to provide the output, from this T*min* value should be greater than total setup and clock to Q delay time .D flip-flop change output on the raising edge of the clock.

Clocked capacitances should be minimized in order to reduce the clock load. The method of logical effort [4] is used in transistor size optimization. The path in the TGFF responsible for the CLK-Q delay is depicted. The off-path capacitance, C_{off}-path is equal to the gate capacitance of two minimum width feedback transistors. Keeper transistors in the feedback of both master and slave latches are of minimal width. Minimum sizing of the master stage minimizes the energy consumption with little impact on the setup time [3].

Transmission gate master slave based scan flop simulation

Scan Flip-flop is realized by the combination of 2:1 multiplexer and DFF using TG based architecture. It is shown in below.

Figure 2.5 -Transmission gate scan flip-flop

Simulation waveform

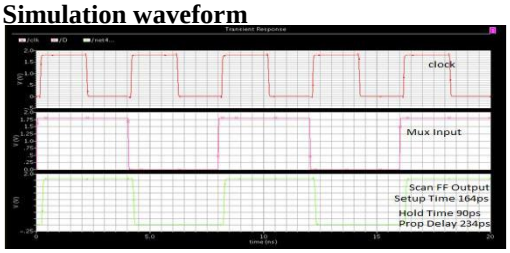


Fig.2.6 Simulation result of Scan d Flip-flop using TG

Thus the Simulation result shows that Scan DFF takes 234ps CLK to Q delay to provide the output, from this T_{min} value should be greater than total setup and clock to Q delay time. D flip-flop change output on raising edge of the clock. Scan input used for to detect the faults during manufacturing process.

3. C²MOS BASED SCAN FLIP FLOP SCHEMATIC

An ingenious positive edge-triggered register that is based on a master-slave concept insensitive to clock overlap as shown in Fig3.1 has been proposed. This circuit is called the C²MOS (Clocked CMOS) scan flip-flop which operates in two phases: when clk=0, the first driver is turned on, and the master stage acts as an inverter sampling the inverted version of D on the internal node X. The master stage is in the evaluation mode. When clk=1, the master stage section is in hold mode, while the second section evaluates. The previous value stored is propagated to the output node through the slave stage, which acts as an inverter [3].

Scan Flip-flop is realized by the combination of 2:1 multiplexer and DFF using C²MOS based architecture. It is shown in below

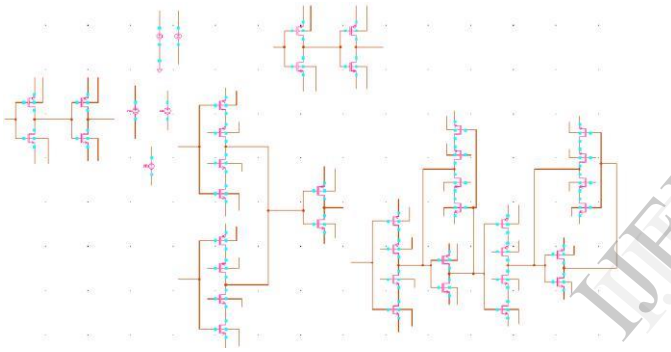


Fig 3.1.C²MOS scan flip-flop

Simulation waveform

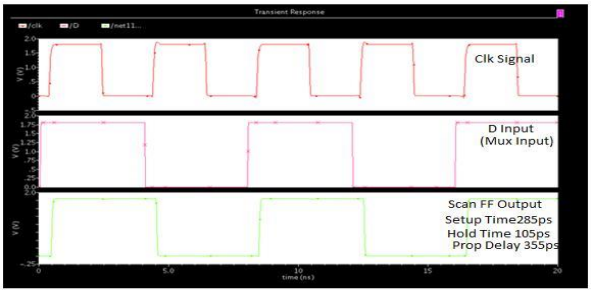


Fig 3.2. Simulation result of Scan D Flip-flop using C²MOS

4. TSPC LOGIC BASED SCAN FLIP FLOP

Scan Flip-flop is realized by the combination of 2:1 mux and DFF using TSPC based architecture. It is shown in below

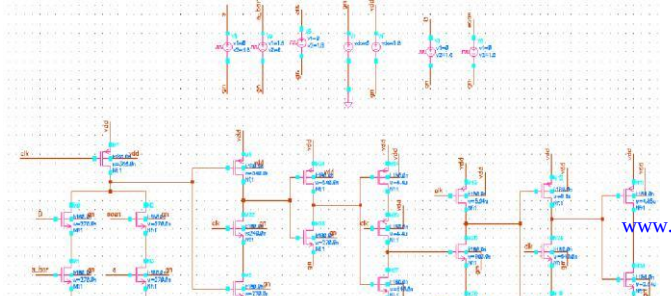


Figure 4.1 -True single phase clock scan flip-flop (TSPC)

Transistor sizing is critical for achieving correct functionality in the TSPC register. With improper sizing, glitches may occur at the output due to a *race condition* when the clock transitions from low to high. Consider the case where *D* is low and *Q*=1 (*Q*=0). This glitch may be the cause of fatal errors, as it may create unwanted events [2].

Simulation waveform

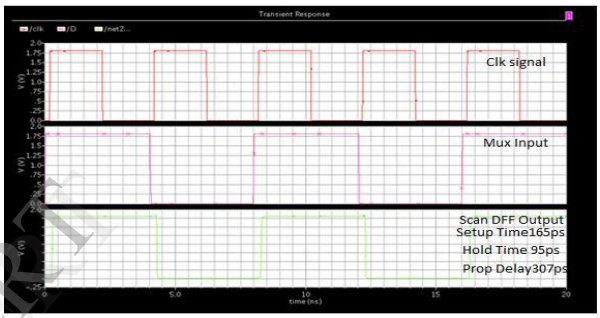


Fig.4.2 Simulation result of Scan D Flip-flop using TSPC

Total propagation delay

The delay experienced by a signal when passing through a gate. It is measured between the 50% transition points of the input/output waveforms

Clock Time Period *T=4ns*

Maximum Operating Frequency *f=1/T=250MHz*

Total Propagation Delay=*0.69* R_{eq} C_{Load}

Where $t_p = \frac{t_{pHL} + t_{pLH}}{2} = 0.69 C_L \left(\frac{R_{eqn} + R_{eqp}}{2} \right)$

$C_{LOAD}=C_{DN}+C_{DP}+C_{GN}+C_{GP}$

$Req=(3/4)V_{DD}/I_{DS}$

The dynamic power consumption is due to dynamic switching events. During the first half cycle, the input voltage, V_{IN} is 0V. The PMOS is turn on and the current
flows through MP and charges C_{OUT} to a voltage $V_{OUT} = V_{DD}$. During the second half, when the input is high, the NMOS is
on and causes the C_{OUT} to discharge. The dynamic power arises from the observation that a complete cycle effectively creates a path for current to flow from the power supply to ground. The charging event leaves C_{OUT} with a voltage $V_{OUT} = V_{DD}$. When the capacitor is discharged through NMOS, the same amount of charge is lost. The dynamic power is given by $P_{DYN} = C_{out}V_{DD}^2f$. Therefore

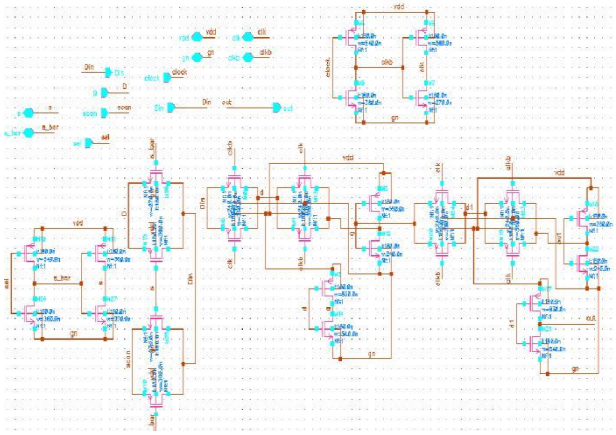
Power Consumption $P= f\, C_{load}\, v_{dd}^2$

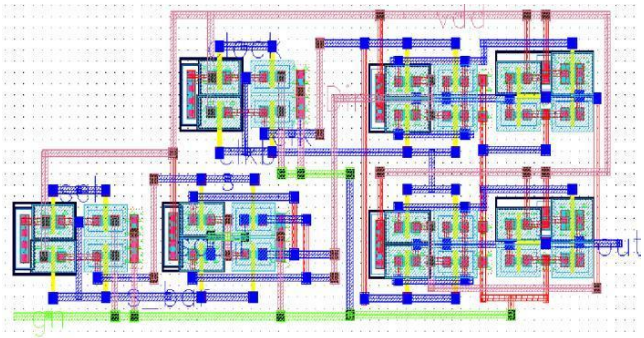
5. COMPARISON OF SCAN FLOP ARCHITECTURES

ARCHITECTURE	*Setup time*	*Hold time*	*Clk - Q delay*	*Power Consume*
TGMS SCAN FLOP	*164ps*	*90ps*	*234ps*	*22 µw*
C²MOS SCAN FLOP	*285ps*	*105ps*	*355ps*	*29 µw*
TSPCR SCAN FLOP	*165ps*	*95ps*	*307ps*	*135µw*

From this tabulation, the paper conclude that among these three scan Flip-flops, Transmission Gate based Flip-flop design have been optimized and consume less Power, causes less propagation Delay as well as setup hold time. Then TG Multiplexer activity is goes rapidly than others, further this scan Flip-flop carried out to Design synthesis. Scan D Flip-flop's Schematic layout and layout have been designed in rapid manner and further have been verified DRC as well as LVS Stage.

6. OPTIMIZED TGMS SCAN D FLIP-FLOP LAYOUT





7. CONCLUSION:

Thus this Paper explores the Setup time, Hold time, Propagation Delay of Three widely referred Scan flip-flops in a 0.18µm CMOS technology. The simulation result has been to find the smallest set of scan flip-flop topologies to be included in a ―high performance‖ flip-flop cell library covering a wide range of Delay constraints targets. Based on the comparison results, transmission gate-based Scan flip-flops show the best power-performance trade-offs with a total delay (clock-to-output + setup time) down to 234ps.

Significant improvements have been found on delay and power, thus showing that this approach realizes high performance designs.

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