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Optimization of Logic Paths for CMOS-Based Dual Mode Logic Gates

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Abstract:- **The project proposes to develop a simple method for minimizing delays and achieving an optimized number of stages in logic paths containing CMOS-based DML gates. This project offers three different approaches (1) Complete Approximated (CA) Method, (2) Complete Un-Approximated (CS) Method and (3) partially/Semi Approximated (SA) Method, which tradeoff between complexity, computation and accuracy.The proposed optimization is shown for the dynamic mode of operation. Theoretical mathematical analysis is presented and efficiency of the proposed methodology is shown in a standard 32 nm CMOS process.**

***Key Words: - Dual Mode Logic (DML), CMOS, High Performance, Logical Effort, Low Power and Optimization*.**

I. INTRODUCTION

The basic tasks for digital circuit designers are logic optimization and timing estimations. It was Sutherland, who first presented the logical effort (LE) method, for easy and fast assessment and optimization of delay in CMOS logicpaths. The LE method has developedas a very widely held tool for designing and education purposes because of its elegance and is adopted to be the basis for several computer-aided-design tools.Granting LE is mainly used for standard CMOS logic, it is also shown to be useful for other logic families, such as the pass transistor logic.

The novel dual mode logic (DML), which provides the designer with a very high level of flexibility, was suggested. It allows on-the-fly switching amid two modes of operation: 1) static and 2) dynamic modes. In the static mode, DML gates accomplish very low power dissipation, with some deprivation in performance, as compared with standard CMOS. On the other hand, dynamic operation of DML gates attains very high speed at the expense of augmented power dissipation.

Anelementary DML gate is composed of any static logic family gate, which can be a conventional CMOS gate, and an extra transistor. DML gates have a very simple and intuitive structure, requiring unconventional sizing methodology to attain the preferred performance. Conventional LE methodology cannot be used with the DML family as it does not contemplate its unconventional sizing rules and topology.

The objective of this project is to develop a humble method for minimizing delays and achieving an optimized number of stages in logical paths containing CMOS-based DML gates. Anintegrated LE method is introduced for the delay evaluation and optimization of logic paths built with DML logic gates. DML-LE responses complete (un-approximate) design problems, which can be resolved numerically, and streamlines these problems to a straightforward and easy computational problematic [approximate and semi-approximate (SA)] solutions with a unified analytic model. Through this model, it is easy estimate the minimum to maximum error under delay approximation and the error in the impartial optimum number of stages for a given logic function. The efficiency of the developed method is shown by a comparison of the theoretical results, achieved using the proposed method with simulation results of the MICROWIND tool using a standard 32-nm technology.

The rest of this paper is planned as follows: a review of the DML family is described in Section II. DML-LE model for simple inverter chains is established in Section III with three dissimilar levels of approximations. In Section IV compare the methods by simplicity and accuracy. The requirement of the optimum number of stages is also described in Section IV, which delivers an intuitive graphical visualization of the problem. DML-LE is prolonged to complex nets containing branching in Section V. In Section VI, the efficiency of the DML-LE theoretical optimization is examined for a standard 32-nm process.

II. DML OVERVIEW

As previously mentioned, an elementary DML gate architecture is poised with a static gate and a supplementary transistor, whose gate is connected to a global clock signal. In this project, we precisely focus on Dual Mode Logic gates that employ conventional CMOS gates on behalf of the static gate implementation.

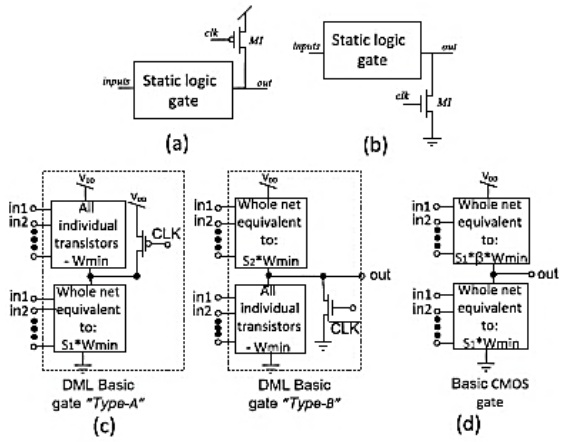


Fig. 1. DML topology: (a) Type *A* and (b) Type *B*. (c) CMOS-based DML gate with sizing factors. (d) Standard CMOS gate with sizing factors.

DML gates are presented with two possible topologies: 1) Type *A*and2) Type *B*, as shown in Fig. 1(a) and (b), consequently. In the static mode of operation, the transistor M1 is turned off by smearing the high Clk signal for Type *A* and low Clk for Type *B* topology. So, the gates of both topologies operate in like way to the static logic gate, which now is a standard CMOS operation.

To activate the gate in the dynamic mode, the Clk is allowed, allowing for two discrete phases: 1) pre-charge and 2) evaluation. Throughout the pre-charge phase, the output is charged to V_{DD}in Type *A*gates and discharged to GND in Type *B* gates. Through evaluation, the output is assessed allowing to the values at the gate inputs.

DML gates demonstrate a very robust process in both static and dynamic modes in process variation at low supply voltages. The toughness in the dynamic mode is mainly achieved by the in-built active restorer (pull-up in Type *A*/pull-down in Type *B*) that also allowed glitch sustaining, charge drip, and charge distribution. It is also exposed that the suitable sizing methodology is the crucial factor to achieve fast operation in the dynamic mode. Fig. 1(c) displays the sizing of Complementary Metal Oxide Semi-Conductor (CMOS)-based DML gates that are optimized to a dynamic mode of operation, whereas Fig. 1(d) displays conventional sizing of a typical CMOS gate. The input and output capacitances of the DML gates are considerably reduced, as related with CMOS gates, due to the application of minimal width transistors in the pull-up of Type 1 or pull-down in Type *B* networks. The size of the pre-charge transistor is kept equal $S*W_{min}$ to uphold a fast pre-charge period even with the increase in the output load.

Differing to CMOS gates, every DML gate can be executed in two ways, only one of which is effective. The ideal topology is such that the pre-charge transistor is positioned in parallel to the stacked transistors, i.e., NOR in Type *A* is favored over NAND, and NAND in Type *B* is desired over NOR. In this event, the evaluation is executedthrough the parallel transistors and hence it isfaster.

The finest design methodology of DML gates is to serially connect Type *A* and Type *B* gates, likewise to np-CMOS/NORtechniques. While this design methodology allows maximum performance, area minimization and improved power efficiency, serial connection of the identical type gates is also possible. However, this case shows many disadvantages, for example the need of footer/header and simple glitching. These well-explored problems are normalfor dynamic gates design. DML asset is that the static mode CMOS-based DML gates with transistor sizes are optimized for the dynamic mode. Because of reduced static and switching energy consumption, Dynamic mode is actually semi-energy optimal CMOS construction of a gate. The static operation of the DML gates is used to considerably reduce energy consumption at the cost of 2–4 times reduction in performance. A common approach is to optimize the delay for the dynamic mode of operation and drive the system in the static mode only in standby/low-energy mode deprived of severe frequency restrictions, i.e., scale of 2–4 times in performance is approachable.

III. DML MODEL FOR SIMPLE INVERTER CHAIN

To enhance the performance of the DML gates, LE technique is needed to employed, modified, and approximated the well-explored. Though LE method is a renowned and widely used by designers, there are a few altered terminologies and metrics. The terminologies will be used to improve the LE for CMOS-based DML gates are presented. The LE design of DML is quite different from the conventional CMOS LE (and domino logic LE), which is conversed in previous section. This is due tounconventional sizing methodology and unique structure of DML gates. Attaining the ideal, non-approximate solution is relatively an exhausting task. However, by slight simplifications it can be solved similarly to the typical CMOS LE method. First, whole non-approximated LE method for DML CMOS-based gates is shown. Even though this solution is very accurate, it is not designer friendly and very complex. Therefore, two approximated solutions are offered. The difficulty of these solutions is much lesser, while attaining very high precision. Lastly, a detail about these approaches for DML LE for all CMOS-based gates is given.

i. Basic Assumptions

DML gates are designed to enhance their dynamic modedelay and thus only one transition amid*T*plhand *T*phl, which is a part of the evaluation phase, should be measured. This illustrates that only acorresponding resistance of the Pull-Down Network (PDN) (nMOSs) will perform a role in delay optimization of Type *A* gates and the Pull-Up Network (PUN) (pMOSs) will be appropriate in optimization of Type *B* gates. Though designing conventional CMOS gates,the PUN is characteristically upsized withβ, independently of the sizing factor EF_{opt}, which is the sizing aid of the load driving effort. This β is the result of the optimal delay of an unloaded gate. Characteristically, β, resulting for an optimal gate delay, is dissimilar from β_{sym}that attains symmetric gate operation (T_{phl}= T_{plh}). Though, in most technologies β is approximately equal to β_{sym}($\beta \approx \beta_{sym}$) [21]. By DML, every stand-alone gate would not be sized with β as the delay in the dynamic mode is defined by a single transition over PDN or PUN and hence there is no necessity in symmetric transitions. One and only sizing factor, S_i, for any *i* stage gate effects the evaluation network and the pre-charge transistor as shown in Fig. 1. In CMOS LE method, the normalization is executed to a typical CMOS inverter. DML gates are normalized to a regular minimal inverter (DML_INV) in Type *A*, which signifies the least standalone gate delay unit. A minimal inverter of Type *B* yields an increased delay, as it calculates the data through pMOS.In this project, assume every DML chain would start with Type *A*gates tailed by Type *B* gates (in a NORA/np-CMOS style).

As stated in the earlier section, 'γ'is the fabrication technology-dependent factor that definesthe transistor gate capacitance to transistor drain capacitance ratio. Usually, in most nanometer scale processes, 'γ'is close to one. For CMOS inverters, it also defines the gate to drain capacitance of a particularMOS transistor. However, for all minimal transistor width DMLINV Type *A* or Type *B* is as follows:

$$\frac{C_{d\_inv\_DML}}{C_{g\_inv\_DML}} = \frac{3C_{d\_MOS}}{2C_{g\_MOS}} \quad (1)$$

$$\text{Yielding:}\gamma' = 3\gamma/2. \quad (2)$$

ii. Defining the Problem for a Simple Inverter Chain

For obtaining the optimal sizing factors to a simple DML inverter chain, just assume a chain as shown in Fig. 2. The delay of a common gate *i* in the chain is known by (3). A normalized delay of every odd gate (Type *A*) and every even gate (Type *B*) can be shown in terms of the delay of a Type *A* minimal DML inverter *t*po_DML as follows:

$$t_{pd\_i} = \underbrace{\frac{\ln(2).R_{min\_A}C_{D,min}}{\gamma'}}_{t_{p0\_DML}} \left(\overbrace{\frac{R_{gate}}{R_{inv}} \cdot \frac{C_{D,gate}}{C_{D,inv}}\gamma'}^{p\_DML} + \overbrace{\frac{R_{gate}}{R_{inv}} \cdot \frac{C_{G,gate}}{C_{G,inv}} \underbrace{\frac{C_{Load}}{C_{G,gate}}}_{f\_DML}}^{LE\_DML} \right) \quad (3)$$

$$t_{pd\_i\_odd} = t_{p0\_DML}\left(\frac{(2S_i+1)}{3S_i}\gamma' + \frac{(S_{i+1}+1)}{2S_i}\right)$$

$$t_{pd\_i\_even} = t_{p0\_DML}\left(\mu_{n/p}\left[\frac{(2S_i+1)}{3S_i}\gamma' + \frac{(S_{i+1}+1)}{2S_i}\right]\right) \quad (4)$$

Where $\mu_{n/p}$is defined as μ_n/μ_p, $S_i$is the *i*th stage sizing factor. Before, supposing an even number of inverters *N* in the chain, the delay of the chain can be stated by adding up the delays of all the chain constituents as

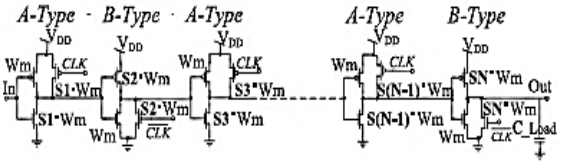
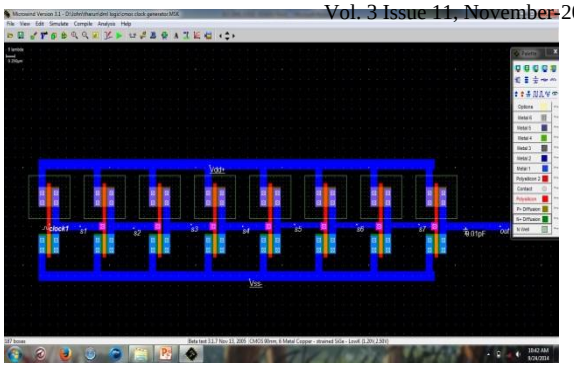


Fig. 2. DML inverter chain with sizing factors (W_m: W_{min}).

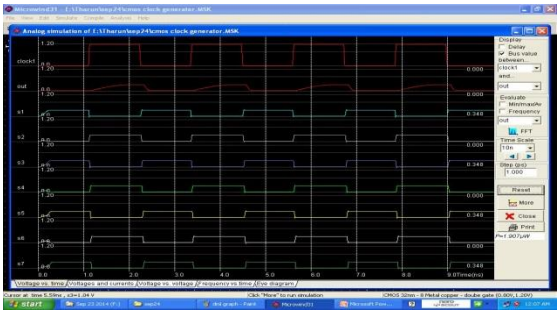
follows:

$$D = \sum_i t_{pd\_i} = t_{p0\_DML} \times \left(\sum_{\substack{odd\_i \\ Type\_A}} \left(\frac{(2S_i+1)}{3S_i}\gamma' + \frac{S_{i+1}+1}{2S_i}\right) + \sum_{\substack{even\_i \\ Type\_A}} \left(\mu_{n/p}\left[\frac{(2S_i+1)}{3S_i}\gamma' + \frac{S_{i+1}+1}{2S_i}\right]\right) \right). \quad (5)$$

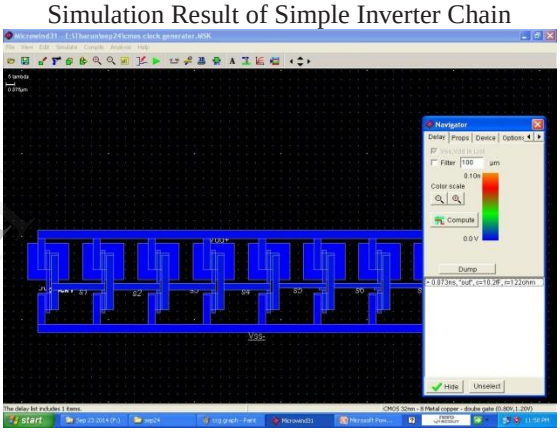
In the next sections, three dissimilar solutions to the delay optimization problem are derived as follows: 1) Complete un-approximated; 2) Complete approximated and 3) partially/SA solutions. These solutions are trading off complexity with accuracy.



Inverter Chain



Simulation Result of Simple Inverter Chain



Delay for Inverter Chain

Power=1.907 μw
Delay=0.073ns
Area :-
Dx=283 lambda (5.660 μm)
Dy=70 lambda (1.40 μm)
So, (Dx)(Dy)=19810 lambda^2 (7.924μm^2)

Power-Delay Product:-
PDP=(1.907 μW)(0.073 ns)= 0.139211 fW-s

iii. Complete Un-approximated (CS) Method for the Sizing Factors of DML Inverter Chain

To solve this problem, differentiate (5) all *Si* factors of the chain and equate to zero, i.e., *dD/dsi*= 0. Afterwards simplifying and substituting γ ', the resulting expression can be written for all odd *i* (6) and all even *i* (7):

$$\frac{S_i}{S_{i-1}} = \frac{(\gamma + 1 + S_{i+1})}{S_i}\frac{1}{\mu_{n/p}} \quad (6)$$

$$\frac{S_i}{S_{i-1}} = \frac{(\gamma + 1 + S_{i+1})}{S_i}\mu_{n/p}. \quad (7)$$

Basically, the first gate in the chain could be all minimal sized transistors and so *S*1 = 1. Supposing, *B* = $\mu n/p$, *B*2 = $(\gamma + 1) \cdot \mu n/p$ (6) and (7) can be signified by the following set of expressions. This is a set of *N* equations with *N*indefinite variables; every equation is nonlinear, comprising mixed

variable multiplication. In common, it can be solved numerically, as below:

$S_1 = 1$

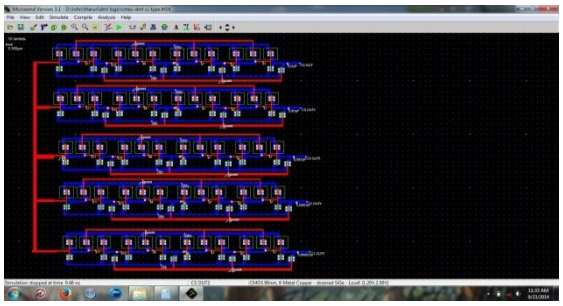
$0 = B_2S_1 - S_{22} + BS_1S_3$

$0 = B_2S_2 - B_2S_{23} + BS_2S_4$
$0 = B_2S_3 - S_{24} + BS_3S_5$

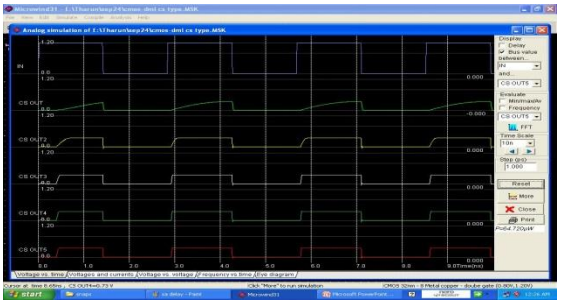
$0 = B_2S_4 - B_2S_{25} + BS_4S_6$
...
...
...
...
...
$S_N^2 = B_2S_{N-1} + BS_{N-1} + BS_{N-1}S_{N+1}.$ (8)

This is the maximum optimal and accurate resolution for DML inverter chain sizing. But, solving it is a very exhausting task. This un-approximated solution (CS) is much more difficult than a simple CMOS LE optimal solution, which is resultant with no assumptions and approximations. DML CS method complexity is owing to a non-standard sizing of transistors, connected in parallel to the Clocked transistor.

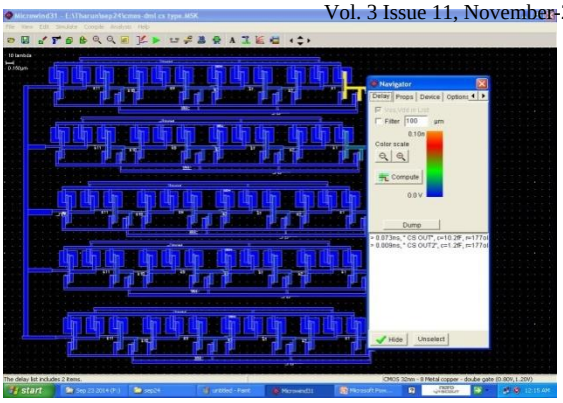
Succeedingsuppositions will be used in the rest of this project. Leading, as solved in previous section, the first gate of any examined chain will be least sized, i.e., S_1=1. S_1can be indiscriminate to some possible sizes in accordance with any input capacitance. Another, even number of stages N is presumed. This is due to the topology of DML chains that mainly consists of Type B gates succeeding Type Agates. Still, the solution for the chain, which has an odd number of stages, can be easily consequential using the same methodology.



Load Capacitance Effect on CS Method



Simulation Result of Load Capacitance Effect on CS Method



Delay for Load Capacitance Effect on CS Method

Load effect on CS:-

Power=64.720 μw

Area :-

Dx=534 lambda (8.010 μm)
Dy=476 lambda (7.140 μm)
So, (Dx)(Dy)=254184 lambda (57.194μm^2)

Power-Delay Product:-
For CS,
PDP_{CS}=(64.720 μW)(0.073 ns)= 4.72456 fW-s
iv. Complete Approximated (CA) Method for the Sizing Factors of DML Inverter Chain

To decrease the difficulty of the LE method, a CA solution, which trades off the accuracy and complexity, is derived.

It is beforehandconferred that (5) defines a common delay expression for the whole chain, supposing an even number of inverters N. The CA method assumes that the involvement of minimal transistors to the drain and gate capacitances is negligible in contrast with 2Si and with Si+1, for every stage of the chain. As exposed in Section V, ignoring these transistors, for complex gates increases the accuracy w.r.t inverters. Then, (5) can be expressed by

$$D = \sum_N D_i = t_{p0\_DML}\left(\sum_{\substack{odd\_i \\ Type\_A}}\left(\frac{(2S_i+1)}{3S_i}\gamma' + \frac{S_{i+1}+1}{2S_i}\right) + \sum_{\substack{even\_i \\ Type\_B}}\left(\mu_{n/p}\left[\frac{(2S_i+1)}{3S_i}\gamma' + \frac{S_{i+1}+1}{2S_i}\right]\right)\right). \quad (9)$$

These suppositions are acceptable only when the output load capacitance of the chain is high. The sizing factors Si is affected by the large load capacitance. As soon as S_i increases, ialsoincreases, along the chain; this calculation will increase in accuracy for high i values. After generalization, (9) can be revised as follows:

$$D = \sum_N D_i = t_{p0\_DML} \times \left(\sum_{\substack{odd\_i \\ Type\_A}}\left(\frac{2}{3}\gamma' + \frac{S_{i+1}}{2S_i}\right) + \sum_{\substack{even\_i \\ Type\_B}}\left(\mu_{n/p}\left[\frac{2}{3}\gamma' + \frac{S_{i+1}}{2S_i}\right]\right)\right). \quad (10)$$

TABLE I
INVERTER CHAIN SIZING FACTORS S_i OF THE CA METHOD

S_1	S_2	S_3	S_4	S_5	S_N	S_{N+1}
1	$\sqrt{\mu_{n/p}}A^{0.5}$	A	$\sqrt{\mu_{n/p}}A^{1.5}$	A^2	$\sqrt{\mu_{n/p}}A^{(\frac{N}{2}-0.5)}$	$A^{\frac{N}{2}}$

By differentiating *dD/dsi*= 0, ensuing the same procedure (Section *B)* for all odd *i* (11) and even *i* (12):

$$\frac{S_i}{S_{i-1}} = \frac{S_{i+1}}{S_i}\frac{1}{\mu_{n/p}} \qquad (11)$$

$$\frac{S_i}{S_{i-1}} = \frac{S_{i-1}}{S_i}\mu_{n/p}. \qquad (12)$$

The sizing factors solution for this CA method is quite related to standard CMOS solution. Likewise to CMOS, the upsizing factor is constant.But every even stage is factored by an additional $\sqrt{\mu_{n/p}}$. On behalf of the *N*-size chain, the sizing factors can be shown in series as in Table I where *A* is expressed in (14). In CMOS, the sizing factors are resulted from the load to input capacitance ratio, while in DML, they are illustrated by the ratio of the first to last sizing factors.

$$\text{In CMOS: } F = \frac{C_{\text{Load}}}{C_{\text{in},g}} = f^N, f = \sqrt[N]{F}. \qquad (13)$$

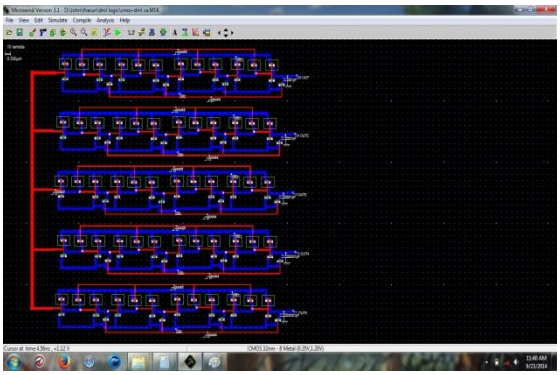
$$\text{In DML: } \frac{S_{N+1}}{S_1} = A^{\frac{N}{2}},\ F_{\text{DML}} = \frac{S_{N+1}}{S_1} = f_{\text{DML}}{}^{\frac{N}{2}},$$
$$A = f_{\text{DML}} = \sqrt[N]{F_{\text{DML}}} \qquad (14)$$

where assuming $S_1 = 1$, S_{N+1} can be extracted from

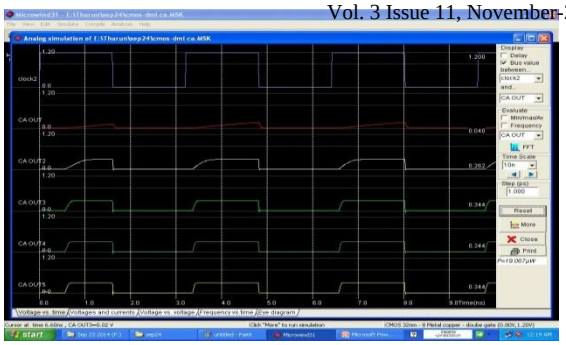
$$\frac{(S_{N+1}+1)\,WL_{\min}}{(S_1+1)\,WL_{\min}} = \frac{S_{N+1}+1}{2} = \frac{C_{\text{Load}}}{C_{\text{in},g}}. \qquad (15)$$

The delay of the total chain is denoted by the sum of delays of all *n*logic stages and of all the added *n*inverters. Distinguishing the chain delay by *N* then equating to zero as follows:

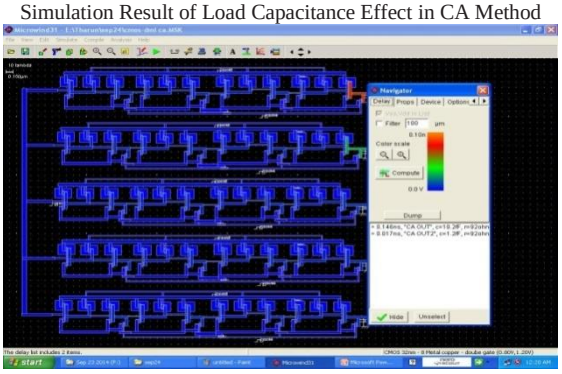
$$\underbrace{\gamma\left(\mu_{n/p}{}^{-0.5}+\mu_{n/p}{}^{0.5}\right)}_{C_1}+\sqrt[N]{F_{\text{DML}}}-\frac{\sqrt[N]{F_{\text{DML}}} * \ln(F_{\text{DML}})}{N} = 0 \qquad (16)$$



Load Capacitance Effect in CA Type



Simulation Result of Load Capacitance Effect in CA Method



Delay for Load Capacitance effect in CA Method

Load effect on CA:-

Power=19.067 μw

Area :-

Dx=505lambda (7.575 μm)

Dy=441 lambda (6.615 μm)

So, (Dx)(Dy)=222705 lambda (50.11μm^2)

Power-Delay Product:-

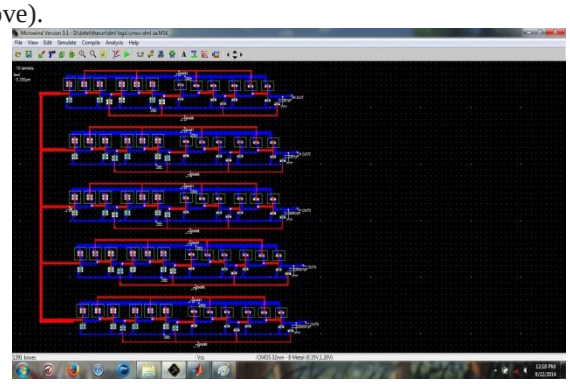
For CA,

PDP_{CA}=(19.067 μW)(0.146 ns)= 2.783782 fW-s

v. SA Method for the Sizing Factors of DML Inverter Chain

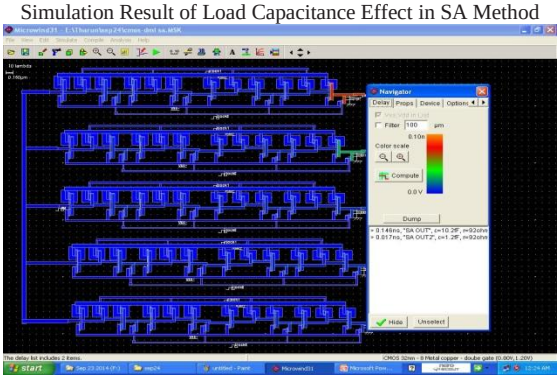
To compromise between the CS and CA methods, a SA approach is introduced. The SA approach is comparatively high precision with compact computational effort w.r.t the CS method.

It is done by ignoring only thefirst and the second terms of (5), as compared with neglectingall terms of the gate and drain capacitances (Complete Approximated method).The solution of the SA is very easy and in addition tothe ordinary CMOS LE optimization manual design, thedesigner should utilize a simple lookup table (given in above).



Load Capacitance Effect in SA Method

Simulation Result of Load Capacitance Effect in SA Method



Delay for Load Capacitance effect in SA Method

Load effect on SA:-

Power=39.180 µw

Area :-

Dx=550 lambda (8.25 µm)

Dy=493 lambda (7.395 µm)

So, (Dx)(Dy)=271150 lambda (61.01µm^2)

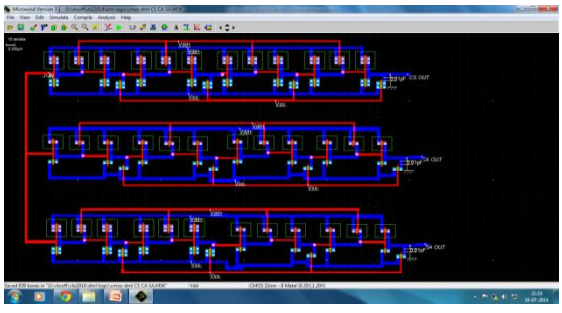
Power-Delay Product:-

For SA,

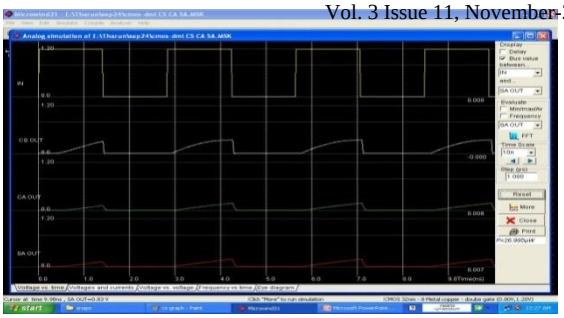
PDP_{SA}=(39.180 µW)(0.146 ns)= 6.61249 fW-s

IV. COMPARISON OF THE DML METHODS

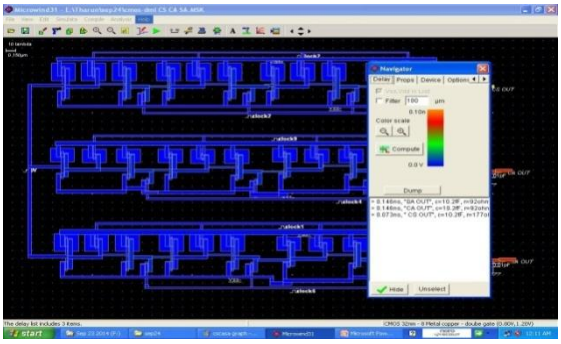
Now, a comparison between the SA, CS, and CA techniques is shown. The techniques are compared with simplicity, accuracy and depend on delay in the optimum number of stages.



Comparison of DML CS, CA and SA Methods



Simulation Results for Comparison of DML CA, CS and SA Methods



Delay for Comparison of DML CA, CS and SA Methods

Comparison between CA, CS and SA Methods:-

Power=26.995µw

Area :-

Dx=494lambda (7.410 µm)

Dy=297 lambda (4.455 µm)

So, (Dx)(Dy)=146718 lambda (33.01µm^2)

Power-Delay Product:-

For CA,

PDP_{CA}= (26.995 µW)(0.146 ns)= 3.94127 fW-s

For CS,

PDP_{CS}= (26.995 µW)(0.073 ns) = 1.970635 fW-s

For SA,

PDP_{SA}= (26.995 µW)(0.146 ns)= 3.94127 fW-s

V. DML EVALUATION FOR COMPLEX GATES AND BRANCHES IN 32 nm PROCESS

The proposed methodology is observed by results derived by MICROWIND tool. The evaluation is executed on two different complex logic networks, realized in a low power typical 32nm technology.

The DML Methods are compared for universal gates NAND & NOR gates, also complex gates like AOI_{21} and OAI_{21} gates.

For 3-input NAND Gate:

First, 3-input NAND gate is implemented using DML methods and compared for Type A and Type B for every methods are tabulated in Table A.

For 3-input NOR Gates:

Now,3-input NOR gate is implemented using DML methods and compared for Type A and Type B in every method are tabulated in Table B.

For AOI_{21} Gate:

Just like above, the same procedure is followed for AND-OR-INVERTER gate which is derived as (A(B+C))'. This AOI_{21} gate is implemented using DML methods and compared for Type A and Type B in every method are tabulated in Table C.

For OAI_{21} Gate:

For OAI_{21} (OR-AND-INVERTER) gate i.e., ((A+B)C)', also executed as in AOI_{21} Gate and is tabulated in Table D.

VI. CONCLUSION

The proposed approach permitted an efficient optimization of DML logic networks for full performance in the dynamic mode of operation, which was the focus of this project. DML logic, optimized conferring to the proposed DML methods, allowed long flexibility in optimizing several structures of DML networks. This optimization usedthe DML inherent properties which significantly condensed parasitic capacitance and ultra-low power dissipation in the static operation mode.

This projectoffered three different approaches, which traded off between complexity, computation and accuracy. The complex CS method was only spoken for error analysis of the further methods. The CA method was indistinguishable to CMOS computation with very minor error and the SA method was also identical to the CMOS computation assisting one more lookup table (which easily derived for all cases and loads). Analysis showed that with these tools only a design can attain very high performance results.

The desired DML gates topology is such that the pre-charge transistor is located in parallel to the stacked transistors, i.e., NOR in Type *A* is preferred over a NAND, and NAND in Type *B* is preferred over NOR.

Advantages and drawbacks of each one of the methods were conferred. Simulation results were carried out in a standard 32-nm process, verified the efficiency of the proposed approach and again compared it with existing CMOS.

Gate	Power (µW)	Delay (ns)	Power-Delay Product (f W-s)	Dx ʎ (or µm)	Dy ʎ (or µm)	Area $ʎ^2$ (or $µm^2$)
NAND_normal	0.331	0.030	0.009	162(3.24)	120(2.40)	19440(7.78)
NAND_TA_CA	0.305	0.053	0.016	184(3.68)	130(2.60)	23920(9.57)
NAND_TA_CS	0.346	0.029	0.010	187(3.74)	132(2.64)	24684(9.87)
NAND_TA_SA	0.352	0.029	0.010	185(3.70)	129(2.58)	23865(9.55)
NAND_TB_CA	11.472	0.056	0.642	185(3.70)	129(2.58)	23865(9.55)
NAND_TB_CS	17.511	0.031	0.543	186(3.72)	129(2.58)	23994(9.60)
NAND_TB_SA	17.500	0.036	0.630	183(3.66)	128(2.56)	23424(9.37)

Table A: Simulation Results comparison of NAND gate

Gate	Power (µW)	Delay (ns)	Power-Delay Product (f W-s)	Dx ʎ (or µm)	Dy ʎ (or µm)	Area $ʎ^2$ (or $µm^2$)
NOR_normal	0.357	0.090	0.032	160(3.20)	107(2.14)	17120(6.85)
NOR_TA_CA	12.595	0.085	1.070	184(3.68)	112(2.24)	20608(8.24)
NOR_TA_CS	29.716	0.046	1.367	182(3.64)	114(2.28)	20748(8.30)
NOR_TA_SA	13.163	0.085	1.119	184(3.68)	111(2.22)	20424(8.17)
NOR_TB_CA	0.324	0.169	0.055	183(3.66)	111(2.22)	20313(8.13)
NOR_TB_CS	0.374	0.092	0.034	183(3.66)	113(2.26)	20679(8.27)
NOR_TB_SA	0.354	0.169	0.059	183(3.66)	112(2.24)	20496(8.20)

Table B: Simulation Results comparison of NOR gate

Gate	Power (µW)	Delay (ns)	Power-Delay Product (f W-s)	Dx ʎ (or µm)	Dy ʎ (or µm)	Area $ʎ^2$ (or $µm^2$)
AOI_normal	0.160	0.044	0.007	167(3.34)	124(2.48)	20708(8.283)
AOI_TA_CA	5.866	0.055	0.323	185(3.70)	129(2.58)	23865(9.550)
AOI_TA_CS	13.118	0.030	0.340	186(3.72)	130(2.60)	24180(9.670)
AOI_TA_SA	5.988	0.052	0.311	187(3.74)	130(2.60)	24310(9.720)
AOI_TB_CA	6.530	0.083	0.542	185(3.70)	128(2.56)	23680(9.470)
AOI_TB_CS	15.023	0.045	0.676	184(3.68)	128(2.56)	23552(9.42)
AOI_TB_SA	6.546	0.058	0.380	186(3.72)	131(2.62)	24366(9.75)

Table C: Simulation Results comparison of AOI_{21} gate

Gate	Power (µW)	Delay (ns)	Power-Delay Product (f W-s)	Dx ʎ (or µm)	Dy ʎ (or µm)	Area $ʎ^2$ (or $µm^2$)
OAI_normal	0.356	0.045	0.016	160(3.2)	119(2.38)	19040(7.62)
OAI_TA_CA	0.325	0.056	0.018	183(3.66)	129(2.58)	23607(9.44)
OAI_TA_CS	0.369	0.031	0.011	183(3.66)	128(2.56)	23424(9.37)
OAI_TA_SA	0.346	0.044	0.015	183(3.66)	131(2.62)	23973(9.59)
OAI_TB_CA	2.012	0.084	0.169	182(3.64)	128(2.56)	23296(9.32)
OAI_TB_CS	4.410	0.046	0.202	185(3.70)	128(2.56)	23680(9.47)
OAI_TB_SA	4.144	0.059	0.244	185(3.70)	129(2.58)	23865(9.55)

Table D: Simulation Results comparison of OAI_{21} gate

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