Optimization Of Power In Hybrid Circuits Using Adiabatic Techniques

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ABSTRACT

Low power and low noise digital circuits has intrigued designers to explore new options in the world of circuit design. One approach that seems to be very promising is the famous energy-recovering (adiabatic) logic. Adiabatic circuits pursue low energy dissipation by restricting the current to flow across devices with low voltage drop and by recycling the energy stored in the capacitors. The energy consumption is analyzed by variation of parameters. In the analysis, two logic families, ECRL (Efficient Charge Recovery Logic) and PFAL (Positive Feedback Adiabatic Logic) are compared with conventional CMOS logic for inverter and Ring counter. The results show that adiabatic technique is a good choice for low power and low area application in specified frequency range.

INTRODUCTION

The explosive growth in laptop and portable systems and in cellular networks has intensified the research efforts in low power microelectronics. Today there is an ever-increasing number of portable applications requiring low power and high throughput than ever before. Equally demanding are developments in personal communication services (PCS's), such as the current generation of digital cellular telephony networks which employ complex speech compression algorithms and sophisticated radio modems in a pocket sized device. Even more dramatic are the proposed future PCS applications, with universal portable multimedia access supporting full motion digital video and control via speech recognition.

Thus, designing low-power digital systems especially the processor is

becoming equally important to designing a high performance one. Fully adiabatic operation of a circuit is an ideal condition. It may be only achieved with very slow switching speed. In practical cases, energy dissipation with a charge transfer event is composed of an adiabatic component and a non-adiabatic component

DISSIPATION MECHANISMS IN ADIABATIC LOGIC CIRCUITS

Fig.1 shows the equivalent circuit used to model the conventional CMOS circuits during charging process of the output load capacitance. But here constant voltage source is replaced with the constant current source to charge and discharge the output load capacitance. Here R is on resistance of the PMOS network, C_L is the load capacitance.
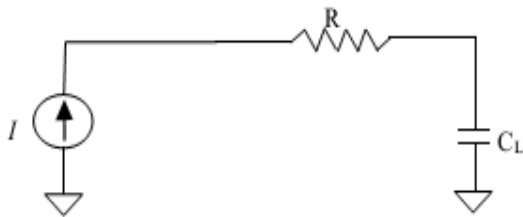

Figure-1

Energy dissipation in resistance R is

$$E_{diss} = I^2.R.T = \left(\frac{C_L V_{DD}}{T}\right)^2.R.T = \left(\frac{RC_L}{T}\right).C_L V_{DD}^2$$

Since E_{diss} depends upon R, by reducing the on resistance of PMOS network, the energy dissipation can be minimized. The on resistance of the MOSFET is given by the \ first order approximation

$$R = \left[\mu C_{OX} \frac{W}{L}(V_{GS} - V_{th})\right]^{-1}$$

The energy stored at output can be retrieved by reversing the current source direction during discharging process instead of dissipation in NMOS network. Hence adiabatic switching technique offers less energy dissipation in PMOS network and reuses the stored energy in the output load capacitance by reversing the current source direction.

ADIABATIC LOGIC FAMILIES

Many adiabatic logic design techniques are given in literature, but here two of them are chosen-ECRL and PFAL. These techniques show that there is good improvement in energy dissipation and are mostly used as reference in new logic families.

A. Efficient Charge Recovery Logic (ECRL) Inverter:

The schematic and simulated waveform of the ECRL inverter gate is shown in figure-2 and figure-a. Initially, input 'in' is high and input '/in' is low and power clock (pck) rises from zero to V_{DD} and F is at output (out) remains at ground level, output '/out' follows the pck.
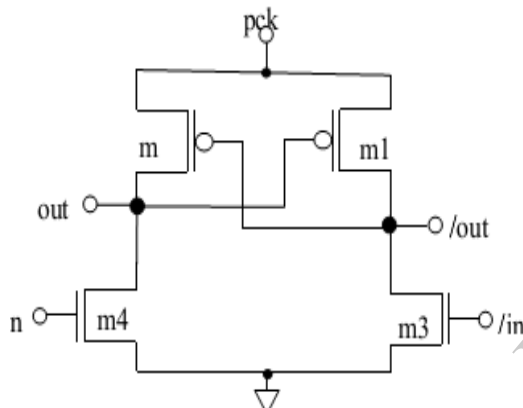

Figure-2

The output values can be used for next stage as inputs. Now pck falls from V_{DD} to zero, '/out' returns its energy to pck due to which delivered charge is recovered. ECRL uses four phase clocking technique to efficiently recover the charge delivered by pck. When pck reaches at V_{DD}, outputs (out) and (/out) hold logic values zero and V_{DD} respectively.

B. Positive Feedback Adiabatic Logic (PFAL) Inverter:

The schematic of PFAL inverter gate is shown in figure-3. Initially, if input 'in' is high and input '/in' is low and power clock (pck) rises from zero to V_{DD}, then F and m4 are at output (out) remains at ground level, output '/out' follows the pck.
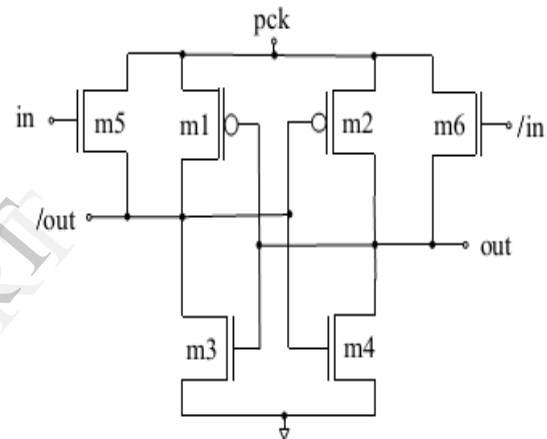

Figure-3

When pck reaches at V_{DD}, outputs 'out' and '/out' hold logic values zero and V_{DD} respectively. These output values can be used for the next stage as inputs. If pck falls from V_{DD} to zero, '/out' returns its energy to pck thereby delivered charge is recovered. PFAL uses four phase clocking technique to recover the charge delivered by pck efficiently.

RING COUNTER USING ECRL

Having observed the fact that only one of the DFFs in the ring counter is activated, the gated-clock technique has then been applied to the DFFs. In this approach, every eight DFFs in the ring counter are grouped into one block. Then, a "gate" signal is computed for each block to gate the frequently toggled clock signal when the block can be inactive so that unnecessary power wasted in clock signal transitions is saved.
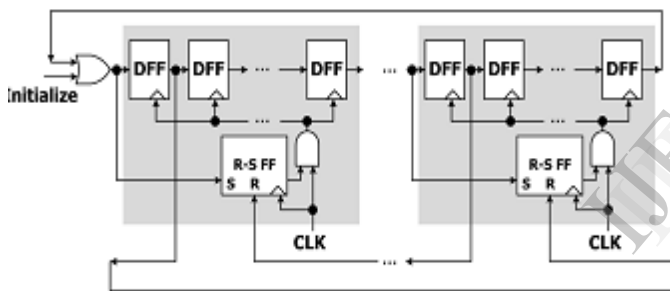

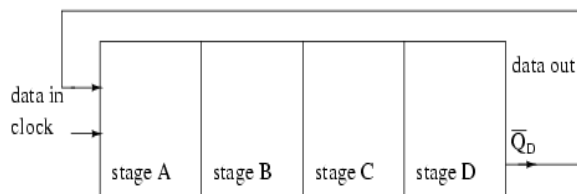**Figure-4 Ring counter with SR flip-flops**

Figure-5 Ring counter, shift register output fed back to input

Provisions are made for loading data into the parallel-in/ serial-out shift register configured as a ring counter below. Any random pattern may be loaded. The most generally useful pattern is a single **1**.
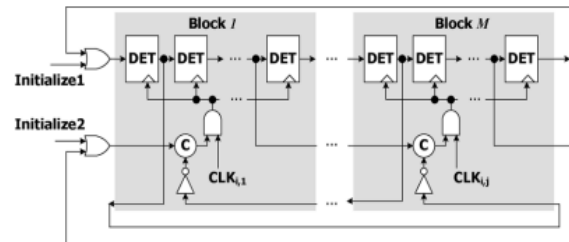
RING COUNTER USING PFAL:

Figure-6

DET: (Double edge triggered flip-flops: Double edge-triggered flip flops are becoming a popular technique for low-power designs since they effectively reduce the clock frequency by half. The logic construction of a double-edge-triggered (DET) flip-flop, which can receives input signals at two levels of the clock, is analyzed and a new circuit is designed namely CMOS DET. According to Hossain et al, a single-edge triggered flip flop can be implemented by two transparent latches in series, a double edge-triggered flip-flop can be implemented by two transparent latches in parallel.

C ELEMENT: The Muller **C-element**, or Muller C-gate, is a commonly used asynchronous logic component originally

designed by David E. Muller. It performs logical operations on the inputs and has hysteresis. The output of the C-element reflects the inputs when the states of all inputs match. The output remains in this state until the inputs all transition to the other state.
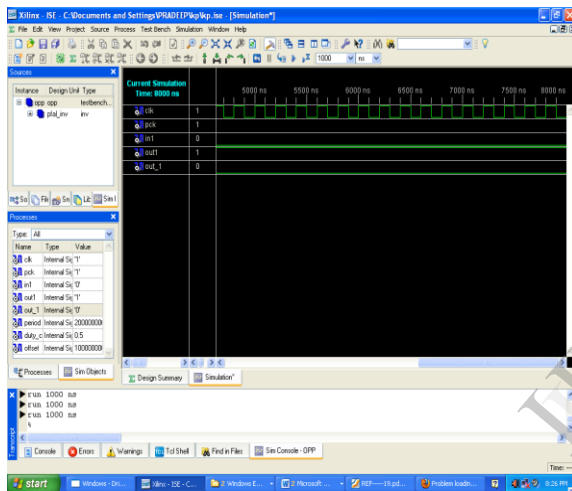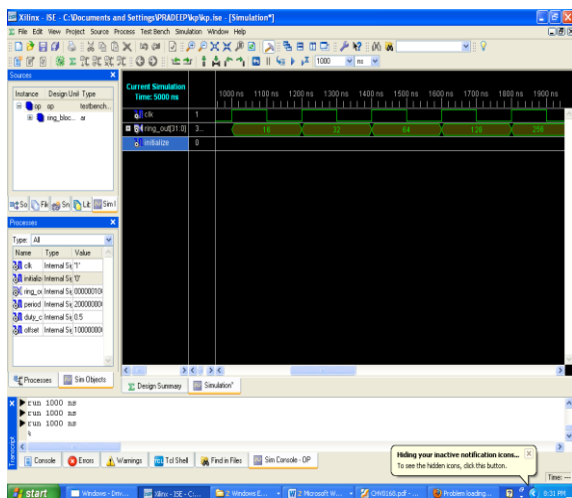
SIMULATION RESULTS:

Figure-A: Inverter:

Figure-B: Ring Counter:

POWER CONSUMPTION:

Target Device : xc4vlx15-12-ff676

Frequency	ECRL		PFAL	
	Inverter (µW)	Ring counter (µW)	Inverter (µW)	Ring counter (µW)
50 MHz	44	41	43	13
100 MHz	80	74	77	17
150 MHz	115	106	111	20
200 MHz	150	138	145	24

CONCLUSION:

With the adiabatic switching approach, the circuit energies are conserved rather than dissipated as heat. Depending on the application and the system requirements, this approach can be used to reduce the power dissipation of the digital systems. With the help of adiabatic logic, the energy savings of upto 76% to 90% can be reached. Circuit simulations show that the adiabatic design units can save energy by a factor of 10 at 50 MHz and about 2 at 250 MHz, as compared to logically equivalent conventional CMOS implementation.

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