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Performance Analysis Of 8-Bit ALU For Power In 32 Nm Scale

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ABSTRACT

The 32 nm process (also called 32 nanometer node) is the next step after the 45 nanometer process in CMOS semiconductor device fabrication. Like the 45 nm generation, the 32 nm node will take advantage of the performance tricks of the prior technology generation, including immersion lithography. The biggest change at 32 nm will be the introduction of high-k dielectrics and metal gates into production.

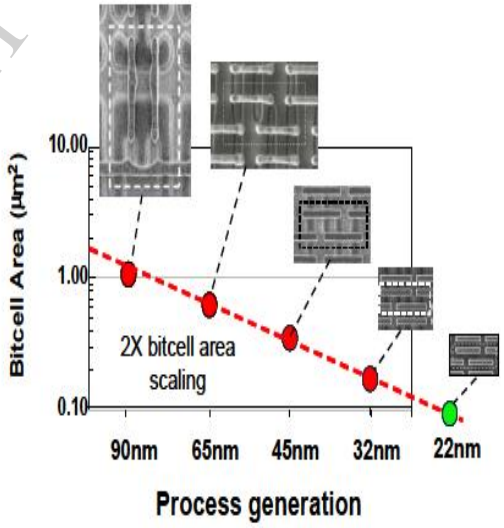
The development of next 32 nm generation needs innovations on not only device structures, but also fabrication techniques and material selections. . This reduces the Power Dissipation and Leakage Current in the designing of any circuitry. The major sources of leakage current are the gate direct tunneling current, the sub-threshold leakage and the reverse biased band-to-band-tunneling junction leakage. To reduce total chip power, these leakage components must be suppressed.

Here, for giving the advantages of 32nm scale technology 8-bit ALU was simulated on the different number of integration scale. The advantages of 32nm technology will be given over the other scaling technology. Result can be analyzed by simulating the schematic circuit with the help of CAD tools as DSCH & MICROWIND. This project work will help in giving the advantages of 32nm scale on comparing with the other counter parts and to provide the information about the advanced half node technology.

1. INTRODUCTION

CMOS technology scaling has allowed for unprecedented integration of analog and digital circuits onto a single chip. For the past 40 years, relentless focus on transistor scaling and Moore's Law led to ever-higher transistor performance and density, translating into tremendous increases in microprocessor functionality and performance. Traditional device scaling led to a steady increase in leakages which threatened the continuance of Moore's Law.

The introduction of high-k dielectric gate transistors on the 32nm generation broke through some of these scaling barriers. At the 32 nm node, high-K dielectric gate will be the mainstream gate stack in high volume manufacturing. In this space, gate length and contact all must be scaled.



1.1 Proposed Work:

This project requires designing of circuit, performance & implementing an offline system & simulating the same on 32nm scale and comparing it with 90nm, 65nm, 45nm and 25nm scale.

1.2 Objective:

The objective of the proposed work is to design a system based on these aims.

1. Our first aim is to give the advantages of 32nm scale on comparing with the other counter parts.

2. To provide the information about the advanced half node technology.

1.3 System Overview:

In this project 8-bit ALU is designed. The ALU having two data input A and B. Here, three selection lines S (3-bit long) given to the ALU and one input carry line is also give to the ALU. Because of 3 selection lines the ALU can be performing maximum 8 numbers of operations from arithmetic and logic functions. These selection lines are combined to perform a function F (8-bit long).

Finally the output of ALU which we are desire will be the combination of two inputs and three selection lines, which is an 8-bit data.

2. PROBLEM IDENTIFICATION:

2.1 Effect of scaling:

For driving the MOSFET (Metal Oxide Semiconductor Field effect transistor) key parameter is the scaling of the transistor gate length, which has a significant performance impact at the 32nm node & beyond. Because of the large gate tunneling currents, the gate oxide cannot be further scaled down and beyond the 45nm node the channel length scaling without gate dielectric scaling actually degrades transistor drive current and performance.

As the gate oxide thickness of a transistor reduces performance of the transistor become poor. This will give the negative impact on all over performance of the CMOS logic circuit.

2.2 Sizing of Chip:

This sizing of the chip will be done keeping in consideration of all over performance of the CMOS logic circuitry. If the size of the chip was decreases the inevitable disadvantages occurring in the digital design circuit. For sizings purpose many parameters are considered like W/L ratio, gate dielectric layer, gate oxide thickness etc. For achieving this purpose semiconductor engineers have continuously decreases the thickness of the gate dielectric layer, higher leakage current will be resulted in the reduced dielectric thickness.

3. METHODOLOGY:

3.1 Study of 32nm Scale Technology:

For applying the maximum number of transistors in a single chip or the further reduction in the circuit area for achieving the small chip size, the 32nm is the next generation technology. The 32nm scale technology is a design technique of making chips in VLSI after the 45nm scale technology. The 32nm technology uses very much different and advanced technology for designing any CMOS logic circuitry.

4. RESULTS & DISSCUSSION:

The designed 8-bit ALU was simulated to analyze performance for Power Dissipation & Leakage Current. Further the layout of the design 8-bit ALU was created and will be extracted at different nm scaling technology. Later in the chapter we also compare the obtained parameter for Power Dissipation & Leakage Current on default 65nm, 45nm, 32nm and 22nm scaling technology through the layout simulation results. The different results are presented here.

The results come from the simulation can be further compared with using the theoretical formula of Power Dissipation & Leakage Current.

4.1 Formula for Power Dissipation:

$$P_d = (I_{avg}) \times (V_{dd})$$

Where, I_{avg} = average current,

V_{dd} = applied voltage.

4.2 Formula for Leakage Current:

$$I_{leakage} = I_0 \, e^{(v_{gs} - v_{th})/nv_t}$$

Here, $I_0 = \mu_0 C_{ox} [W/L] V_t 2e^{1.8}$

Where, C_{ox}= gate oxide capacitance,

(W/L) = width to length ratio of the leaking MOS device,

μ_0 = zero bias mobility,

V_{gs} = gate to source voltage,

V_t = thermal voltage and

n =2 (sub-threshold swing coefficient

4.3 Result of Simulated ALU:

SCALE	LEAKAGE CURRENT		POWER DISSIPATION
	MAXIMUM	AVERAGE	
65nm	7.840mA	0.234mA	0.164mW
45nm	1.529mA	0.032mA	12.633µW
32nm	1.090mA	0.021mA	7.293µW
25nm	43.943mA	2.201mA	5.503mW

4.4 result of calculation of ALU:

SCALE	LEAKAGE CURRENT	POWER DISSIPATION
65nm	7.55 mA	0.1638mW
45nm	1.64103 mA	12.8µW
32nm	1.03 mA	7.35µW
25nm	44.981 mA	5.5025mW

5. Conclusion:

For 32nm technology, it is to be said "High performance at low power".

Here simulation was performed for quantitatively evaluation for the benefits of 32nm scaling technology with channel length scaling. The result shows that MG devices with scaled Tinv and EOT exhibit electrostatic and performance advantages over PG devices. MG/HK also provides additional channel length scaling without degrading the total leakage current of the chip for 32nm high performance CMOS devices and beyond. From the table (comparison of different scaling technology for 8-bit ALU) it can be concluding that the 32nm scaling technology running with the very much high, good and efficient performance for the fabrication of the Chips in the VLSI industries.

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