Performance Analysis of Cascaded H-Bridge Multilevel Inverter Fed PMSM Drive

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***Abstract* — In this paper, 3 phase cascaded Half-Bridge (CHB) multilevel inverter topology is presented based on power cells connected in cascaded mode using two inverter legs in series. Half-Bridge cells are usually connected in cascaded mode on their ac side to achieve medium-voltage operation and reduction of harmonic effect. Both IGBT/Diode switches are used in same leg with input voltage as Vdc/2. The severity of explosion of power cell is reduced to half by this connection as half power is dissipated in switches. It improves reliability of system. Three phase cascaded Half-bridge multilevel inverter is designed by using phase shift multicarrier pulse width modulation fed permanent magnet synchronous motor (PMSM) drive for best results in high power high voltage applications. Simulation results were carried out using MATLAB/Simulink. Steady state and dynamic performance of drive is validated.**

Keywords— Cascaded System; Multilevel System Inverters; Pulse Width Modulation (PWM); permanent magnet synchronous motor (PMSM); Medium-voltage drives

I. INTRODUCTION

The PMSM motors are most suitable motors in application field which require fast dynamic response of speed, because of their high efficiency and can be easily controlled in a wide speed range. This is relatively new class of motors whose application have been increasing at a rapid rate each year, due to declining costs as well as increasing functionality [7-8]. In PMSM, the electromagnetic field system is absent. Slip rings and brushes are replaced by permanent magnets. The use of permanent magnets eliminates field copper loss, brush friction loss. This result in high efficiency of PMSM compared to a conventional synchronous motor. The advantages of PMSM combined with the availability of advanced permanent magnets whose cost is low lead to wide spread use of PMSM in several variable speed drives.

Recent decade's multilevel inverters have been attracting wide industrial interest. The main characteristics of these inverters are an output waveform with multiple voltage levels. With the use of these Multilevel inverters we can reduce the harmonic content to a great extent. By using more no of steps harmonics can be further more reduced. Traditional multilevel inverter topologies are classified into mainly three types: 1) Diode clamped/neutral point clamped (NPC) multilevel inverter, 2) Flying capacitor (FC) multilevel inverter, and 3) cascaded Half-Bridge (CHB) multilevel inverter [4]. Other topologies such as the hybrid converters are not fully received for industrial applications.

In case of the cascaded Half-bridge multilevel converter have the advantage of connecting single-phase inverters in series that are fed by unequal dc voltage sources or single dc source, showing the possibility of different implementations for this topology [6]. An alternative three-phase cascaded multilevel inverter topology is proposed in this paper. It uses power cells connected in cascade using two inverter legs in series, instead of two parallel inverter legs, as conventionally found in CHB power cells. A detailed analysis of the proposed structure with five levels is carried out using pulse width-modulation phase- shifted multicarrier modulation.

In this paper, five level Cascaded Half-Bridge multilevel inverter fed PMSM drive is implemented in MATLAB/Simulink and simulation results are presented for verification and validation of the proposed work.

II. PROPOSED TOPOLOGY

The proposed three phase multilevel inverter fed PMSM is as shown in Fig.1. This inverter is composed of (3VLL−3) switches and (3VLL−3)/2 isolated dc voltage sources, where VLL is the number of voltage levels of the line-to-line output voltage. The load can be connected in delta or wye.

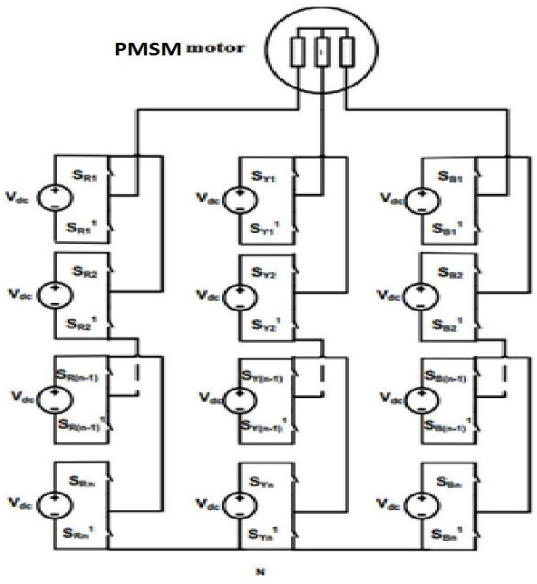

Fig. 1. Proposed multilevel Inverter fed PMSM drive

A basic inverter leg with two switches, working in a complementary way, is shown in Fig. 2(a). Each power cell is composed of two inverter legs with the connections defined in Fig. 2(b).Voltage VPC(t) in Fig. 2(b) is composed of three voltage levels: Vdc, 0, and−Vdc. When switches Sp−1and Sp conduct, the output voltage in the power cell is Vc(t) =Vdc. Similarly, with S/p−1 and S/p switched on, Vc(t) = −Vdc. To obtain the level zero, the switches Sp−1 and S/p or S/p−1 and Sp should be switched on.

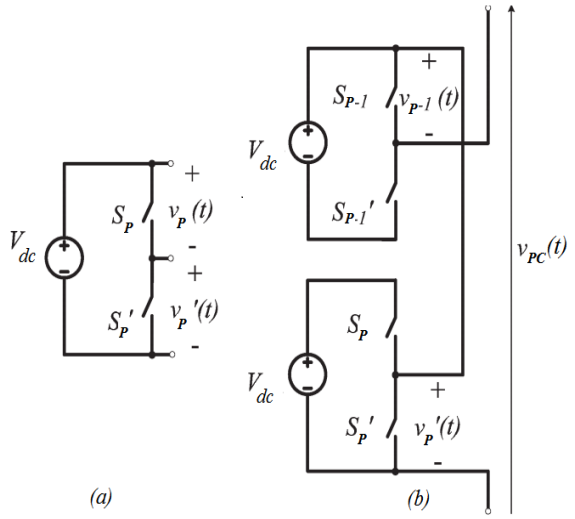

Fig. 2. (a) Inverter leg connected to isolated dc voltage source. (b) Power cell using two inverter legs connected in series.

Thus, by connecting the power cells in cascade (Fig. 3), with a certain phase shift in the switch command between two power cells in the same phase, the number of voltage levels from phase-to-neutral voltage (VPN) can be arbitrarily increase[13-16].

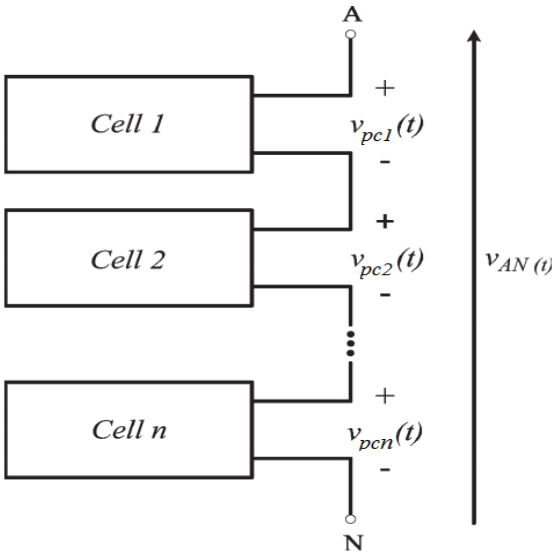

Fig. 3. Per-phase diagram of power cell in cascade

The maximum numbers of voltage levels of the line-to-line output voltage Vab (t) and phase-to-neutral voltage Van (t) are respectively represented by

$$V_{LL} = 4Np+1 \quad (1)$$

$$V_{PN} = 2Np+1 \quad (2)$$

Where Np is the number of power cells per phase. By construction, the number of voltage levels for this topology is always odd.

By selecting proper switching functions, positive, negative, and zero voltages can be synthesized. The output voltage VO is the sum of the output voltage produced by each Half-bridge cell. Hence, every Half-bridge module requires an independent voltage source.

III. PHASE SHIFTED CARRIER PWM (PSCPWM) APPLIED TO PROPOSED MULTILEVEL INVERTER

For the Cascaded inverter, Phase Shifted Carrier Pulse width modulation (PSCPWM) is the standard modulation strategy. For this technique the modulation of the full bridge inverters in each multilevel phase leg is modular. Recent work has shown that better results for a Cascaded inverter occur when each full bridge inverter is controlled using three level modulations. With this approach, the sinusoidal reference waveforms for the two phase legs of each full bridge inverter are phase shifted by 180°, while the carriers between the full bridge inverters are phase shifted by 180°/" (N' is the number of full bridge inverters in a multilevel phase leg). This strategy leads to cancellation of all carrier and associated sideband harmonics up to the 2N''h carrier group [17].

Phase shift multicarrier pulse width modulation technique was used shown in Fig. 4, all the triangular carriers have the same frequency and the same peak-to-peak amplitude and phase shift between two adjacent carrier waves to increase harmonic cancellation. A phase shift defined by

$$(K-1)/N_P \qquad K = 1,2,3,.....,2N_P \quad (3)$$

Designed for an inverter with two power cells in cascade, it is necessary to occupy four triangular carriers with phase shifts of 0, π/2, π, and 3π/2. The upper switch-gate signals for one phase are shown in Fig. 4, because the lower switch-gate signals are complementary. The other two phases are shifted by±120◦. Comparison between the triangular carriers and the modulator is carried out to obtain the switch gate signals as shown in Fig.4. The ensuing signal would be lofty when the instantaneous values of the sinusoidal wave surpass the triangular carrier; or else, it would be lowered. These high- frequency pulses are sent to the switches of the circuit in Fig. 1, with four inverter legs in cascade [12] [19].

In Fig. 5, the modulation schematic is given. The phase shift modulation portrayed here is comparable to the one used in CHB multilevel inverters. A CHB multilevel inverter with Vpn voltage levels entails (Vpn − 1) triangular carriers. In the phase-shifted multicarrier modulation, all the triangular carriers embrace the identical frequency and the same peak-to- peak amplitude, in the company of a phase shift between any two neighboring carrier waves. Nevertheless, the phase shift involving two parallel inverter legs of each power cell ought to be 180◦.

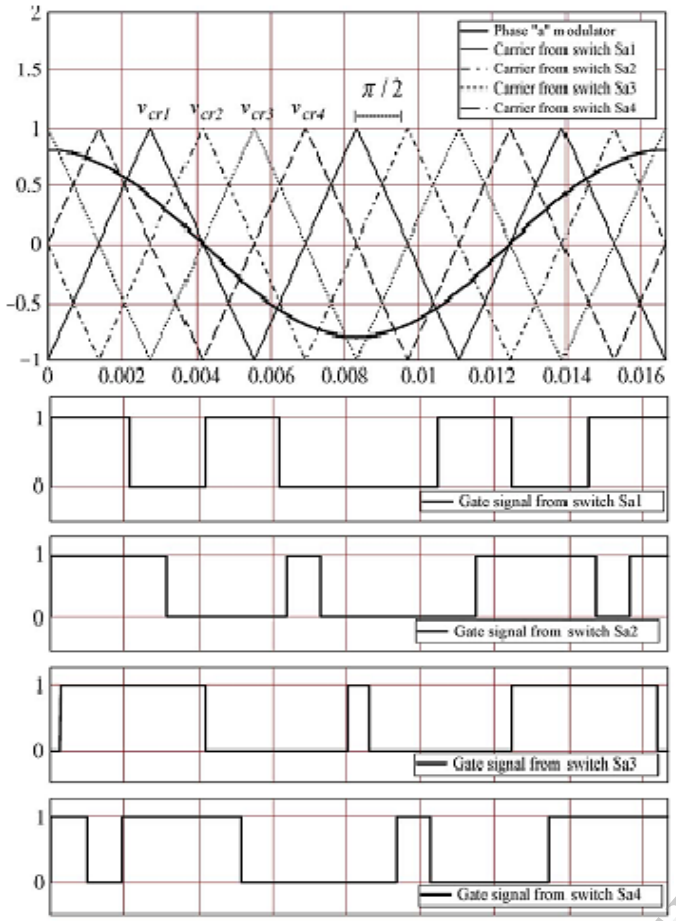

Fig. 4. Simulated waveform of the proposed multilevel inverter

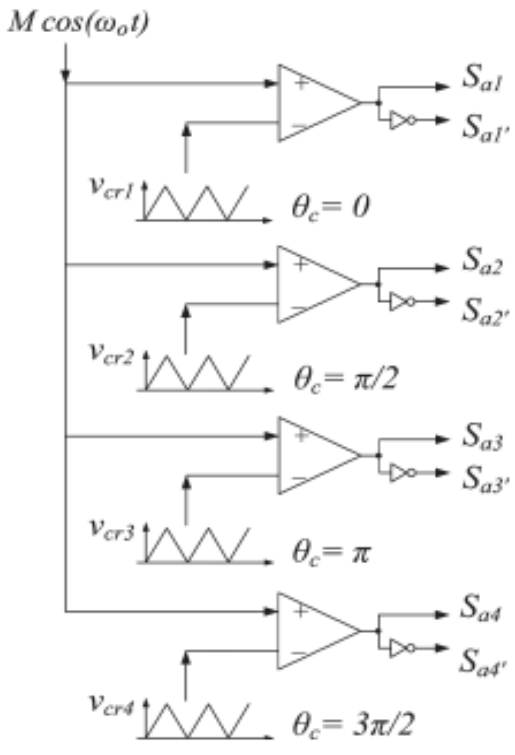

Fig. 5. Simplified modulation schematic

All comparators share the same modulator waveform, and each unipolar triangular carrier has an unwavering shift. The proposed CHB uses less number of switches to fabricate supplementary voltage levels [9]. This will shrink Gate Drivers and protection circuit requirement accordingly it diminish cost and intricacy of the circuit.

IV. SIMULATION RESULTS

The proposed cascade half bridge cell multilevel inverter fed PMSM with phase shifted PWM modulation technique has been developed using MATLAB/Simulink. Fig. 6 Shows the MATLAB/Simulink model of three-phase cascaded half bridge inverter fed PMSM drive.

In this proposed topology, power cells linked in cascade using two inverter legs in series, as an alternative of two parallel inverter legs, set up in CHB power cells, conservatively. In this proposed topology input voltage is Vdc/2 and in condition any module goes amiss, and the topology can maneuver with shortened output voltage and consequently reduced power. So that severity of explosion is reduced to half and results in increase of the reliability of the system and cost effectual [18].

Fig. 7 shows the inside view of one phase leg. It uses power cells connected in cascade using two inverter legs in series, instead of two parallel inverter legs, as conventionally found in CHB power cells. Output voltage between phase-neutral of 5-level proposed multilevel inverter is shown in Fig.8.

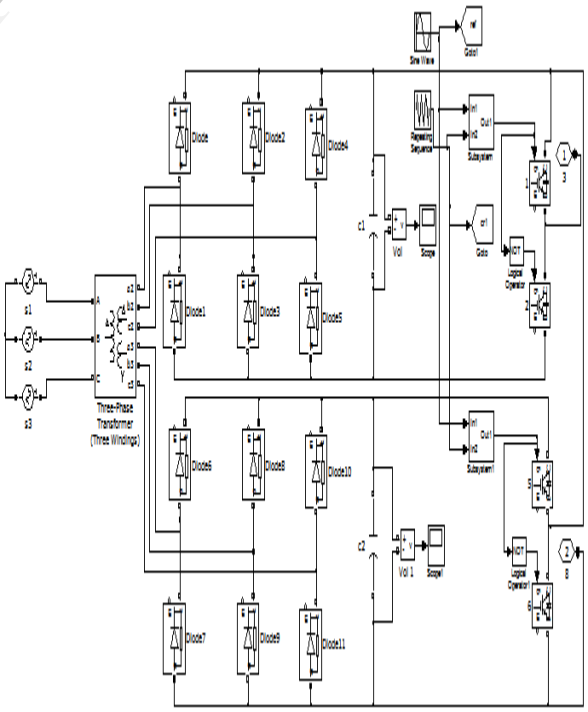

Fig. 6. Simulink model R-phase proposed half bridge power cell

Fig.9 shows the five levels of three phase output voltage of the proposed phase shifted PWM Inverter. The switching frequency in this technique is usually kept constant. This control is based on the principle of comparing a triangular

carrier signal of desire switching frequency and is compared to the error of the controlled signal.

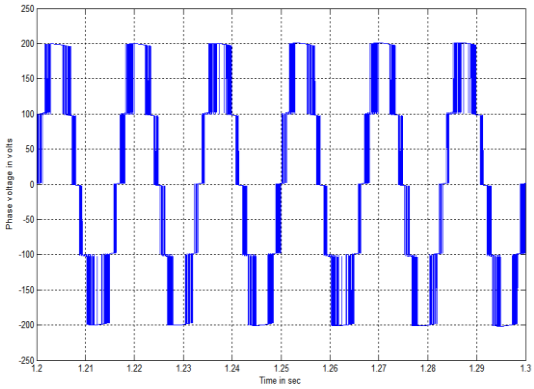

Fig. 7. Output of Five-level proposed MLI phase voltage

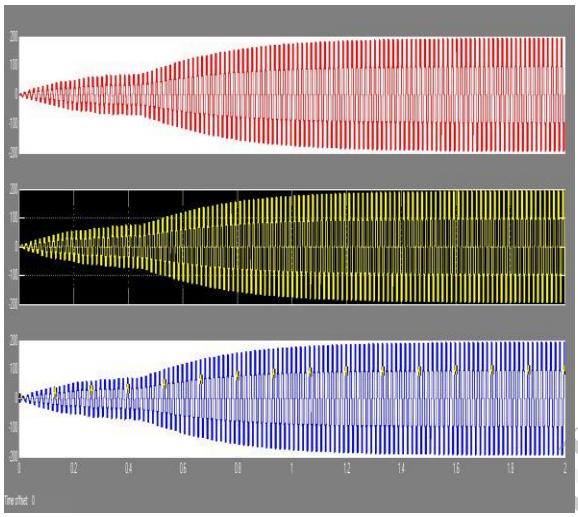

Fig. 8. Five level output voltages with phase shifted PWM Modulation technique

Stator current represented each phase is shown in Fig.10 The IGBT/DIODE currents can be obtained from the load current by multiplying with the corresponding duty cycles.

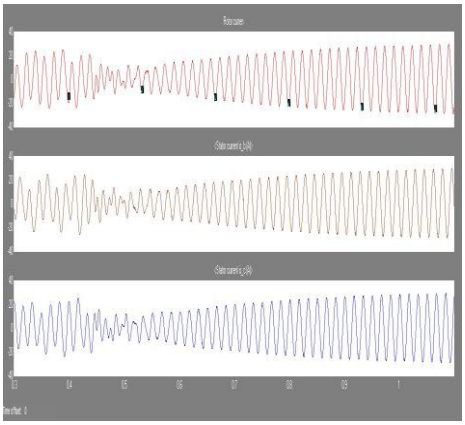

Fig. 9. Stator currents in three phases

The required capacitance for each cell depends on the allowable ripple voltage and the load current. The ripple current frequency is double the load current frequency.

Fig.11 and Fig.12 shows output speed and the generated torque of the 5-level proposed multilevel inverter fed PMSM drive with phase shifted PWM modulation technique. The behavior of the generated electromagnetic torque is also of vital importance. The peak, or maximum torque required for the application, can be calculated by summing the load torque (TL), torque due to inertia (TJ) and the torque required to overcome the friction (TF).

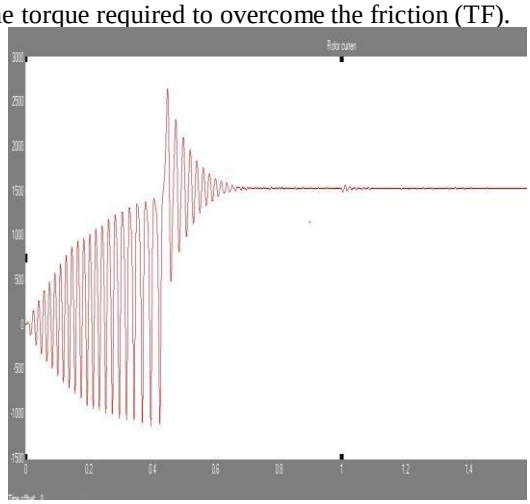

Fig. 10. Output rotor Speed for PMSM drive

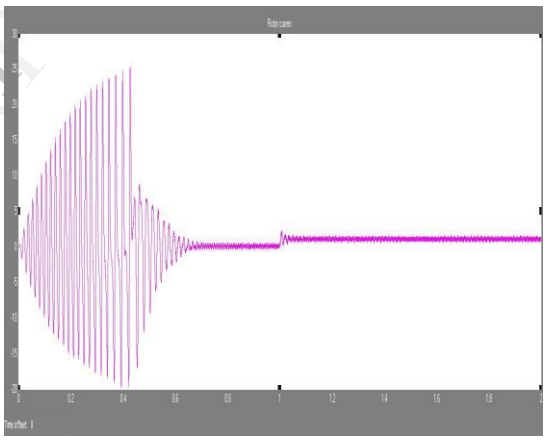

Fig. 11. Generated torque of the 5-level proposed multilevel inverter fed PMSM drive

V. COMPARISON BETWEEN PROPOSED MULTILEVEL INVERTER AND CHB MULTILEVEL INVERTER

The main difference between the proposed topology and a CHB inverter is the way how the inverter legs are connected. These two converters have the same number of switches on each power module, by this means; the voltage levels generated in the terminals of each power cell are the equivalent. In consequence the numbers of voltage levels of the phase-to-neutral voltage (VAN) and line to-line output voltage (VAB) will result in equal, as described in Table 1.Each power cell in the proposed topology employs double the number of isolated dc voltage sources, with half the power. The PWM phase-shifted multicarrier modulation technique used in the proposed topology is similar to that used in CHB multilevel inverters. Compare with cascaded multilevel Inverter our proposed multilevel inverter reduces

switch stress. In this half-Bridge connection half power is dissipated through the switch and the severity of explosion of power cell is reduced to half.

TABLE I. COMPARISON BETWEEN THE PROPOSED MULTILEVEL INVERTER TOPOLOGY AND CASCADED H-BRIDGE MULTILEVEL INVERTER

Topology	Proposed Inverter	CHB Inverter
Phase to neutral voltage levels	n_p	n_p
Line to line voltage levels	$2n_p$-1	$2n_p$-1
Number of power cells per phase	$(n_p$-1)/2	$(n_p$-1)/2
Number of switches per phase	$2(n_p$-1)	$2(n_p$-1)
Number of isolated DC voltage sources per phase	$(n_p$-1)	$(n_p$-1)/2
Load voltage THD	Similar	Similar
Modulation strategy	Similar	Similar
Power of each isolated DC voltage source	$P_{nominal}$ / $3(n_p$-1)	$2P_{nominal}$ / $3(n_p$-1)

VI. CONCLUSION

Cascaded H bridge Multilevel inverter topology is presented by using phase shifted multicarrier pulse width modulation technique. The PMSM drive is evaluated for the above topology for its steady state and dynamic performance. It shows satisfactory performance. A comparison is also made between the proposed topology and the CHB multilevel inverter was also presented, showing similar characteristics; thus, the topology described in this paper can be seen as an alternative to be applied in similar applications.The proposed topology using phase shift pulse width modulating technique is carried out for five level cascade Half- bridge inverter fed PMSM motor drive and the simulation results are presented for the performance of the motor. The results show that the dynamic performance of the motor is quite satisfactory. In this proposed topology input voltage is Vdc/2 means that half of power fritter away from it and is easy to reinstate that leg which is cost effective and it will also amplify the reliability of this topology. MATLAB/Simulink model is developed and simulation results are presented.

VII. FUTURE SCOPE

The levels of multilevel configuration can be increased and further improvements in terms of performance and power quality issues can be broadly studied and could be implemented with hardware circuits. The same cascaded multilevel inverter configuration can be installed for other applications like SVC system and performance can be studied for larger ac systems. The proposed system can be designed for larger electrical drives and parameters can be monitored and varied dynamically with high speed network interconnections. Hence the power quality problems in power distribution can be controlled or completely eliminated.

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