Performance Analysis of new low power Modified Feedthrough Logic (MFTL) Structure

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***Abstract*—In this paper a new modification of existing CMOS domino logic family called feedthrough logic for a low power and high performance dynamic circuit is presented. Faster circuits with low power dissipation can be designed with feedthrogh logic. The proposed circuit for low power improves dynamic power consumption as compared to the existing feedthrough logic. The proposed circuit is simulated using 0.18 µm, 1.8 V CMOS process technology in HSPICE environment. Intensive simulation shows that the proposed modified low-power structure reduces the dynamic power and improves speed considerably for 10-stage of inverters and 8-bit ripple carry adder in comparison to existing feedthrough logic. The concept is validated through extensive simulation. The disadvantages of domino logic like problem of requirement of output inverter and non-inverting logic are also completely eliminated in the proposed design.**

Keywords—Modified feedthrough Logic (MFTL), Low Power Modified feedthrough Logic (LP-MFTL), domino CMOS logic, Ripple Carry Adder(RCA).

I. INTRODUCTION

The concept of using FTL is now being researched due to its high speed over standard CMOS circuit [1]. It offers high performance operation for speed and power critical circuit like arithmetic or pipelining circuit [2]. The basic principle of FTL is domino logic [3] with an added feature of pre-evaluation of output before all input is valid, thus increasing the speed of a digital circuit. Moreover, FTL overcomes the shortcomings of domino logic like inability to provide non inverting logic, problem of charge sharing, monotonic nature of output and need of extra inverter at output, with reduced chip area [1],[2],[3].

FTL has numerous applications like direct cascading of dynamic CMOS, to produce differential output, to design iterative networks. This paper presents a new modified approach in FTL, called Modified feedthrough Logic (MFTL), that results in reduced delay and power consumption as compared to the existing design. This report is organized as follows: Section 2 briefly describe the principle of operation for FTL. In Section 3 modified FTL is presented, Section 4 provides analysis of modified FTL and FTL for inverter circuit and RCA. Section 5 gives a brief idea about the future work Finally, Section 6 gives conclusion.

II. PRINCIPLE OF CONVENTIONAL FTL

The basic structure of FTL is shown in Fig.1.

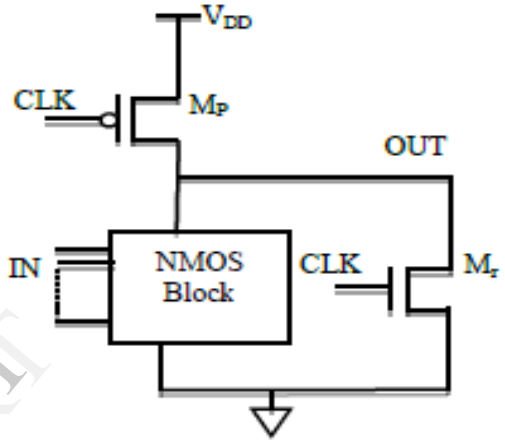


Fig.1 Basic structure of FTL[1]

It consist a NMOS reset transistor Mr for resetting the output node to low logic level, a pull up PMOS load transistor Mp and an NMOS block. Mp and Mr controlled by the clock signal CLK

The basic principle of operation of a FTL circuit was presented in [1] and is briefed here. During CLK=1, (reset phase) Mr turned on and the output node pulled to ground through Mr . Since the output node is pulled to ground during reset phase the need of inverter during cascading is eliminated. When CLK goes low (evaluation phase) Mr is turned off and the output node conditionally evaluates to logic high (V_{OH}) or low (V_{OL}) depending upon input to NMOS block. If the NMOS block evaluates to high then output node is pulled towards $V_{DD,}$ otherwise it remains at logic LOW.

A long chain of inverter designed by using FTL is shown in Fig.2. When CLK=1, all the output nodes are at logic zero. When CLK goes low (evaluation), the output node of the cascaded gate rises to the gate threshold voltage VTH as shown in Fig. 3.Now even a small variation in the input voltage causes a fast variation in voltage at the output node. When the inputs to the gates are valid then output node makes only a partial transition from V_{TH} to V_{OH} or V_{OL} [1].Hence delay decreases.

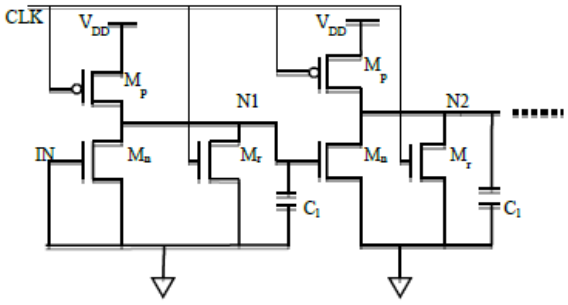


Fig.2 Transistor level diagram for FTL inverter chain[1]

A. Existing Low Power FTL (LP-FTL)

Power consumption reduction of CMOS integrated circuits with improved performance has been a topic of great interest and research in recent years. The different design techniques proposed for high performance trade power for performance. This is achieved through a mix of dynamic and static circuit styles [1]. For many high speed applications, speed improvement is achieved at the expense of power.

The existing low power FTL circuit is shown in Fig.4. This circuit reduces V_{OL} by using one additional PMOS transistor MP2 in series with MP1.During reset phase i.e. when CLK = 1, output node is pulled to ground (GND) through Mr[1]. During evaluation phase output node charges through Mp1 and Mp2 [1]. During evaluation phase Mr is turned off and the output node conditionally evaluates to logic high (V_{OH}) or low (V_{OL}) depending upon input to NMOS block. Since Mp1 and Mp2 are in series the voltage at drain of MP1 is less than VDD. During evaluation due to ratio logic the output node pulled to logic low voltage i.e. V_{OL} which is less than the V_{OL} of existing FTL [1].

This reduction in V_{OL} causes significant reduction in dynamic power consumption but due to the insertion of PMOS transistor Mp2 propagation delay of the LP-FTL increases [1].

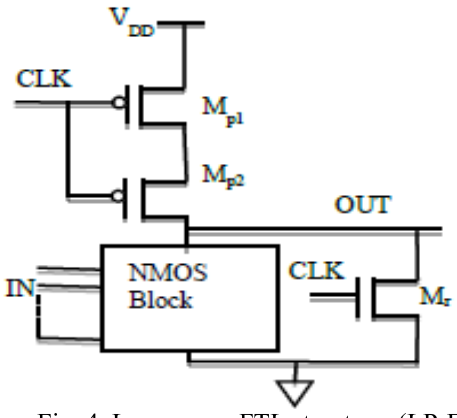


Fig..4 Low power FTL structure (LP-FTL) [1]

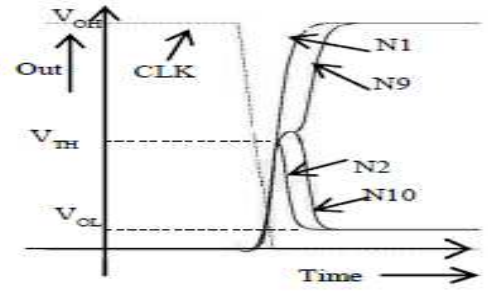


Fig.3 Output voltages of Inverter chain in FTL [1]

III. PROPOSED MODIFIED FTL (MFTL)

Figure 5. presents the modified FTL. MFTL is similar to the FTL with an additional NMOS transistor Ta in PDN. The gate of NMOS is driven by VDD as Vgs, keeping it always ON.

The principle of operation of modified FTL is as follows: During Clock = 1 (Reset), output is pulled to 'LOW' through reset transistor Tr. During Clock = 0(Evaluation), the output is generated according to the given set of inputs.

Here, additional transistor increases the dynamic resistance of the PDN, due to which the output node discharges up to V_{OL} value greater than the V_{OL} of existing FTL. This change in V_{OL} results for less high to low propagation delay from V_{TH} to V_{OL} or vice-versa. Also the increased value of V_{OL} causes a reduction in the dynamic power consumed by the circuit. The dynamic power consumption of a digital circuit is given by,

$$P_{dyn} = \alpha_s . C_{LOAD} . V_{DD} . V(x) . Fclkmax \quad (1)$$

Here, α_s is the switching factor, C_{LOAD} is the load capacitance, V_{DD} is supply voltage, Fclkmax is the maximum operating frequency and V(x) is the power delivered by the source during low to high transition. V(x) reduces due to increased value of V_{OL} in modified FTL. Therefore, MFTL has lower power consumption than in FTL.

A. Low power modified FTL (LP-MFTL)

Fig.6 shows the circuit diagram of LP-FTL. The operation of this circuit is similar to that of FTL in [1]. Low power proposed modified FTL (LP-MFTL), has an NMOS transistor Ta connected as shown in Fig 6. When clock goes 'HIGH', output is pulled to 'LOW' through reset transistor Tr. When clock goes 'LOW'; the output is generated according to the given set of inputs with additional transistor Ta always 'ON'. For LP-MFTL also due to the insertion of PMOS transistor TP2 propagation delay increases.

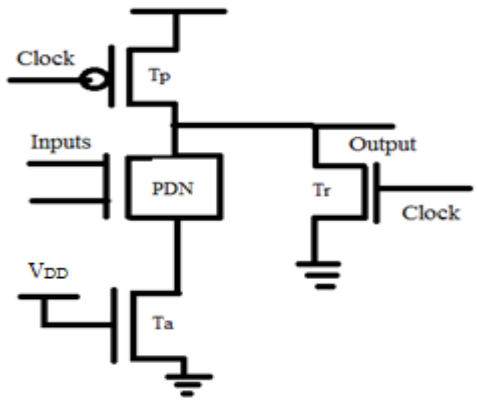
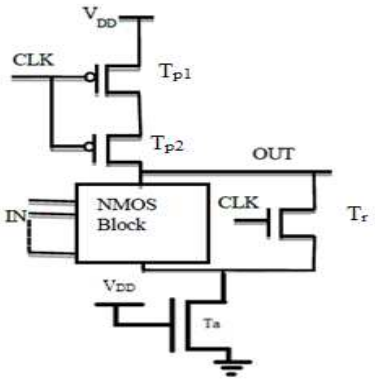


Fig.5. Modified FTL(MFTL)



. Fig.6. Low power Modified FTL(LP+MFTL)

IV. ANALYSIS DESCRIPTION AND RESULTS

A. Analysis of proposed MFTL inverter

The proposed MFTL structures' performance is verified against the existing FTL structure in [1] by designing 10 chain inverter at 0.18µm at 1.8V CMOS process technology model library from HSPICE at 1fF capacitance. Circuits are simulayted and power estimated using HSPICE environment.

Figures 7 and 8 shows the inverter stages using FTL[2] and proposed MFTL structures.

Table I shows the dynamic power, average values of propagation delays (t_p), and power delay product comparison of two proposed modified FTL and the existing FTL in [2] for a single stage inverter.

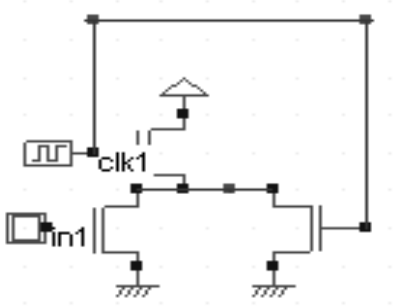


Fig.7. Circuit diagram of FTL single inverter

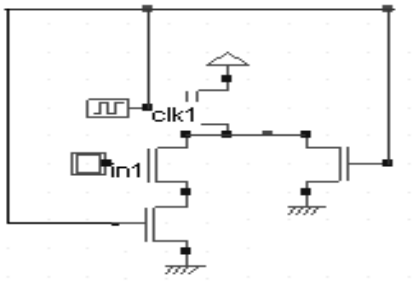


Fig. 8 Circuit diagram of MFTL single inverter.

Figures 9 and 10 shows the 10 chain inverter stages using FTL[2] and proposed MFTL structures.

Table II shows the dynamic power, average values of propagation delays (t_p), and power delay product comparison of two proposed modified FTL and the existing FTL in [2] for a 10 chain inverter.

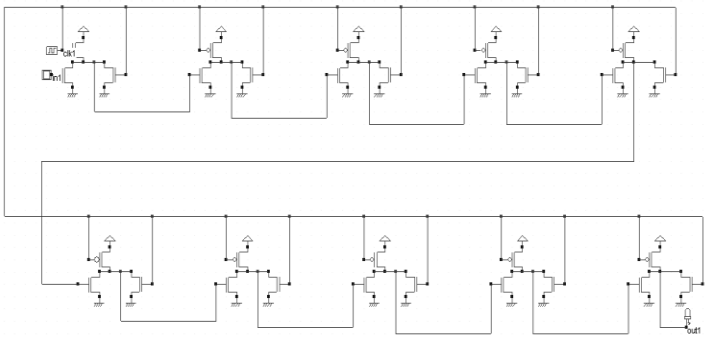


Fig. 9 Circuit diagram of FTL 10-inverter chain[1].

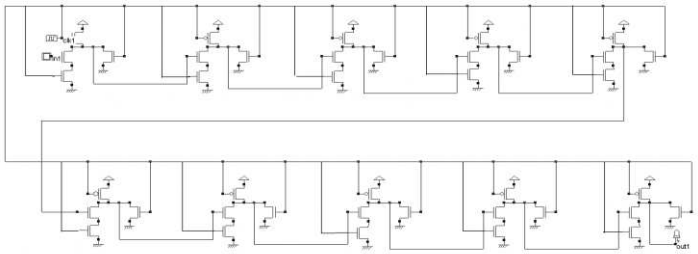


Fig. 10 Circuit diagram of MFTL 10-inverter chain

TABLE I. COMPARISON OF PDP FOR FTL, MFTL (SINGLE INVERTER)

Logic Family	Power(uW)	Delay (ps)	PDP(uW x ps) X 10^-16
FTL[1]	6.174	26.14	1.6
MFTL	5.931	25.83	1.5

B . RCA Design and Performace Analysis

It is possible to create a logical circuit using multiple full adders to add N-bit numbers. Each full adder inputs a Cin, which is the Cout of the previous adder. This kind of adder is called a ripple-carry adder, since each carry bit "ripples" to the next full adder. Note that the first (and only the first) full adder may be replaced by a half adder.

A full adder is designed by using the basic sum and carry cell shown in Figures 11and 12. Then the basic cells are designed by using proposed MFTL structure, as in Fig 13 and Fig 14.. These cells are used for the design of 8-bit ripple carry adder and compared with existing structure. Then modification is extended to the low power structure as in [1], as in Fig 15 and Fig 16.

All the 8-bit ripple carry adders designed by various structures are simulated and compared with existing FTL structures in 0.18µm CMOS process technology model library from HSPICE and power estimated using HSPICE. Power supply V_{DD} is constant for all simulations and is equal to 1.8V

Table III and Table IV shows the comparison of Power Delay Product (PDP) and AreaDelay Product (ADP) in FTL [1], MFTL,LP-FTL[1], LP-MFTL for 8 bit RCA.

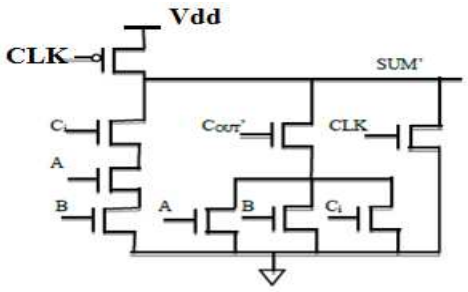


Fig.11.FTL Structure of Sum cell [1]

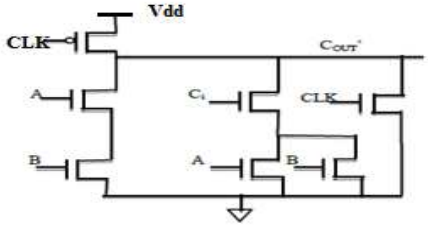


Fig.12.FTL Structure of Carry cell [1]

TABLE II. COMPARISON OF PDP FOR FTL, MFTL (10 CHAIN INVERTER)

Logic Family	Power(uW)	Delay (ns)	PDP(uW x ns) X 10^-13
FTL[1]	265.2	2.059	5.4
MFTL	214.8	2.055	4.41

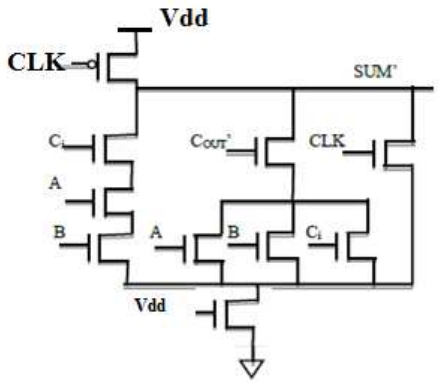


Fig.13. Structure of proposed MFTLSum cell

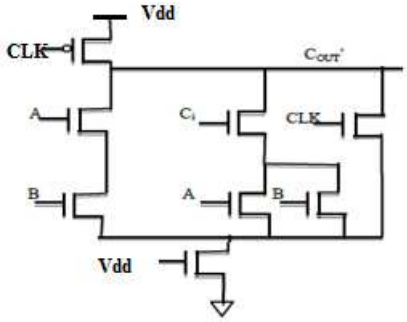


Fig.14. Structure of proposed MFTL Carry cell

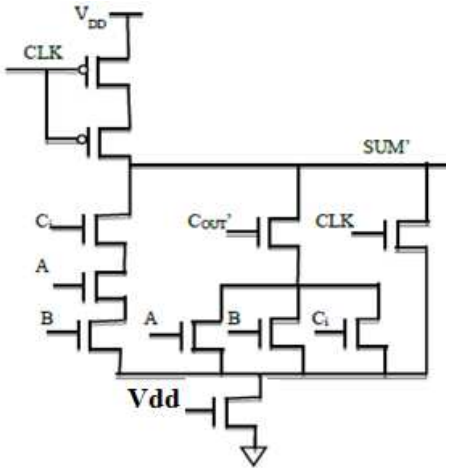


Fig.15. Structure of proposed LP_MFTLSum cell

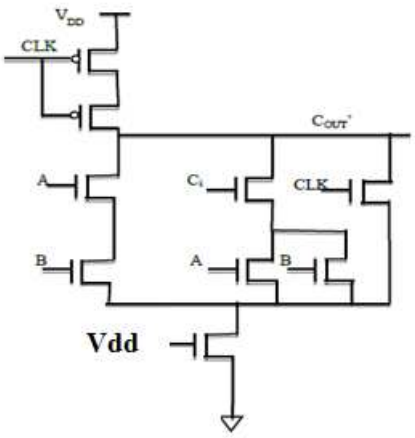


Fig.16. Structure of proposed LP_MFTL Carry cell

TABLE III. COMPARISON OF PDP IN FTL, MFTL, LP-FTL and LP-MFTL for 8 bit RCA

Logic family	Power(uW)	Delay(ns)	PDP(uW x ps) X 10^-12
FTL	560.3	2.062	1.15
MFTL	557.1	1.047	0.583
LP-FTL	267.6	3.011	0.805
LP-MFTL	209.3	1.089	0.227

TABLE VI . COMPARISON OF ADP IN FTL ,MFTL, LP-FT, LP-MFTL for 8 bit RCA (0.18 um)

Logic family	Delay(ps)	Count	ADP(um^2 x ps) X 10^-20
FTL	2.062	128	1.28
MFTL	1.047	144	0.73
LP-FTL	3.011	144	2.10
LP-MFTL	1.089	160	0.84

Analysis of power and delay under load capacitance from 10fF to 50 fF was done to obtain better results for the proposed MFTL structures. The change in power with load is small, while the delay changes in a more noticeable manner. This points to the serious fact of avoiding dissimilar capacitive loads. Figures 17 and 18 shows the resulting graphs.

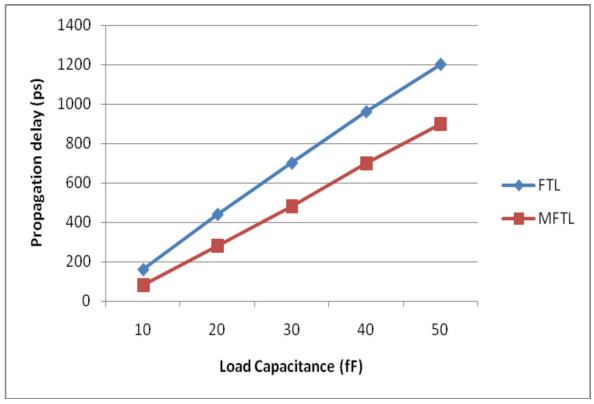


Fig. 17 Effect of capacitive loads on delay

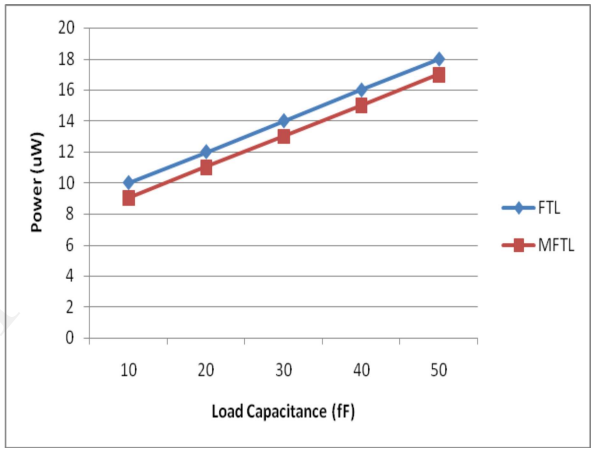


Fig. 18 Effect of capacitive loads on power

IV. FUTURE WORK

To extend the advantages of MFTL to higher levels of scaling by incorporating the work in nanometer scale through CNT [5] and to analyze t he performance. The behaviour of CNT with length and diameter is to be considered. A study of various parameters like mobility, conductance etc. of the CNT may also be done to analyze the performance not just through delay and power.. This main focus is on CNT based FET's, that are gaining interest as replacements for conventional CMOS, in many modern circuits and also new devices.

V. CONCLUSION

In this paper, is proposed a low power dynamic circuit. The proposed circuit is simulated in 0.18 µm CMOS process technology. In this era of high speed digital circuits, FTL gives advantage of having lower delay and smaller power consumption compared to any other logic families in literature. This paper presented a Modified FTL based on partial evaluation concept. According to the result in tables, MFTL is suitable for high speed arithmetic circuit design over FTL. MFTL also has lesser delay, reduced power

consumption and improved PDP. In terms of both PDP and ADP, the modified structures prove to hold an improved value than existing FTL structure. The simulation for a long chain of inverter (10-stage) and 8-bit ripple carry adder is also carried out in this work. Study on the effect of output load capacitance from 10 fF to 50fF on power and delay was also done The simulation result confirms that for a given load, the power delay product (PDP) and area delay product (ADP) of the proposed circuit is much better than that of existing FTL structure.

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