Performance Evaluation Of Strained Si/Sige N-Channel Mosfet

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ABSTRACT

Electronics, and in particular the integrated circuit has made possible the design of powerful and flexible processors which provide highly intelligent and adaptable devices for the user. Integrated circuit memories fabricated by using MOS (Metal-Oxide-Semiconductor) technology have provided the essential elements to complement these processors and, together with a wide range of logic and analog integrated circuitry. N MOS technology has an important role in IC fabrication. Works are going on to improve the performance of n MOSFETs. Device scaling which was a major driving force in the development of high density ICs is facing a number of obstacles, making it very difficult to sustain the trend of device performance improvements. Consequently, innovative device structures and materials are actively being investigated to boost performance. The tensile-strained-Si MOSFET is getting attention recently, as it significantly enhances the inversion layer electron mobility and hence the performance of deep submicron MOSFETs for high speed operations. One of the suggestions from researcher was to develop a strained SiGe channel structure grown on a normal Si substrate. These SiGe-channel MOSFET's show some significantly better electrical characteristics as compared to the silicon-channel MOSFET's. In this performance of a strained Si/SiGe n-Channel MOSFET has been studied on the basis of ORCAD simulations. Parameters needed for the simulations were first obtained on the basis of analytical model. Physics based 2-D model for the surface potential variation along the channel in an n-channel SiGe MOSFET's is developed by solving the two-dimensional Poisson's equation. It is simple in its functional form and lends itself to efficient computation. Concept of strained silicon and effects due to germanium concentration in device parameters are also studied in this work Strained Si/SiGe n-channel MOSFET has tremendous applications in biomedical field. The modern communication world is also taking interest to use strained Si/SiGe n-channel MOSFET in its applications because of high speed of operation

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INTRODUCTION

Electronics is characterized by reliability, low power dissipation, extremely low weight and volume, and low cost, coupled with an ability to cope easily with a high degree of sophistication and complexity. Electronics, and in particular the integrated circuit has made possible the design of powerful and flexible processors which provide highly intelligent and adaptable devices for the user. Integrated circuit memories fabricated by using MOS (Metal-Oxide-Semiconductor) technology have provided the essential elements to complement these processors and, together with a wide range of logic and analog integrated circuitry. Within the bounds of MOS technology the possible circuit realizations may be based on p-MOS, n-MOS and BiCMOS devices. Although CMOS is the dominant technology, but emphasis is given to nMOS technology. The reasons for this are as follows slightly less than the dielectric constant εr of the substrate because the fringing fields from the patch to the ground plane are not confined in the dielectric only, but are also spread in the air.

If the design of nMOS technology is to be carried out effectively or the performance of circuits based on it is to be understood than one must have a sound knowledge of MOS active device. For the performance improvement of n-MOS device, since last 3 decades scaling has been the primary means. However, device scaling is facing a number of obstacles, making it very difficult to sustain the trend of device performance improvements. Consequently, innovative device structures and materials are actively being investigated to boost performance [1], [2]. The tensile-strained-Si MOSFET is getting attention recently, as it significantly enhances the inversion layer electron mobility and hence the performance of deep submicron MOSFETs for high speed operations. One of the suggestions from researcher was to develop a strained SiGe channel structure grown on a normal Si substrate [3], [4]. A SiGe layer of several nm thick provides the big advantage that only a small change from the standard fabrication process is needed for electron mobility enhancement. High-speed devices require a large charging current that is now obtained by increasing their carrier mobility with the introduction of SiGe layer.

CONCEPT OF STRAINED SILICON

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The tensile-strained-Si MOSFET is getting attention recently, as it significantly enhances the inversion layer electron mobility and hence the performance of deep submicron MOSFETs. The strained-Si MOSFETs exhibit a shifted threshold voltage from conventional Si devices, due to the band offset at the heterojunction between the strained-Si and SiGe layers. The strain of Si is obtained from a Si layer grown epitaxially on a relaxed Si Ge layer. A chemical mechanical polishing (CMP) step is introduced in the middle of SiGe epitaxy to reduce the surface roughness. Overall thermal budget and etch steps can be controlled tightly to minimize strain relaxation, Ge out-diffusion, and strained-Si consumption [37]. Relaxed $Si_{1-x}Ge_x$ graded buffers can be used as a template for epitaxially growing Si in a state of biaxial tensile strain and *n*-type MOSFETs fabricated on strained-silicon $(\varepsilon - Si)$ demonstrate higher effective mobility than those on Czochralski-grown Si (Cz-Si) [49]. Even in devices with high channel doping and short gate lengths, the strain-induced electron mobility enhancement leads directly to increased drive currents. Figure shows the impact of Ge in the lattice of silicon when SiGe layer is formed.

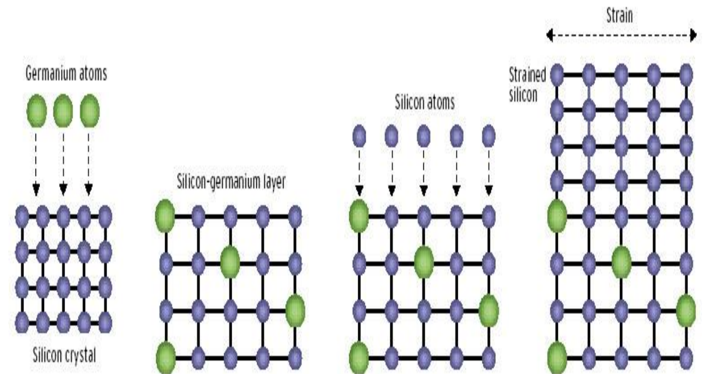

Figure : *(a) Ge is introduced into the lattice (b) Si is deposited on top of the SiGe. Atoms align causing a strain in the lattice.*

ANALYSIS AND DESIGN

MATHEMATICAL FORMULATION FOR SURFACE POTENTIAL

As $\psi(x,y)=\psi_i(x,y)-\psi_i(x=\infty)$ is defined as the intrinsic potential at a point (x,y) with respect to the intrinsic potential of the p-type substrate [46].The substrate is assumed to be uniformly doped with a concentration Na .

In the oxide region AFGH, Poisson's equation becomes a homogeneous (Laplace) equation,

$$\frac{\partial^2\psi}{\partial x^2} + \frac{\partial^2\psi}{\partial y^2} = 0 \qquad (1)$$

In the depletion region in silicon, the concentrations of both types of mobile carriers are negligible under subthreshold conditions.

Therefore, in ABEF, Poissin's equation is approximated by-

$$\frac{\partial^2\psi}{\partial x^2} + \frac{\partial^2\psi}{\partial y^2} = \frac{qN_a}{\varepsilon_{SiGe}} \qquad (2)$$

The length of the SiGe region is equal to the channel length L. the depth is given by the depletion layer width, W_d, to be determined later.As the normal component of the electric field changes by a factor of $\varepsilon_{SiGe}/\varepsilon_{ox} \approx 3$ across the silicon-oxide boundary AF [46]. To eliminate this boundary condition so that ψ and its derivatives are continuous, the oxide is replaced by an equivalent region of the same dielectric constant as SiGe, but with the thickness equal to $3t_{ox}$. This preserves the capacitance and allows the entire rectangular region to be treated as a homogeneous material of dielectric constant ε_{SiGe}. The drawback is that it may cause some error in tangential field, whose magnitude does not change across the silicon-oxide boundary. In the equivalent structure, the tangential field apparently experiences a thicker-than-actual oxide. The errors are expected to be smaller when the gate oxide is thin compared to the silicon depletion depth W_d so that the oxide field is dominated by its normal component.

If the source and drain junctions are abrupt and deeper than W_d, the set of simplified boundary conditions will be as follows:

$$\psi(-3t_{ox}, y) = V_g - V_{fb}$$

along GH.

$$\psi(x,0) = \psi_{bi}$$

along AB. (3)

$$\psi(x,L) = \psi_{bi}$$

along EF. (4)

$$\psi(W_d, y) = 0$$

along CD. (5)

Where V_g and V_{ds} are the gate and source-drain voltages. V_{fb} is the flat-band voltage of the gate electrode, and ψ_{bi} is the built-in potential of the source- or drain-to-substrate junction. For an abrupt n^+-p junction, $\psi_{bi} = E_g/2q + \psi_B$,

where $\psi_B = \frac{KT}{q}\ln\left(\frac{N_a}{N_i}\right)$.

The bottom boundary is movable one, as W_d will change with the gate voltage V_g. The distance BC is approximately given by the source junction depletion width,

$$\text{Ws} = \sqrt{\frac{2\varepsilon_{siGe}\psi_{bi}}{qN_a}} \qquad (6)$$

Similarly, DE is given by the drain junction depletion width,

$$W_D = \sqrt{\frac{2\varepsilon_{siGe}(\psi_{bi} + V_{ds})}{qN_a}} \qquad (7)$$

The boundary conditions along FG and HA are assumed to very linearly between the end point values, while those along BC and BE are assumed to vary parabolically between the end points.The surface potential solution technique makes use of the superposition principle and breaks the electrostatic potential into the following terms.Here $v(x, y)$ is a solution to the inhomogeneous (Poisson's) equation and satisfies the top boundary condition, Equation (4.3). u_L, u_R, u_B are solutions to homogeneous (Laplace) equation, and are chosen in order for $\psi(x, y)$ to satisfy the rest of the boundary condition namely, on the left, the right, and the

A natural choice for $v(x, y)$ is approximated as:

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$$v(x,y)=\psi_S^{\circ}-\frac{V_g-V_{fb}-\psi_S^{\circ}}{3t_{ox}} \quad (8)$$

for the oxide region, $-3t_{ox}\le x\le 0,$

and

$$v(x,y)=\psi_S^{\circ}\left(1-\sqrt{\frac{qNa}{2\varepsilon_{SiGe}\psi_S^{\circ}}}x\right)^2 \quad (9)$$

for the Channel region, $0\le x\le W_d$.

Here long channel surface potential ψ_S° is related to V_g by the requirement that $\partial v/\partial x$ be continuous at $x=0$:

$$\frac{V_g-V_{fb}-\psi_S^{\circ}}{3t_{ox}}=\sqrt{\frac{2qNa\,\psi_S^{\circ}}{\varepsilon_{siGe}}} \quad (10)$$

v and $\partial v/\partial x$ are zero at $x=W_d^{\circ}$ is the long-channel depletion width given by

$$W_d^{\circ}=\sqrt{\frac{2\varepsilon_{siGe}\psi_S^{\circ}}{qNa}} \quad (11)$$

The third series, u_B, however, cannot be treated similarly, since exp$\left[-n\pi(W_d+3t_{ox})/L\right]$ decreases much more slowly with n. fortunately, the coefficients d_n^* are at least an order of magnitude less than b_1^* and c_1^* combined. The entire u_B series can therefore be neglected altogether.

This point corresponds to the point of maximum barrier height. It is close to the mid point of the channel when the drain voltage is low. When the drain voltage is high, the point of highest barrier moves closer to the source.

So the threshold voltage of device can be calculated by the following relation

$$V_{th}=V_{fb}+2\psi_{bi}+\frac{t_{ox}\varepsilon_{SiGe}}{\varepsilon_{ox}}\left.\frac{\partial\psi}{\partial x}\right|_{x=0,y=y_c}$$

SIMULATION

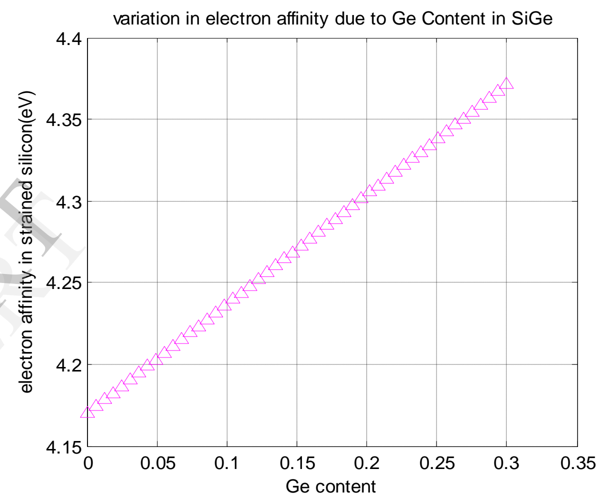

Figure : *Electron affinity in strained silicon Vs. Germanium content in SiGe alloy.*

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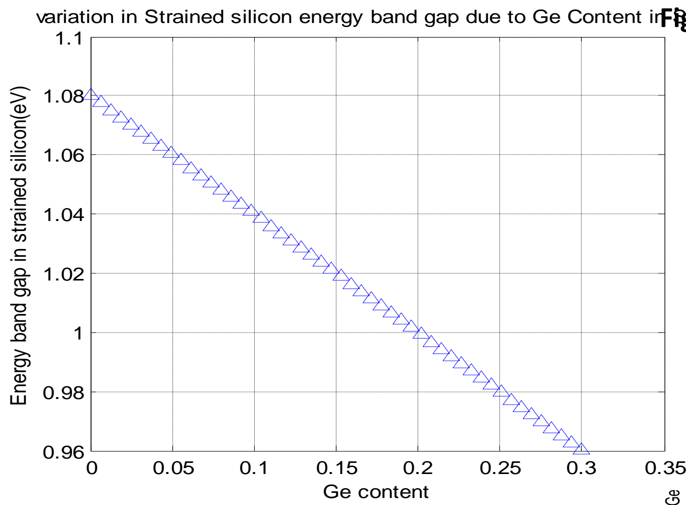

Figure : *Energy band Gap in strained Silicon Vs. Ge content*

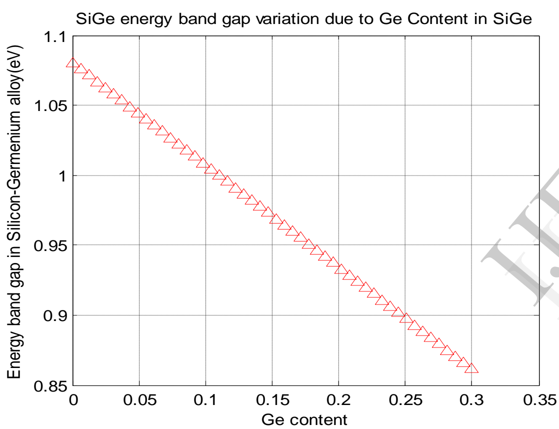

Figure : *Energy Band Gap in silicon-Germanium alloy Vs. Ge Content*

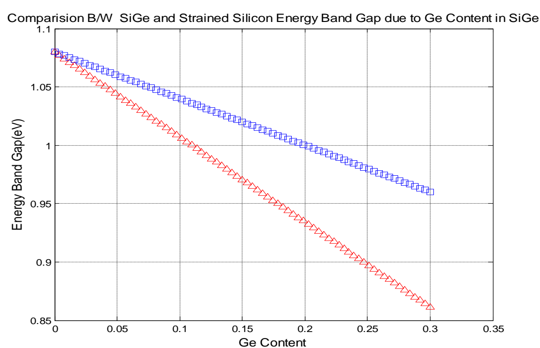

Figure : *Comparison between energy band gaps for strained silicon and SiGe alloy.*

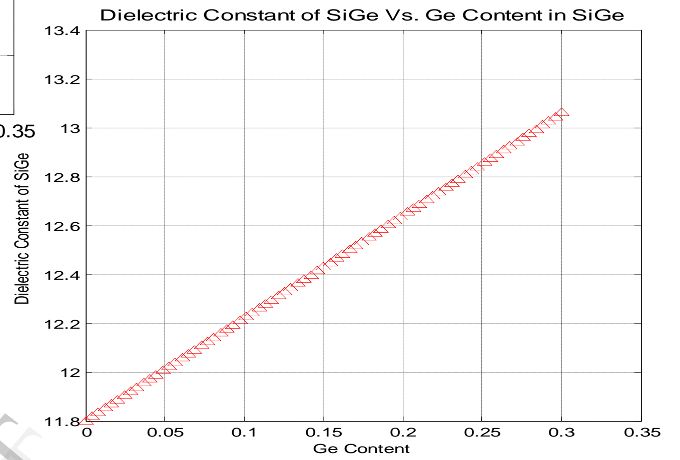

Figure : *Dielectric Constant of SiGe alloy Vs. Ge Content*

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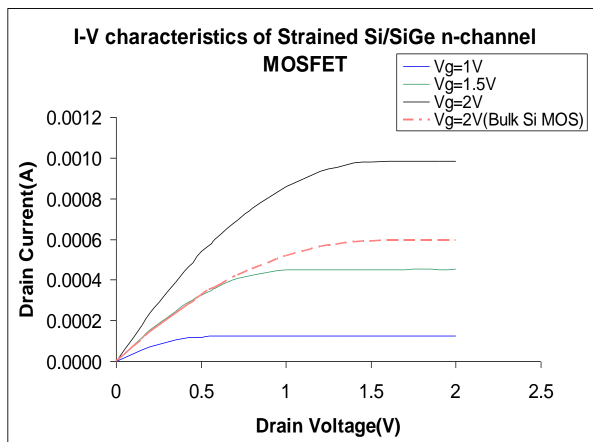

Figure : *I-V Characteristic of a 0.25µm strained Si/SiGe n-channel MOSFET. The device width is 9.5µm.*

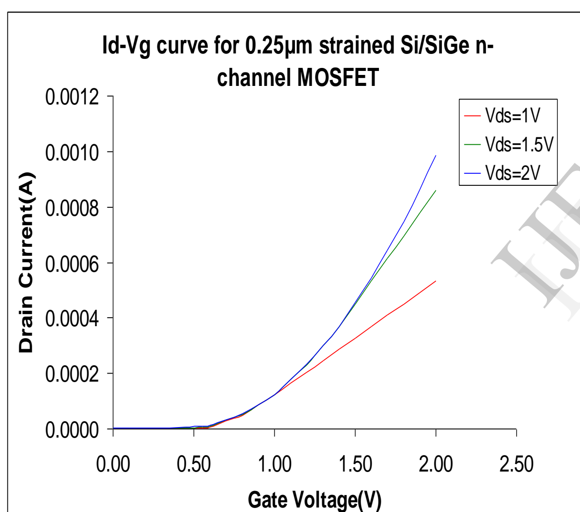

Figure : *I_d-V_g curve for 0.25µm strained Si/SiGe n-channel MOSFET. The device width is 9.5µm.*

CONCLUSION

The work presented here shows the performance of a 0.25µm strained Si/SiGe n-channel MOSFET. In this work, the behavior of MOSFET is observed with the help of OrCAD simulation software. The effect of Ge concentration in strained Si/SiGe channel is seen. SiGe band gap is affected more by Ge introduction in SiGe compared to that of strained silicon band gap. Strain generated in channel increases the mobility of electrons in MOSFET that enables that device to be used for high speed operation and due to low threshold voltage it also takes less power for their operation. Hence one can say that this strained Si/SiGe n-channel MOSFET can have tremendous applications in modern communication equipment and biomedical field.

The present work can be extended to a device with different doping profile concentrations. The speed of operation can be enhanced by use of other combination of alloy in the channel. Hence one can analyze the current behavior of the device with different alloy combinations. Analytical model for obtaining current can also be done to validate the simulated results. Performance of a device with high dielectric constants may also be evaluated by using this model.

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REFERENCES

[1] Y. Taur, “CMOS design near the limit of scaling,” IBM J. Res. Develop., vol. 46, no. 2/3, pp. 213–222, Mar./May 2002.

[2] E. J. Nowak, “Maintaining the benefits of CMOS scaling when scaling bogs down,” IBM J. Res. Develop., vol. 46, no. 2/3, pp. 169–180, Mar./May 2002.

[3] F. Schaffler et al.: High-mobility Si and Ge structures. Semicond. Sci. Technol, 12, p.1515-1549, 1997.

[4] Y. Yeo et al.: Enhanced Performance in Sub- 100nm MOSFETs Using Strained Epitaxial Silicon-Germanium. International Electron Devices Meeting Technical Digest, p.753-756, 2000.

[5] M. J. Palmer et al.: Effective mobilities in pseudomorphic Si/SiGe/Si p-channel metaloxide- semiconductor field-effect transistors with thin silicon capping layers. *Applied Physics Letters*, **78**, p.1424-1426, 2001.

[6] F. Wanlass and C. T. Sah, "Nanowatt logic using field-effect metal-oxide-semiconductor triodes", Technical Digest of the Int. Solid-State Circuit Conf., IEEE, pp. 32-33, 1963.

[7] E. A. Fitzgerald, Y.-H. Xie, D. Monroe, P. J. Silverman, J. M. Kuo, A. R. Kortan, F. A. Thiel, and B. E. Weir, J. Vac. Sci. Technol. B 10, 1807, 1992.

[8] M. T. Currie, C. W. Leitz, T. A. Langdo, G. Taraschi, D. A. Antoniadis, and E. A. Fitzgerald, J. Vac. Sci. Technol. B 19, 2268, 2001.

[9] K. Rim, J. Welser, J. L. Hoyt, and J. F. Gibbons, Tech. Dig. - Int. Electron Devices Meet. 1995, 517.

[10] D.J. Frank, R.H. Dennard, E. Nowak, P.M. Solomon, Y. Taur, and H.-S.P. Wong, "device scaling limits of Si MOSFETs and their application dependencies", Proc. IEEE 89, pp. 259-288, 2001.

[11] E.J. Nowak, "Maintaining the benefits of CMOS scaling when scaling bogs down", IBM J. Res. Develop. 46, pp. 169-180, 2002.

[12] F. Wanlass and C. T. Sah, "Nanowatt logic using field-effect metal-oxide-semiconductor triodes", Technical Digest of the Int. Solid-State Circuit Conf., IEEE, pp. 32-33, 1963.

[13] R. Dennard, F. Gaensslen, H. Yu, V. Rideout, E. Bassous, and A. LeBlanc, "Design of Ion-Implanted MOSFET's with Very Small Physical Dimensions", IEEE J. Solid-State Circuits SC-9, pp. 256–268, 1974.

[14] Hasan M.Nayfeh, Judy L Hoyt, and Dimitri A. Antoniadis, IEEE Transactions on Electron Devices,VOL.51,NO.12, DECEMBER2004.

[15] T. E. Whall and E. H. C. Parker, "SiGe heterostructures for CMOS technology", Thin Solid Films 367 250-259, 2000.

[16] J. G. Fossum and W.Zhang, "Performance projections of scaled CMOS devices and circuits with strained Si-on-SiGe channels," IEEE Trans. Electron Devices, vol. 50, no. 4, pp. 1042–1049, Apr. 2003.

[17] Q. Xiang et al., "Strained siliconNMOS with nickel-silicide metal gate," in Symp. VLSI Tech. Dig., Jun. 2003, pp. 101–102.

[18] J.Goo et al., "Scalability of strained-Si nMOSFETs down to 25 nm gate length," IEEE Electron Device Lett., vol. 24, pp. 351–353, May 2003.

[19] D. J. Paul, Silicon Germanium Heterostructures in Electronics:- The Present and the Future, Thin Solid Films 321 172-180 (1998).

[20] G. Abstreiter, Electronic Properties of Si/SiGe/Ge Heterostructures, Physica Scripta, T68, 61-71 (1996).

[21] K. Ismail, M. Arafa, K. L. Saenger, J. O. Chu and B. S. Meyerson, " Extremely high electron mobility in Si/SiGe modulation-doped heterostructures", Applied Physics Letters 66 (9) 1077-1079 (1995)

[22] K. Rim et al., "Characteristics and device design of sub-100 nm strained Si N- and PMOSFETs," in Symp. VLSI Tech. Dig., Jun. 2002, pp. 98–99.

[23] Q. Xiang et al., "Strained siliconNMOS with nickel-silicide metal gate," in Symp. VLSI Tech. Dig., Jun. 2003, pp. 101–102.

[24] P.C. Yeh and J.G.Fossum, IEEE Trans. ED, vol. 42, 1995, p. 1605.

[25] D.Suh and J.G.Fossum, IEEE Trans. ED, vol. 42, p. 729

IJERT

[26] T.C.Hsiao, and J.C.S.Woo, IEEE Trans. ED, vol. 42, p. 1120.

[27] S.Biesemens, K. De Meyer, in Extended Abstracts of SSDM, 1994, p. 892.

[28] S.Pidin and M.Koyanagi, Japanese Journal of Applied Physics, Vol. 36, Part 1, No. 3B, March 1997, p.1497.

[29] J.Welser, J. L. Hoyt, and J. F. Gibbons, "Electron mobility enhancement in strained-Si n type metal-oxide-semiconductor field-effect transistors," IEEE Electron Device Lett., vol. 15, pp. 100–102, Mar. 1994.

[30] A.Das Gupta and S. K. Lahiri,"A Two-Dimensional analytical model of threshold voltages of short-channel MOSFET's with Gaussian-Doped channels," IEEE Transactions on Electron Devices, VOL. 35, NO. 3. March 1988.

[31] Tina Mangla, Amit Sehgal, Mridula Gupta, and R. S. Gupta, "Modeling Aspects of Sub-100-nm MOSFETs for ULSI-Device Applications," IEEE Transactions on Electron Devices, VOL. 54, NO. 1, January 2007.

[32] S. D. Cho, H. T. Kim, S. J. Song, S. S. Chi, M. S. Kim, W. S. Chang, H. J. Kang, H. T. Shin, T. E. Kim, D. J. Kim and D. M. Kim, "A Physics-Based Continuous Charge-Sheet MOSFET Model Using a Balanced Bulk-Charge-Sharing Method," Journal of the Korean Physical Society, Vol. 42, No. 2, February 2003, pp. 214-223.

[33] D. R. Poole and D. L. Kwong, "Two-dimensional analytical modeling of threshold voltages of short-channel MOSFET's," IEEE Electron Device Lett., vol. EDL-5, pp. 443-446, 1984.

[34] C. Y. Wu, S. Y. Yang, H. H. Chen, F. C. Tseng, and C. T. Shih, "An analytic and accurate model for the threshold voltage of short channel MOSFETs in VLSI," Solid-State Electron., vol. 27, pp. 651- 658, 1984.

[35] K. N. Ratna kumar and J. D. Meindl, "Short-channel MOST threshold voltage model," IEEE J. Solid-state Circuits, vol. SC-17, pp. 937-947, 1982.

[36] K. Rim, J. L. Hoyt, and J. F. Gibbons, "Fabrication and analysis of deep submicron strained-Si n-MOSFETs," IEEE Trans. Electron Devices, vol. 47, pp. 1406–1415, July 2000.

[37] J.-S. Goo, Q. Xiang, Y. Takamura, F. Arasnia, E. N. Paton, P. Besser, J. Pan, and M.-R. Lin, "Band offset induced threshold voltage in strained-Si n-MOSFETs," IEEE Electron Device Lett., vol. 24, pp. 568–570, Sept. 2003.

[38] Y.Taur and, T.Ning, "Fundamentals of modern VLSI Devices," Cambridge Uni - versity Press, 1998.

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