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Phase Locked Loop for synchronization of Inverter with Electrical grid: A Survey

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Abstract **- In order to meet the requirements for grid interconnection, it is necessary that the control of Distributed Power Generation systems (DPGSs) should be improved. Therefore, grid synchronization algorithms play a vital role for Distributed Power Generation Systems (DPGSs). This paper discusses one of the synchronization strategies that use Phase Locked Loop (PLL) and its various types for synchronization of the grid - side converter. Different PLL implementation structures and their major characteristics are pointed out. The primary application of the proposed synchronization method is for the distributed generation units with renewable energy sources, which utilize power electronic converters as an integral part of their systems. The synchronization is usually carried out with respect to the voltage, frequency and phase angle of voltage (or current) signal(s) of the utility system.**

Index Terms- **Microgrid, Distributed Power System; Inverter; PLL strategies; Amplitude, frequency and phase control.**

I.INTRODUCTION

A Microgrid consists of multiple distributed generators (DGs), renewable energy sources, conventional energy generators and energy storage systems those which provide both electric power and thermal energy as shown in figure.1. Typically, a Microgrid operates in parallel with the main grid. Microgrid may be operating in an islanded mode or in a standalone state. Islanded distributed generators (DGs) in a microgrid can change its operational mode to grid connected operation by synchronization with the main grid i.e. reconnection to the grid. A Microgrid or a portion of the power grid can be isolated from grid. However, the synchronization of microgrids that operate with multiple distributed generators (DGs) and loads cannot be controlled by a traditional synchronizer. It is necessary to control multiple distributed generators and energy storage systems in a coordinated way for the microgrid synchronization. Power converter system can be operated in islanded or standalone mode. In ideal condition, the output voltage parameters like amplitude, frequency and phase cannot be controlled for a grid together where multiple DGs are working in parallel; whereas the same parameters for standalone inverter to be connected to grid can be controlled by means of the various control strategies [1].

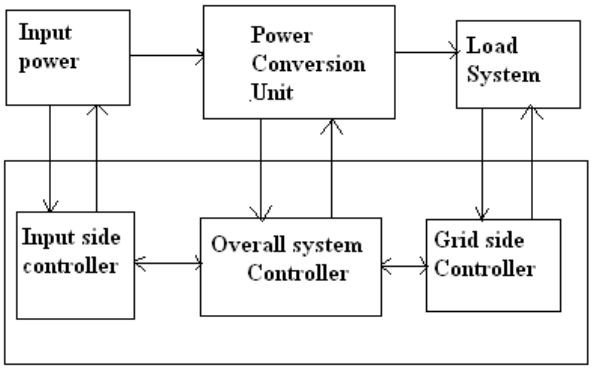

Figure.1.General structure of distributed power system [1]

The Inverter which working in standalone mode and is ready for synchronization to go for grid connected mode, has to closely track the grid frequency [2]. Normally grid frequency is varying according to load variations [3]. Any mismatch on frequency may lead to generate unwanted circulating currents and may lead to damage electronic devices. In this regard use of PLL is widely preferred technique that enables tracking the grid frequency [4].

Various techniques of synchronization of the inverter based on the Phase Locked Loop (PLL) are described in the second section named Methodology. Different issues and solutions related to different PLL methods are also described in it.

II.METHODOLOGY

In this section, the various techniques of Phase Locked Loop (PLL) for synchronization of the different parameters of inverter with electrical grid are discussed.

A. Phase Locked Loop (PLL)

A Phase Locked Loop (PLL) is an electronic circuit with a voltage or current driven oscillator that is constantly adjusted to match in phase with the (and thus lock on) the frequency of an input signal. The PLL is used in various applications of electrical technology as a fundamental concept [5]. The block diagram of conventional PLL is shown in figure.2.

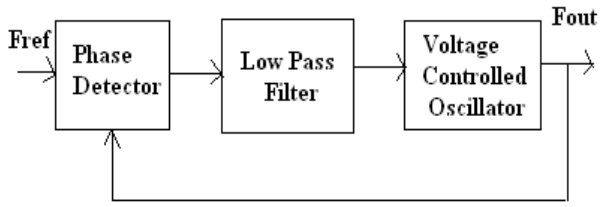

Figure.2.Phase Locked Loop Structure [8]

The basic idea of phase locking is to evaluate the difference between phase angle of the input signal and generated output signal [6]. The phase difference is usually estimated by a phase detector (which is usually a multiplier or comparator), Voltage-Controlled Oscillator (VCO) and loop controller or a Loop Pass Filter (LPF). The phase angle difference between of the input signal and output signal is measured by the Phase Detector and also provides a proper error signal. To generate the output signal, the LPF output signal drives the Voltage-Controlled Oscillator (VCO). The VCO provides a measure of variations of the phase and generates a signal whose frequency is equal to its input signal [7]. The deviation of the error signal from zero is because of any change in the phase angle (or frequency) of the input signal [8].

In order to utilize renewable energy such as wind and solar energy, three-phase grid-tied inverters are widely installed in micro-grids. Using impedance based method; the stability issue caused by grid-tied inverters can be studied. The output impedance of the grid-tied inverter modelled as shown in Figure.3.Phase-Locked Loop (PLL) control subsystem tracks the grid's frequency and phase angle. Hence, accurate and fast-responding PLL's for controlling of parameters are required. Ripple noise appearing in the estimated frequency is reduced or eliminated without the use of low-pass filters [6].

Although error signal is finely filtered by the LPF, still its nonlinear function of the phase difference for PD as multiplier. The VCO locks the generated output signal with the phase angle of input signal. It is necessary to estimate the derivative of the phase angle of the input signal for VCO [7].

However, Control loop may not be properly tracked due to large and abrupt variations of phase and frequency of the input signal. It may possible that the PLL cannot track the input signal at all due to PLL output signal can contain jitter. Although similarity in the concept of the PLL and adaptive notch filter (ANF), the PLL actively generates its output signal where the ANF passively extracts it from the input signal. By using either an analog or a digital phase-locked loop (PLL), realization of phase synchronization is possible. The PLL may be unsatisfactory because of corrupted input signal with strong disturbances. To overcome such difficulties, synchronization method based on a multirate PLL can be used. Disturbances like Noise, distortions, and frequency variations increases the complexity of phase locking [7]-[16].

B. Enhanced Phase Locked Loop (EPLL)

An Enhanced Phase-Locked Loop (EPLL) system is based on a nonlinear dynamic system. The block diagram of the EPLL is shown in Figure.3. It consists of three functional blocks such as Phase Detector (PD), Loop Filter (LF), and Voltage-Controlled Oscillator (VCO) are identified distinctly. In figure.3; EPLL receives input signal u(t), simultaneously it provides harmonic signal e(t), corresponding amplitude A(t), fundamental component y(t), phase component and frequency component. The EPLL maintains structural simplicity provides five fundamental signal attributes as mentioned above and also it exhibits a high degree of robustness due to the uncertainties external disturbances and noise also in its internal setting. This method provides higher degree of immunity and insensitivity to harmonics, noise and other types of pollutions as compared to existing synchronization method [8]-[20].

When the centre frequency of the base signal varies, its frequency adaptively permits satisfactory operation. This method of synchronization is also capable of coping with the unbalanced system scenarios. Structural simplicity greatly simplifies its implementation in digital software and/or hardware environments as an integral part of a digital control platform for power electronic converters. Distributed generation units, e.g., wind generation systems is primary application of EPLL which utilize power electronic converters as an integral part of their systems [17]-[19].

There are two categories of synchronization methods such as closed loop & open loop method. The EPLL is capable of providing an on-line estimate of the fundamental component of the input signal while following its variations in amplitude, phase, and frequency. Closed loop synchronization method again divided into four filter processing methods such as LPF (Low Pass Filter) based, SVF (Space Vector Filter) based and Extended Kalman Filter (EKF)-Based, Weighted Least-Squares Estimation (WLSE) based method. Closed loop method follows two methods Synchronization Based on Three-Phase PLL, Extended Three-Phase PLL-Based Method. EPLL provides an output signal whose phase is locked to that of the fundamental component of the input signal and the output signal is also locked to the fundamental component of the input signal in its amplitude and frequency. In addition EPLL also provides an on-line estimate of the basic parameters such as amplitude, phase and frequency. It also provides the 90-degree phase-shifted version of the fundamental component. It directly estimates the phase angle of the fundamental component of its input. The EPLL synchronization method not only detect the phase of the utility signal as fast as possible but also adequately eliminating the impacts of corrupting sources on the signal.Figure.4.shows the phase detection technique using EPLL [18].

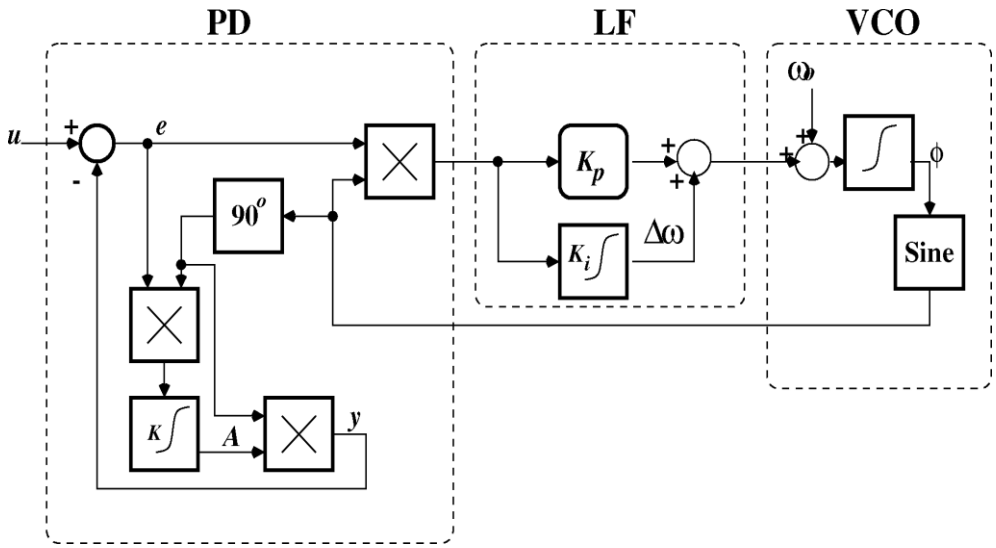

Figure.3. Block Diagram of EPLL [8]

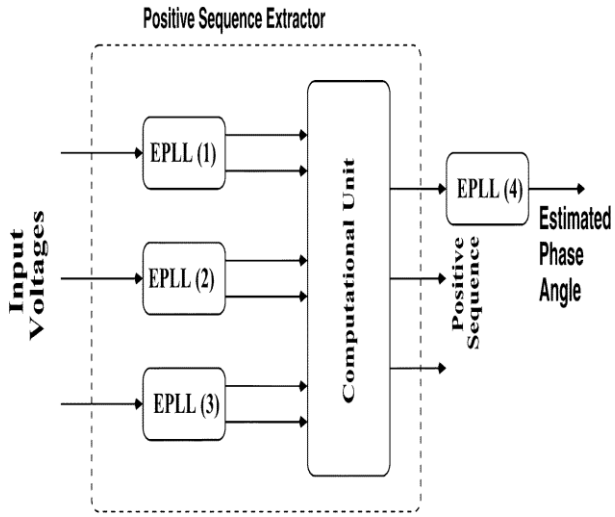

Figure.4.EPLL for Phase Detection [18]

Non-linear Adaptive notch Filter based on the EPLL can be applied for signal analysis both under stationary and non-stationary conditions. This filter can be applicable for sinusoidal waveform peak detection, harmonic identification/detection, detection/extraction of individual components of a signal, instantaneous reactive ,current extraction, disturbance detection, noise reduction in zero-crossings detection, and amplitude (phase) demodulation for flicker estimation [17].

C. Quadrature Phase Locked Loop (QPLL)

Based on estimations for the in-phase and quadrature amplitudes and frequency/phase variations of the input signal, QPLL generates the fundamental component of the input signal. The QPLL is fundamentally different from that of the conventional PLL in the process of phase detection. The sophisticated structure of the Phase Detector of the QPLL estimate the time derivative of the phase angle of the desired component of the input signal directly. The QPLL prevented the presence of nonlinear dependency of the error signal to the phase difference which is the main structural drawback of the conventional PLL. Particularly, in wider lock-in and pull-in ranges and faster convergence rate, the QPLL must have a superior performance over the conventional PLL [5], [21].

The Phase Detector of QPLL consists of six multipliers, two integrators, four different gains, and three adders as shown in figure.5. In-phase and Quadrature-phase outputs of the VCO are multiplied by outputs of the integration units (Ks and Kc). To generate the desired component y (t), results are added. In order to generate an error signal e (t), this component is subsequently subtracted from the input signal u (t) and then multiplied by the VCO outputs. The results are properly gained to drive the two integration units. Input signal fundamental component in terms of frequency, amplitude and phase angle can be locked by QPLL. Also, it directly estimates the frequency [5].

The QPLL output consider a summation of two in-phase and quadrature-phase Components such as

$$y(t) = Ks(t)\sin\Phi(t) + Kc(t)\cos\Phi(t)$$

A proper error signal is

$$e(t)=u(t)-y(t)$$

The frequency of the input signal is derivative of the phase angle such as

$$\omega(t)=d\Phi(t) / d(t)$$

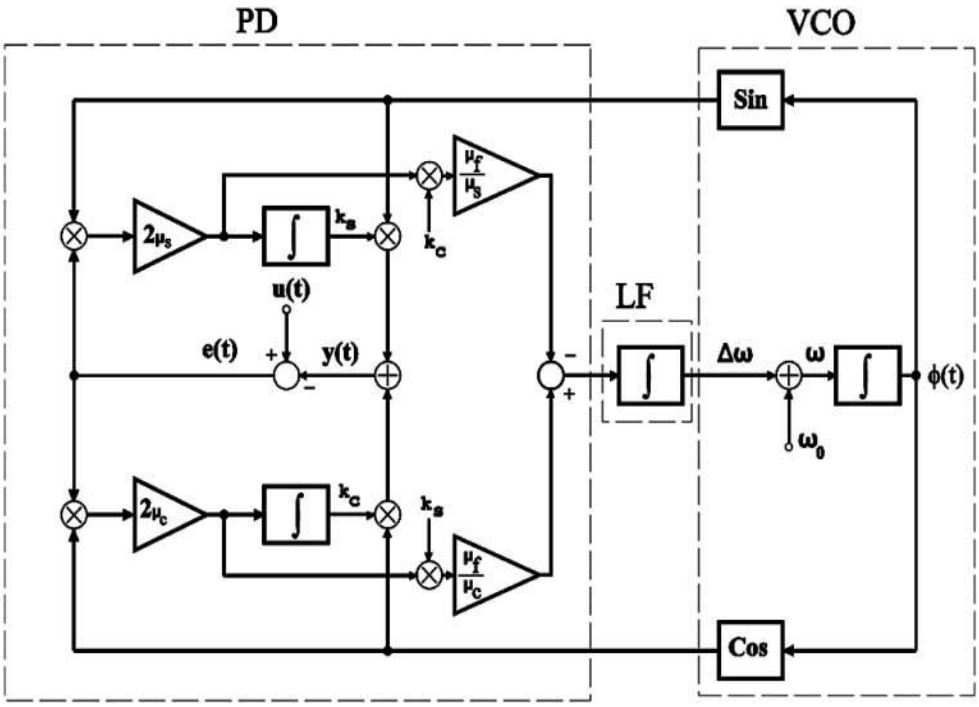

Figure .5.Block Diagram of QPLL [5]

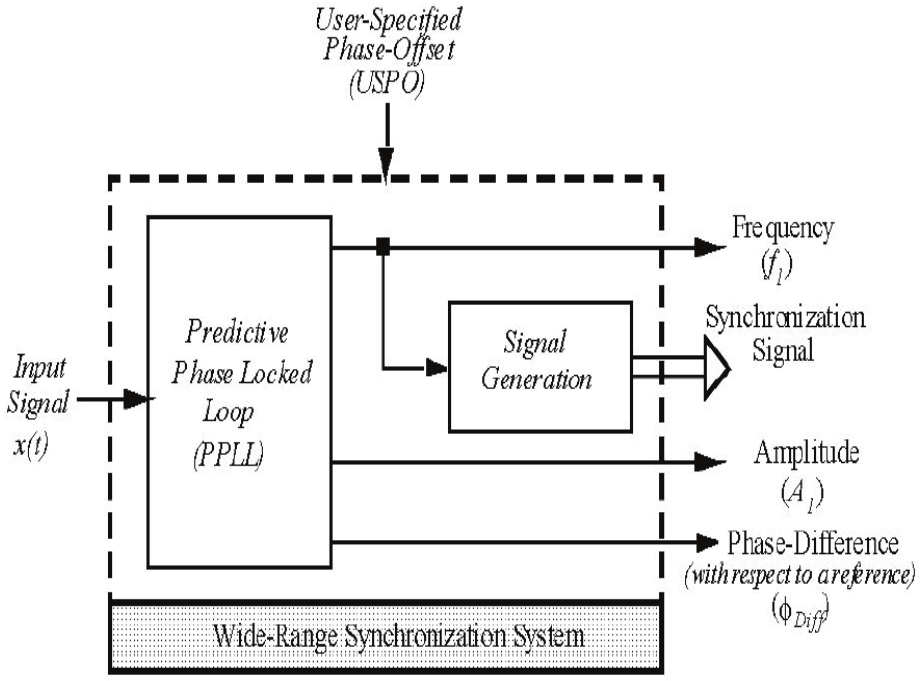

Figure.6.Block Diagram of PPLL [22]

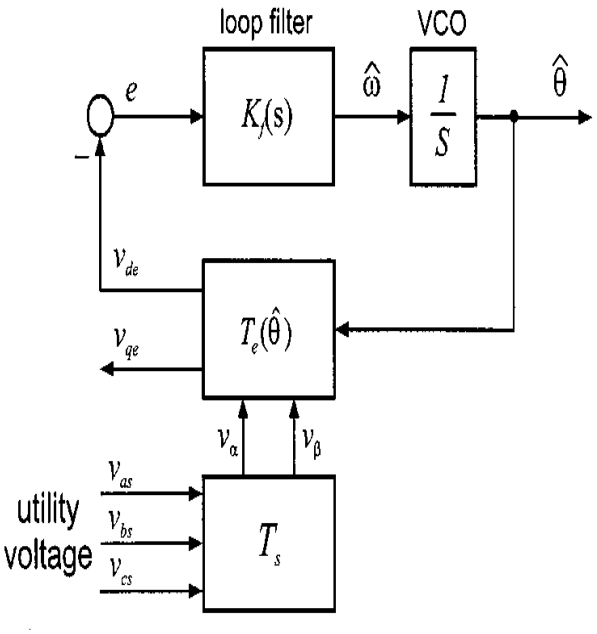

Figure.7.The block diagram of SF-PLL [33]

D. Predictive Phase Locked Loop (PPLL)

One of the wide-range synchronization methods for ac power systems is Predictive phase locked loop (PPLL).Figure.6. Shows block diagram of PPLL. It consists of a predictor (core of PPLL), data acquisition blocks, oscillator and phase-shifter. The predictor acquires three 120◦equidistant samples from the input signal. So that one period of a sinusoidal waveform can be characterized by this samples .In the wide-range synchronization capability, its unique feature lies [22]-[24].

As compare to the conventional PLL phase locking mechanism is same i.e. PPLL locks the phase of input signals. Also PLL employs the analytical expressions for computing the amplitude, phase difference and frequency in a predicted manner. Under the worst cases such as perturbations in amplitude, phase angle and frequency, synchronization information can be extracted within two cycles of the input signal period [15].

E. Adaptive Phase Locked Loop (APLL)

This PLL regulates the system gain adaptively hence it is called as Adaptive PLL (APLL). There are three control units that control voltage magnitude, frequency and phase angle individually. Reduced gain due to voltage sag compensate by voltage controller output. In order to enable elimination of phase and frequency error without compromising transient responses, the output phase angle and its derivative, the frequency signal, are controlled .In case of reduced ac voltage magnitude, Settling time and overshooting are significantly lower are the main advantages of the adaptive PLL [25]-[26].

F. Robust Single Phase Locked Loop (RPLL)

RPLL consists of a multirate sample-holder, a vector rotator, two-phase signal generator, a phase synchronizer and a low-pass filter. Generalized integral-type PLL method based on the phase synchronizer is different from other single-phase PLLs. In case of varying input, the unique multirate sample-holder keeps the output to be constant for a specified holding period. Due to instant reuse of the frequency estimate, it is necessary to avoid the instability phenomenon. In transients, differential-type two-phase signal generator is better than the integral-type. Estimatation of amplitude, phase and frequency of single-phase signals with, harmonics distortion, amplitude sag/swell, frequency variation, contaminated noise, and/or phase jump can be possible by robust single-phase PLL [27]-[32].

G. Synchronous Frame Phase Locked Loop (SF-PLL)

This PLL technique is mostly used in three-phase systems. Figure.7. illustrated the block diagram of SF-PLL. By synchronizing the PLL rotating reference frame to the utility voltage vector, the instantaneous phase angle theta is detected. The setting of direct or Quadrature axis reference voltage Vd or Vq to zero by PI the controller. So that in the reference being locked to the utility voltage vector phase angle. Also, the voltage frequency f and amplitude Vm can be obtained by the products. The SF-PLL with a high bandwidth can detect the phase and amplitude of the utility voltage vector very fast and precisely for ideal utility conditions without any harmonic distortions or unbalance [33]-[35].

In order to reject and cancel the effect of high-order harmonics in distorted utility voltage on the output, the SF-PLL can still operate if its bandwidth is reduced at the cost of the PLL response speed reduction. However, in the presence of the unbalanced utility voltage, the PLL bandwidth reduction is not an acceptable solution. It avoids the double-frequency error problem of single-phase standard PLL. It offers ease of parameter tuning, a relatively simple structure and robust features for digital implementation. The representation of the SRF-PLL in the stationary frame shows that the three-phase SRF-PLL does not really need to have three input signals to operate. It can operate if it is supplied by phase-a signal and its orthogonal version that is its 90º phase shifted version. The frequency, amplitude and phase values provided by SRF-PLL are average information not individual-phase. The SRF-PLL may not be applied to single phase systems in a straightforward. The SF-PLL provides a useful structure for single-phase PLLs. Also it created the 90-degree-shifted orthogonal component of the single phase input signal [36]-[38].

III.CONCLUSION

A phase-locked loop or phase lock loop (PLL**)** is a control system that generates an output signal whose phase is related to the phase of an input signal. Phase-locked loops are widely used for synchronization purposes. In PLL applications it is frequently required to know when the loop is out of lock. Due to noise, distortions, and frequency variations, the complexity of phase locking is increased. However, large and abrupt variations of frequency and phase of the input signal may not be properly tracked by a control loop. In case of EPLL, the extracted output is coherent and synchronized with the desired component of the input. With respect to external noise pollution and internal parameter variations, this structure is robust The QPLL prevented the main structural drawback of the conventional PLL such as the presence of nonlinear dependency of the error signal to the phase difference. By proper designing the loop filter, SF-PLL frequency and phase tracks the utility frequency and phase respectively. In three-phase system, the most extended technique used for grid synchronization is a synchronous reference frame PLL (SRF-PLL).Hence for detection and control of the phase, frequency and amplitude of the grid voltage & inverter voltage we can use the a synchronous reference frame PLL (SRF-PLL) as an synchronization technique.

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