Power Efficient D Flip Flop Circuit Using MTCMOS Technique in Deep Submicron Technology

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Abstract

In analog, digital and mixed signal designs D Flip Flop plays very crucial role. These class of flip flops are preferred over other to realize different counters and other circuits. This paper addresses the design of low power D flip flop cell and its comparison with standard 5T TSPC D flip flop. The low power D flip flop cell is designed by employing MTCMOS leakage power reduction technique with standard 5T TSPC D flip flop cell. These two circuits are simulated on Cadence Virtuoso tool in 180 nm, 90 nm, 45 nm technology. Parameters like power dissipation, delays, leakage power etc are compared for these two different circuits. However layouts and waveforms are shown only for 180 nm technology.

Keywords— *D Flip Flop, Delays, Leakage power, MTCMOS, TSPC.*

1. Introduction

The memory elements used in clocked sequential circuits capable of storing one bit of information. A flip flop circuit has two outputs, one for the normal value and one for the compliment value of the bit stored in it [1]. Different type of Flip Flops signifies the way in which binary information enters a flip flop. A binary state can be maintained by flip flop circuit indefinitely (as long as power is delivered to the circuit) until directed by an input signal to switch states.

The D-Flip Flop is a modification of basic clocked SR flip flop. The D flip-flop is by far the most important of the clocked flip-flops as it ensures that inputs S and R are never equal to one at the same time. D-type flip-flops are constructed from a gated SR flip-flop with an inverter added between the S and the R inputs to allow for a single D (data) input. This single data input D is used in place of the "set" signal, and the inverter is used to generate the complementary "reset" input thereby making a level-sensitive D-type flip-flop from a level-sensitive RS-latch as now S = D and R = not D as shown.. The D flip flop receives the designation from its ability to transfer “data” into a flip flop. It is also expanded as Delay Flip Flop.

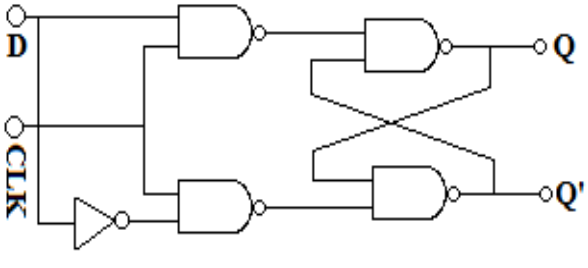


Fig.1: D Flip Flop Circuit

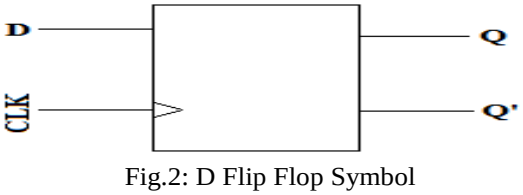


Fig.2: D Flip Flop Symbol

The analysis of excitation table of D flip flop shows

that D must be 0 (zero) if Q(t+1) has to be 0 (zero) and D must be 1 (one) if Q(t+1) has to be 1 (one) regardless the value of Q(t) [2]. The excitation table of D flip flop is given below.

TABLE 1: Excitation Table of D Flip Flop

D	Q(t+1)
0	0
1	1

D Flip Flop is one of the important digital circuit which has enormous applications in various digital design. This is the age of fabricating the digital and analog circuits on ICs using CMOS technology. CMOS is most promising technology among available techniques. Among various advantages associated with this technique the most important is its low power dissipation feature. Whether digital systems are high speed, high density, low power, or low cost, CMOS technology finds ubiquitous use in the majority of leading edge commercial applications [3].

Digital CMOS circuits dissipate power in three ways due to signal transition, due to short circuit currents and due to leakage currents [4]. Delays depend on many factors like supply voltage, threshold voltage, aspect ratio, oxide thickness and load capacitances [5].

Low power design with high performance for battery operated portable systems, is a strong direction for CMOS system design. The power dissipated by a CMOS circuit (P_{TOTAL}) is the sum of the static power (P_S), the dynamic power (P_D), and the short circuit power (P_{SC}). i.e.

$$P_{TOTAL} = P_S + P_D + P_{SC}$$

Ps may be reduced to that due to leakage, if any circuits that draw DC power such as pseudo NMOS circuits are eliminated. The dynamic power is dependent on the supply voltage, the stray capacitances, and the frequency of operation. The reduction in supply voltage is quadratic while the speed is inversely proportional to supply voltage [6,7]. The stray capacitances may be reduced by using smaller no. of transistors to implement a function [6]. The essential thing in CMOS design technique is that it should maintain the performance while achieving the low power [6].

In this paper 5T TSPC D Flip Flop is compared with power efficient 5T TSPC D Flip Flop employing MTCMOS leakage power reduction technique [8], these two circuits are designed and simulated in 180 nm, 90 nm, and 45 nm technologies in Cadence virtuoso tool using Spectre simulator.

The paper is organized as follows, Section I is giving the brief introduction in context of theory of D Flip Flop, modes of power dissipation in CMOS circuits, and the brief idea of what this paper is dealing with.

In Section II brief theory of 5T TSPC D Flip Flop is given.

Section III is dealing with the implementation of 5T TSPC D Flip Flop with MTCMOS technique, in this section concept of MTCMOS technique is also taken up.

Simulations of different circuits are presented in Section IV.

Section V is giving the results obtained for different parameters and then followed by a brief discussion of these results. The results are tabulated in two tables, Table 2 is showing the results for 5T TSPC D Flip Flop, and Table 3 is showing the results for 5T TSPC with MTCMOS.

Section VI is giving the conclusion of this paper, which is then followed by the Reference section.

2. 5T TSPC D Flip Flop

In this section brief theory of 5T TSPC D Flip Flop is presented. TSPC stands for True Single Phase Clocked logic in which we only have one clock, and do not need an inverted clock. TSPC circuit technique uses only one phase of the clock and avoids skew problems thereby improving the performance of a digital system. There are several benefits with this technique such as the elimination of skew due to different clock phases and clock signal being generated off chip, which implies significant savings in chip area and power consumption [9].

The following figure is showing the schematic of 5T TSPC D Flip Flop which is composed of 3 NMOS and 2 PMOS transistors [10, 11, 12]. The truth table of 5T TSPC D Flip Flop is shown in following table.

TABLE 2: TRUTH TABLE of 5T TSPC D FLIP FLOP

CLK	D	P1	N1	N2	P2	N3	Q
1	0	ON	ON	OFF	OFF	ON	0
1	1	OFF	ON	ON	ON	OFF	1
0	0	ON	OFF	OFF	OFF	OFF	0
0	1	OFF	OFF	ON	OFF	OFF	0

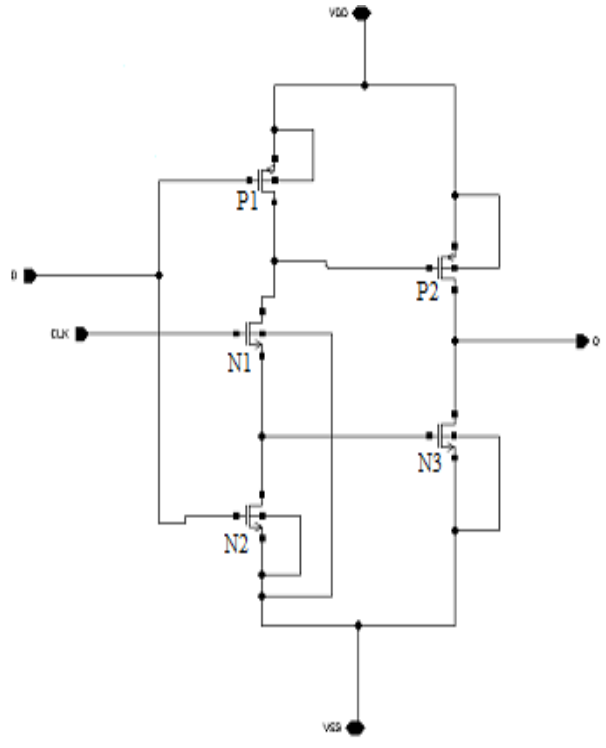


Fig.3: 5T TSPC D Flip Flop Schematic

When CLK and input D are high then the transistors P1, N3 are OFF and remaining transistors P2, N1, N2 are ON. The output becomes high. During ON clock period whatever is the values of input it becomes output.

3. 5T TSPC D Flip Flop with MTCMOS

Multi-threshold CMOS (MTCMOS) is a variation of CMOS chip technology which has transistors with multiple threshold voltages (V_{th}) in order to optimize delay or power. A common implementation of MTCMOS for reducing power makes use of sleep transistors. Logic is supplied by a virtual power rail. Low V_{th} devices are used in the logic where fast switching speed is important. High V_{th} devices connecting the power rails and virtual power rails are turned on in active mode, off in sleep mode. High V_{th} devices are used as sleep transistors to reduce static leakage power. High V_{th} devices are used on non-critical paths to reduce static leakage power without incurring a delay penalty. Typical high V_{th} devices reduce static leakage by 10 times compared with low V_{th} devices [13].

Multithreshold voltage CMOS (MTCMOS) reduces the leakage by inserting high-threshold devices in series to low V_{th} circuitry [14].

The brief description of MTCMOS in general is given on next page. The MTCMOS operates in two modes – high threshold and low threshold modes. The high threshold mode reduces the leakage power and low threshold mode improves the speed performance.

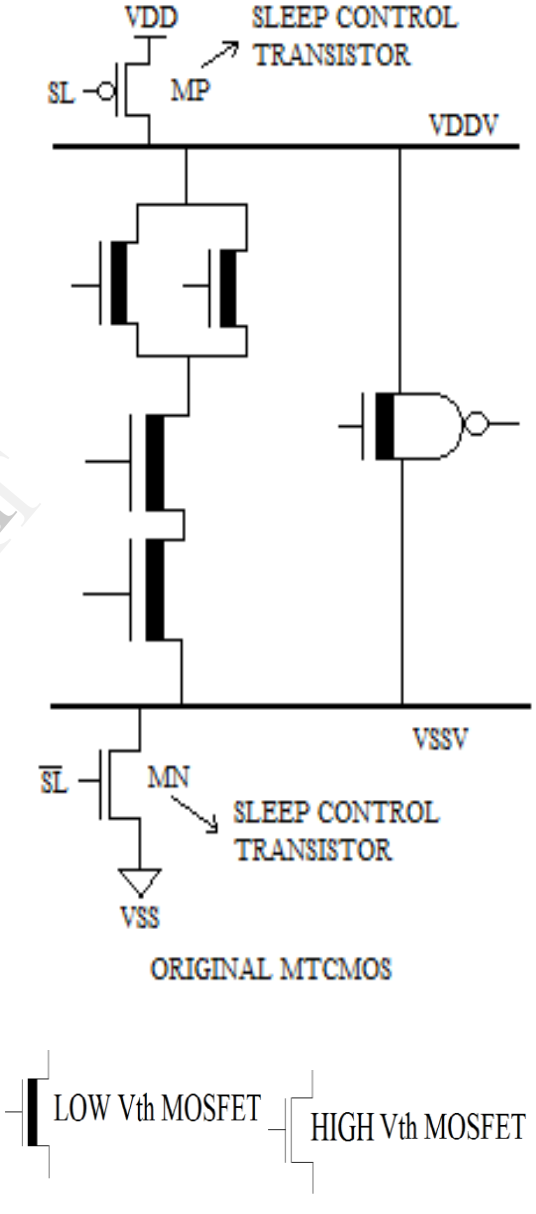


Fig.4: MTCMOS in General

Fig. 4 shows the schematic of an MTCMOS circuit. A sleep control scheme is introduced for efficient power management. In the active mode, SL is set low and sleep control high transistors (MP and MN) are turned on. Since their on-resistances are small, the

virtual supply voltages (VDDV and VSSV) almost function as real power lines. In the standby mode, SL is set high, MN and MP are turned off, and the leakage current is low [15]. This is the general mechanism of MTCMOS technique, which is employed in this work.

The following figure is showing the schematic of 5T TSPC D Flip Flop with MTCMOS technique. Two sleep transistors P3 and N4 are used in this circuit. The transistor N4 is supplied with signal SL (sleep) and transistor P3 is supplied with signal SL' (complement of sleep). SL and SL' transistors are supplied with high threshold voltages. When SL signal is low SL' is high, there will be no current flow in low threshold voltage main circuit. When SL is high and SL' is low circuit works in normal mode.

The table following the D Flip Flop circuit is the truth table of 5T TSPC with MTCMOS D Flip Flop.

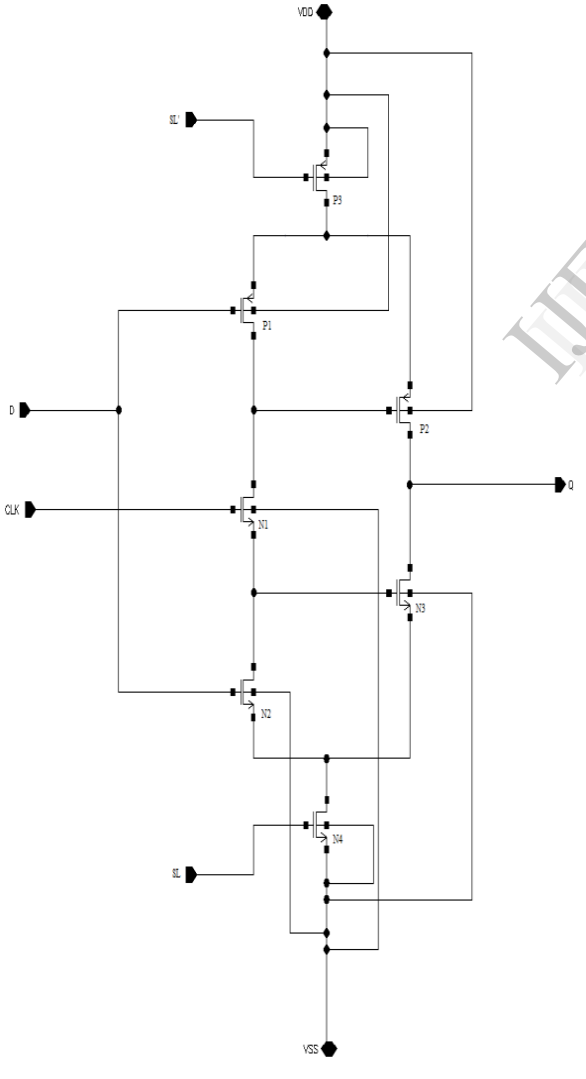


Fig.5: Schematic of 5T TSPC With MTCMOS D Flip Flop

TABLE 3: TRUTH TABLE of 5T TSPC WITH MTCMOS D FLIP FLOP

CLK	D	SL	P1	N1	N2	P2	N3	P3	N4	Q
1	0	0	ON	ON	OFF	OFF	ON	ON	OFF	0
1	0	1	ON	ON	OFF	OFF	OFF	OFF	ON	0
1	1	0	OFF	ON	ON	ON	OFF	ON	OFF	1
1	1	1	OFF	ON	ON	ON	OFF	OFF	ON	1
0	0	0	ON	OFF	OFF	OFF	OFF	ON	OFF	0
0	0	1	ON	OFF	OFF	OFF	OFF	OFF	ON	0
0	1	0	OFF	OFF	ON	OFF	OFF	ON	OFF	0
0	1	1	OFF	OFF	ON	ON	OFF	OFF	ON	0

4. Simulations

The Fig.6 is showing the layout of 5T TSPC D Flip Flop.

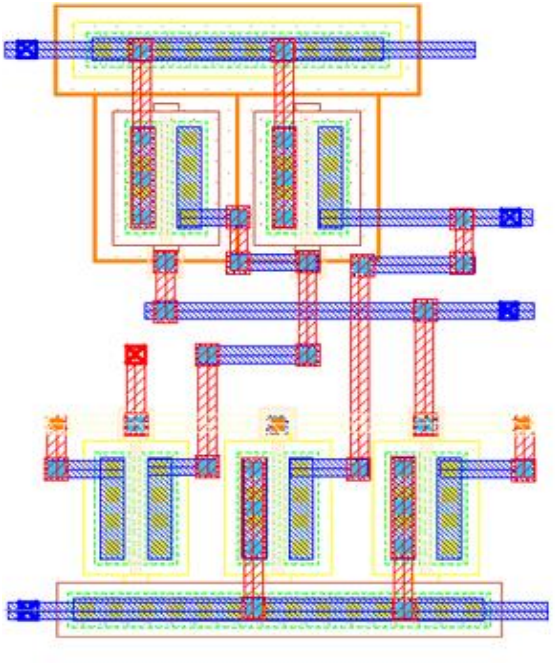


Fig.6: Layout of 5T TSPC D Flip Flop

The following Fig.7 is showing the layout of 5T TSPC D Flip Flop with MTCMOS.

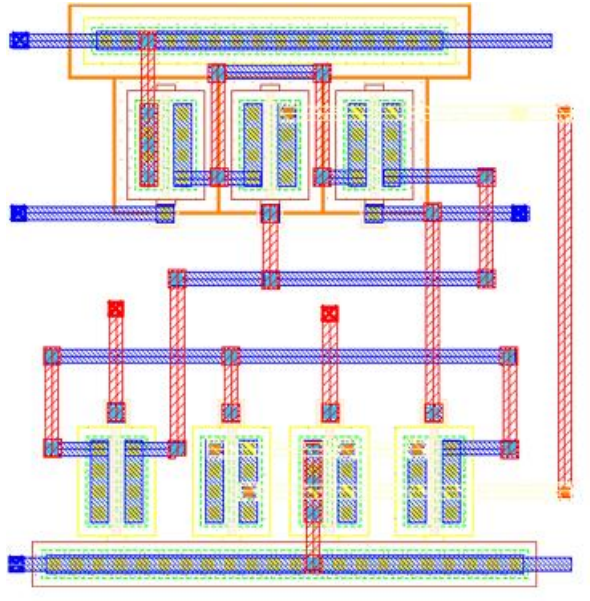


Fig.7: Layout of 5T TSPC with MTCMOS D Flip Flop

Though study is being done for 180 nm, 90 nm and 45 nm technologies the layouts of 180 nm technology circuits are shown. These layouts are drawn keeping in mind the industry conventions like metal layers 1, 3 and 5 for horizontal connections and metal layer 2, 4 and 6 for vertical connections. The total width of all the transistor of both the circuits is kept equal to 2u. The number of fingers in each of the transistors is equal to one and consequently finger width of each finger will be equal to 2u [16].

5. Results and Discussion

The different circuits have been simulated in Cadence Virtuoso tool in 180 nm technology [17]. The parameters and concerned results are tabulated in the table drawn below. The results are calculated for two supply voltages for each technology so that the effect of the supply voltage variation can also be adjudged [18].

The variations in the values of various parameters, for 5T TSPC D Flip Flop can be seen in Table 4. As the technology is scaling down the value of power dissipation is increasing the similar trend can be seen in the values of leakage power. The variations in delay are not showing any regular trend. Power delay product is simply the product of corresponding values of power dissipation and delay.

TABLE 4: RESULTS OF 5T TSPC D FLIP FLOP

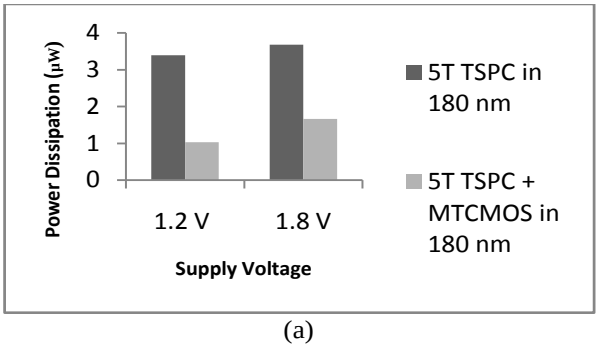
Parameters	5T TSPC D FLIP FLOP					
	180 nm		90 nm		45 nm	
	1.2 V	1.8 V	0.7 V	0.9 V	0.5 V	0.7 V
Power Dissipation (µW)	3.39	3.68	3.54	3.98	3.73	4.20
Delay(nS)	0.131	0.140	0.138	0.112	0.129	0.091
Power Delay Product (fJ)	0.444	0.515	0.488	0.446	0.481	0.382
Leakage Power (nW)	188	199	215	241	254	283

The table drawn below is showing the variations in the values of various parameters, for 5T TSPC with MTCMOS D Flip Flop. Due to the MTCMOS leakage power reduction technique used with this circuit, the values for power dissipation and leakage power are showing declining trend as we scale down through the technology, this is what we expecting.

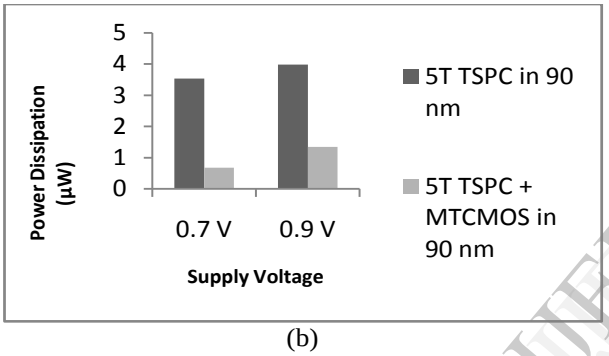
TABLE 5: RESULTS OF 5T TSPC WITH MTCMOS D FLIP FLOP

Parameters	5T TSPC D FLIP FLOP WITH MTCMOS					
	180 nm		90 nm		45 nm	
	1.2 V	1.8 V	0.7 V	0.9 V	0.5 V	0.7 V
Power Dissipation (µW)	1.03	1.66	0.68	1.34	0.41	0.97
Delay(nS)	0.152	0.149	0.223	0.197	0.321	0.256
Power Delay Product (fJ)	0.156	0.247	0.152	0.264	0.132	0.248
Leakage Power (nW)	103	112	75	99	61	78

The comparison of power dissipation and leakage power for these two circuits has been shown in the form of bar diagrams, to have a glance at the relative difference between the values of these parameters.



(a)



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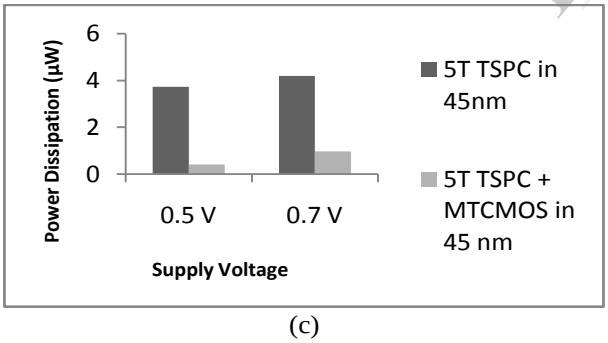

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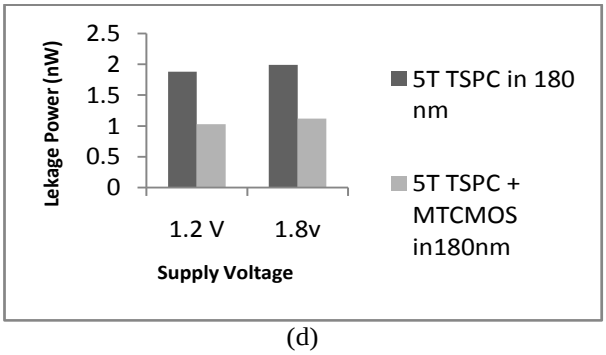

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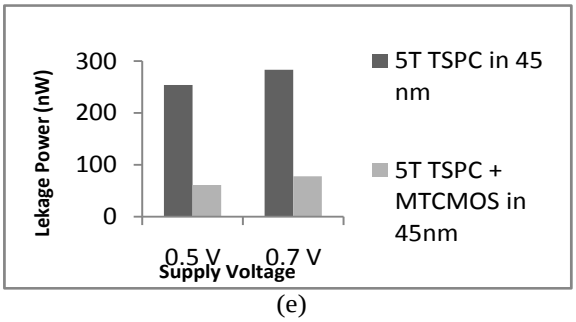

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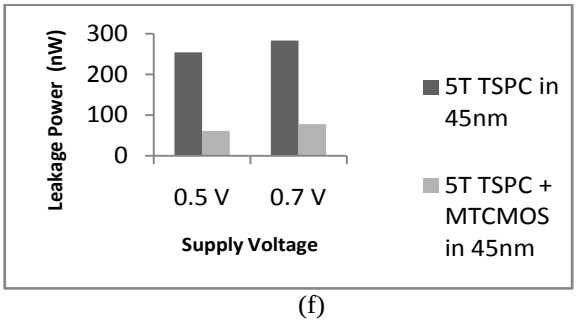

(f)

Fig.8: Bar Diagrams for Comparison of Parameters

The values of various parameters studied, for these two circuits are tabulated in Table 4 and Table 5, from where clear comparison between values of different parameters for these circuits in different technologies at different supply voltages can be seen. To emphasize the results for power dissipation and leakage power their comparative variations are shown in the form of bar diagrams in Figure 8.

6. Conclusions

It is concluded that 5T TSPC D Flip Flop with MTCMOS technique is having the considerably low, power dissipation and leakage power values in comparison of 5T TSPC D Flip Flop without MTCMOS technique, for each submicron technology taken for study i.e. 180 nm, 90 nm, and 45 nm.

7. References

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