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Power Electronic Interface for Grid-Connected PV array using SEPIC Converter and Line-Commutated Inverter with MPPT

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Abstract

A power electronic interface for grid connected PV system has been proposed using SEPIC converter and line commutated SCR inverter. A PV array consisting of three panels each rated for 21.2V and 5.17A connected in series has been considered. The firing angle of the line commutated inverter is fixed at some value and a closed loop controller has been designed to automatically adjust the duty cycle of SEPIC converter to provide the required maximum dc link current so that always the maximum power available at the output of the PV array is fed to the utility grid. The complete system is modeled in MATLAB platform and simulations have been carried out and the results are furnished.

KEYWORDS: *Grid-connected PV, Line commutated inverter, Maximum Power Point Tracking, and SEPIC converter.*

1. Introduction

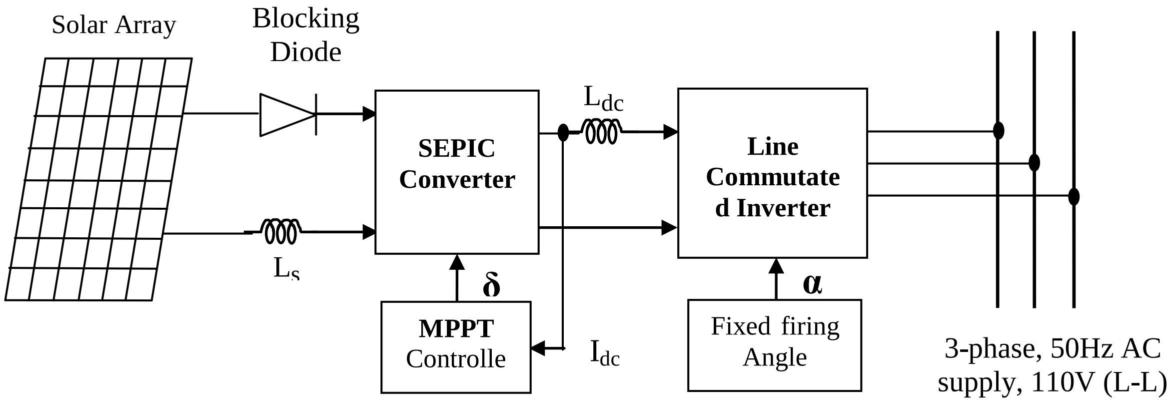
The development in renewable energy sources replaces the other traditional energy sources. Among the renewable energy sources, solar energy plays a major role due to its pollution-free nature. For economical reasons the solar energy is not directly interfaced with the utility grid. Hence a power electronic interface is developed to interface the solar systems to the utility grid [1,2].

A SEPIC converter is introduced between solar system and grid connected line commutated inverter (LCI). SEPIC converter has output voltage can be greater than or less than peak input voltage. It can be include lesser transistor stresses, higher value of transistor RMS current, limiting the inrush currents and isolated topologies are possible.

Further, recent researches have focused on how to get maximum power from solar energy [3,4]. All the schemes invariably employ forced commutation for an inverter. In the present paper three phase line commutated inverter is operating at fixed value of firing angle, SEPIC converter and its closed loop simulation using MPPT Controller designed to automatically adjust the duty cycle of SEPIC converter to provide the required maximum dc link current so that always the maximum power available at the output of the PV array is fed to the utility grid.

2. Proposed Scheme

The block diagram of the proposed solar energy conversion scheme is shown in Fig.1. It consists of a solar array having three solar panels connected in series, interfaced to the three-phase utility grid through a power electronic interface. The DC voltage available at solar array is first stepped up to a voltage greater in magnitude to the grid voltage and converted to AC using the line commutated inverter in order to transfer the power to the utility grid. In the feedback loop, an MPPT controller is used to control the duty cycle of the dc-dc converter to maintain maximum value of dc link current always. This method senses the dc link current and compares it with previous value. The result decides the change (increment or decrement) in duty cycle of the converter. The duty cycle for the dc-dc converter is thus adjusted so that always the maximum power available at the output of the PV array is fed to the utility grid. This is because as line commutated



δ-duty cycle of SEPIC converter (Variable)
α-firing angle delay of inverter (Fixed)

Fig.1. Block diagram of the proposed scheme

inverter is operating at fixed value of firing angle, its output DC voltage is fixed, so maximum DC link current results in maximum power. Here the DC-DC converter is involved in both PV panel voltage boosting and MPP tracking.

3. PV Array Model

The electrical equivalent circuit of PV cell is shown in Fig.2.

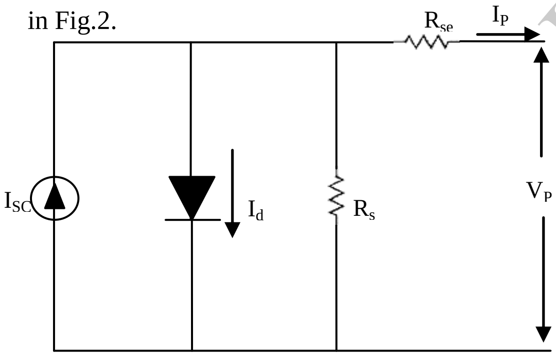


Fig.2. Equivalent circuit of PV cell

The classical equation of a PV cell is describes the relationship between current and voltage of the cell.

$$I_{PV} = I_{SC} - I_d - I_{sh} \qquad (1)$$

$$I_{PV} = I_{SC} - I_0\left\{\exp\left[\frac{q(V+R_{se}I_{PV})}{nkT_k}\right]-1\right\} - \frac{V+R_{se}I_{PV}}{R_{sh}} \qquad (2)$$

Assuming

$$\exp\left[\frac{q(V+R_{se}I_{PV})}{nkT_k}\right] >> 1$$

$I_0/I_{SC} = 10^{-9}$ And $I_{ph} = I_{SC}$

Now equation (2) can be written as

$$I_{PV} = I_{SC} - I_d$$

Where,

$$I_d = 10^{-9} I_{SC}\left[\exp\left\{\frac{20.7}{V_{oc}}(V_{PV} + R_{se}I_{PV})\right\}\right] \qquad (3)$$

Further from equation (2) the value of V_{OC} can be expressed as

$$V_{OC} = \left(\frac{nkT_k}{q}\right)\ln\frac{I_{SC}}{I_0} \quad \text{, making } I_{PV} = 0 \qquad (4)$$

The PV model developed using the above equations are used for simulation in the proposed scheme [5].

4. SEPIC Converter

It consists of a SEPIC converter, an inductor and line commutated inverter. The SEPIC converter is a non-inverting DC-DC converter and can generate voltages either above or below the input. The input current is non-pulsating, but the output current is pulsating. The name SEPIC is an acronym for single ended primary inductance converter. The power circuit of SEPIC DC-DC converter is shown in Fig.3.

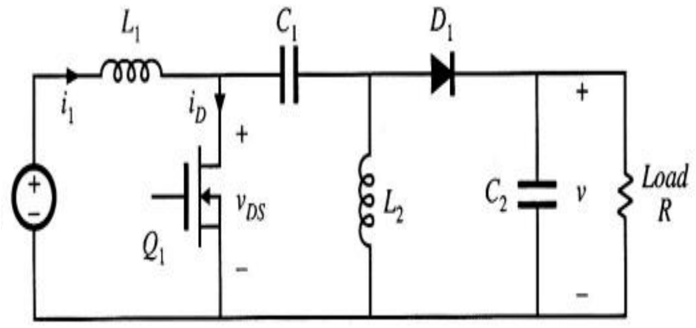


Fig.3. Power circuit of the SEPIC converter with R load

4.1 Design of SEPIC Converter

By developing an equivalent model for the SEPIC converter without coupled inductors, the converter can be analyzed and designed in a unified framework. The design equations are as follows: For continuous mode, the duty cycle is,

$$D = \frac{Vo + VD}{Vi + V_o + V_d} \qquad (5)$$

Where,

Vi: Input voltage (V), V_D: Diode voltage (V), V_o: Output Voltage (V)

$$D\max = \frac{Vo + VD}{Vi\min + Vo + VD} \qquad (6)$$

Choosing $(V_i)_{min}$ = 35 V,

$$D\max = \frac{145 + 0.7}{35 + 145 + 0.7}$$

= 0.81

The minimum possible duty cycle (D_{min}) is limited by the maximum input voltage of the regulator and is calculated as

$$D\min = \frac{Vo + VD}{Vi\max + Vo + VD} \qquad (7)$$

Choosing V_{imax} = 55 V

$$D\min = \frac{145 + 0.7}{55 + 145 + 0.7} = 0.725$$

A good rule for determining the inductance is to allow the peak-to-peak ripple current to be approximately 40% of the maximum input current at the minimum input voltage. The ripple current flowing in equal value inductors L1 and L2 is given by:

$$\Delta I_L = I_O X \frac{V_O}{(V_i)_{\min}} X\, 20\% = 1.62 X \frac{145}{35} X\, 0.23 = 1.54A$$

Inductor values are calculated as:

$$L1 = L2 = \frac{(V_i)_{\min}}{\Delta I_L X f_{sw}} X D_{\max} = \frac{35}{1.54 X 5 X 10^3} X\, 0.81 \approx 4mH$$

f_{sw} is the switching frequency of the dc-dc converter, which is taken as 5 kHz.

So values of inductors are L1=L2 = 4mH

The output capacitance can be calculated as

$$C2 \geq \frac{Io.D\max}{Vripple.0.5.f} \quad ,$$

V_{ripple} = 2 % of output voltage Vo

$$\geq \frac{1.62 x 0.81}{0.02 x 0.5 x 145 x 5kHz}$$

$$\geq 250 \mu F$$

So it is taken as 500µF

The capacitor value for C1 is assumed as 100µF.

5. Analysis of Line Commutated Inverter

In the proposed scheme the dc output from the dc-dc converter is connected to grid via line commutated inverter. A line commutated inverter [6] is nothing but a fully controlled bridge converter as shown in Fig.4, which is operated at firing angle delay (α) in the range 90^0 to 180^0.

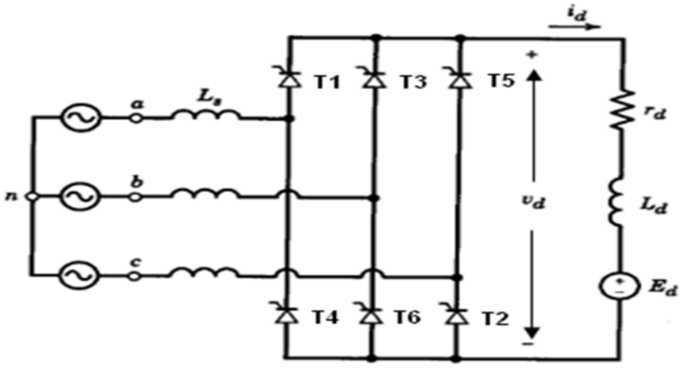


Fig. 4 Line Commutated Inverter

If the load is capable of supplying power, then the direction of power flow can be reversed by the reversal of the dc voltage (E_d), the current direction being unchanged. The firing angle delay α must be

greater than 90°. In the present case, no extra effort is required to synchronize the inverter output frequency with that of the grid supply. This of course is possible only with SCR converters. The inductance L_{dc} is used in the dc side to reduce the ripple in current.
The average output voltage Vd is hence given by

$$V_d = \frac{3\sqrt{3}}{\Pi}(V_m)_{ph}\cos\alpha \qquad (8)$$

where

$(V_m)_{ph}$ = maximum phase voltage of the utility grid

α = firing angle delay.

5.1 Harmonic Analysis of Three Phase Line Commutated Inverter

The RMS value of fundamental component of phase-a current I_a is

$$I_{a1} = \sqrt{\frac{a_1^2+b_1^2}{2}} = \sqrt{\frac{6}{\Pi}}I_{dc} = 0.7797I_{dc} \qquad (9)$$

$$(I_a)_{rms} = \sqrt{\frac{1}{\Pi}\int_{\alpha+30^0}^{\alpha+150^0}\left(I_{dc}^2\right)d\omega t} = I_{dc}\sqrt{\frac{2}{3}} \qquad (10)$$

$$THD = \left[\left(\frac{I_a}{I_{a1}}\right)^2 - 1\right]^{\frac{1}{2}} = 0.3108 = 31.08\% \qquad (11)$$

6. Maximum Power Point Tracking Controller

To obtain maximum power from photo array, photovoltaic power system usually requires a maximum power point tracking (MPPT) controller. The output power of a PV array varies according to the sunlight conditions, atmospheric conditions, including cloud cover, local surface reflectivity, and temperature. So, a MPPT is necessary in order to extract the maximum power from the array irrespective of temperature and irradiation conditions. In the present work, MPPT controller is realised using an algorithm implemented in m-file. The closed loop controller used to track maximum power from PV array in the proposed scheme is shown in Fig.5

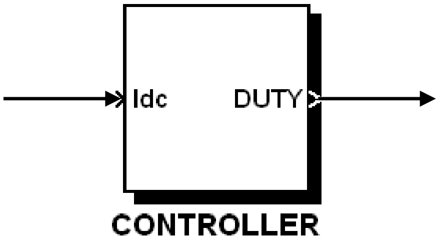


Fig. 5 MPPT Controller

It adjusts the duty cycle of the dc-dc converter (SEPIC) to maintain maximum value of dc link current always. The algorithm [7] used is presented as a flowchart in Fig.6.

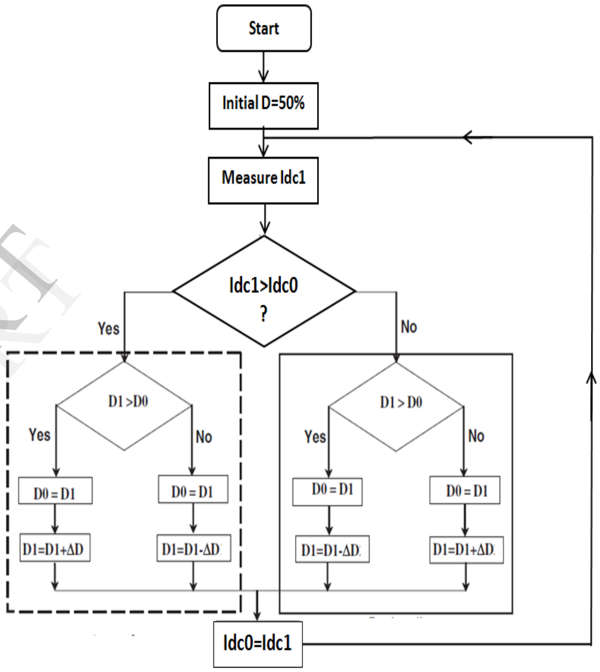


Fig. 6 Flow chart of Algorithm used in Controller

The algorithm starts with an initial duty cycle of 50% (D1) and the pulses are fed to the SEPIC converter. The DC- link current is measured and it is taken as present value ($I_{dc}1$) and is compared with previous value ($I_{dc}0$, which is initially taken as zero) and the result decides the further code to be implemented. If present value is greater than previous value it goes to CODE-1. In CODE-1, present value of duty cycle (D1) is compared with previous value **(D0,** initial value is zero**)**. If it is greater ,algorithm increments the duty cycle and if it is less ,decrements the duty cycle on the other hand if present value of current is less than previous value it goes to CODE-2.

In CODE-2 increment and decrement cases are reversed as shown in flow chart. The duty cycle for the SEPIC converter is thus adjusted so that always the maximum current is maintained at d.c. link this in turn means maximum power available at the output of the PV array is fed to the utility grid. This is because as line commutated inverter is operating at fixed value of firing angle, its output dc voltage is fixed, so maximum dc link current results in maximum power.

7. Complete Closed Loop Model of the Proposed Scheme

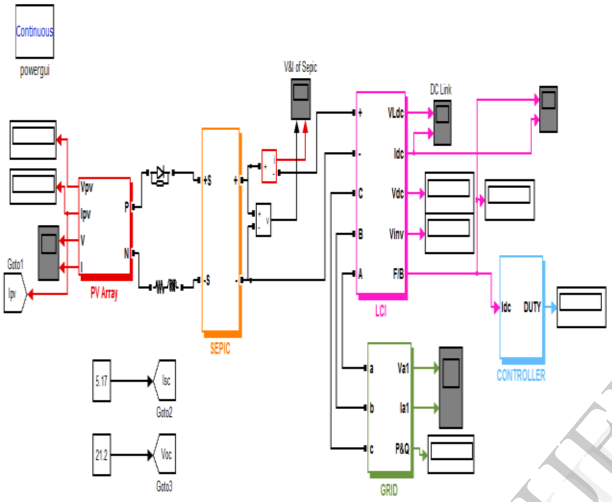


Fig. 7 Complete Simulation model of Proposed Scheme

8. Simulation Results

The proposed solar energy scheme is completely modeled using MATLAB simulink blocks in PSB platform. It consists of solar array block, SEPIC converter; line commutated inverter, three-phase power grid and closed loop controllers. As the solar radiation increases, the output of the solar array increases. For any variation in solar irradiation, the output of the SEPIC converter is held constant. The closed loop model of the proposed scheme is simulated and the simulation results of the proposed scheme such as power fed to grid, injected grid current, and grid voltage, dc link voltage and current are shown in Fig.8, Fig.9 and Fig.10 the results for standard climate conditions: i.e. V_{OC} = 63.6V (Each panel Voc=21.2V) and I_{sc} = 5.17A

Table 1 Simulation results of the proposed scheme for standard conditions

Parameters	Simulation results
Duty of SEPIC at which maximum power occurs, δ	73%
DC link voltage, V_{dc} (in V)	-143.79
DC link current, I_{dc} (in A)	1.592
Active power fed to the grid, P_{grid} (in W)	-230

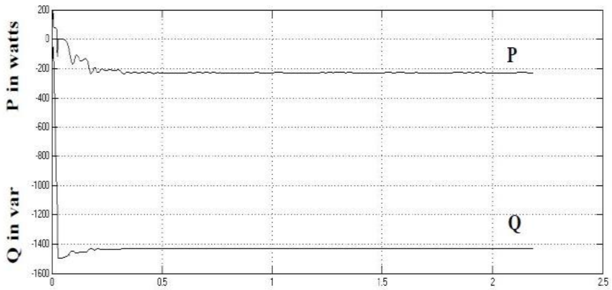
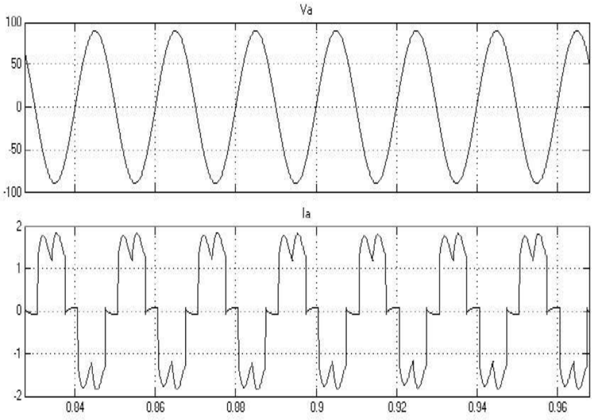


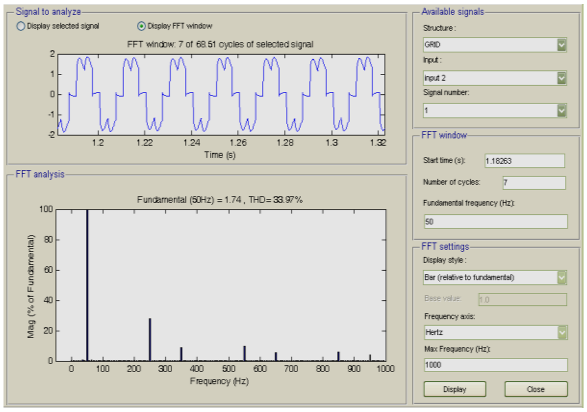
Fig. 8 Active and reactive power at grid for standard conditions

8.1 Grid Voltage and Current

Grid voltage and current of phase-a are shown in Fig.9 and Fig.10, Waveforms without filter are shown in Fig.9 and with filter are shown in Fig.10



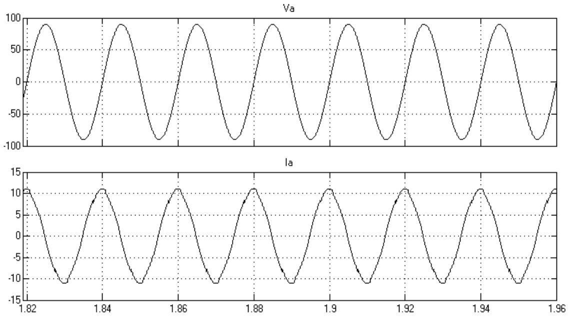
(a) Voltage and current Waveforms



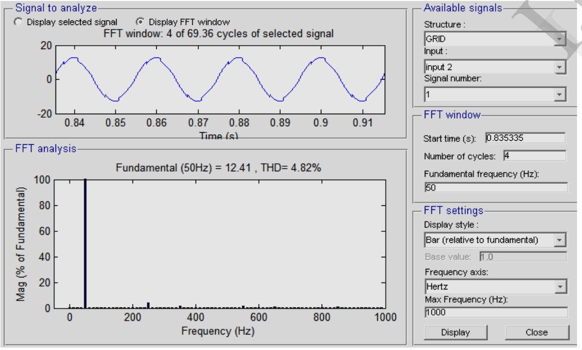
Structure : GRID
Input : input 2
Signal number: 1
Start time (s): 1.18263
Number of cycles: 7
Fundamental frequency (Hz): 50
Display style : Bar (relative to fundamental)
Base value: 1.0
Frequency axis: Hertz
Max Frequency (Hz): 1000

(b) FFT analysis of phase-a current showing THD = 33.97%

Fig. 9 Simulation results of Phase-a of grid without filter



(a) Voltage and current Waveforms



Structure : GRID
Input : input 2
Signal number: 1
Start time (s): 0.835335
Number of cycles: 4
Fundamental frequency (Hz): 50
Display style : Bar (relative to fundamental)
Base value: 1.0
Frequency axis: Hertz
Max Frequency (Hz): 1000

(b) FFT analysis phase-a current showing THD = 4.82%

Fig. 10 Simulation results of Phase-a of grid with filter

9. Conclusion

A simple closed loop scheme employing a SEPIC converter and Three-phase line commutated inverter has been developed for interfacing solar array with the utility grid. Simulation studies have been carried out to get the various parameters of the scheme such as active power and reactive powers. As the inverter is being operated as line commutated, the synchronization of output frequency with grid frequency does not arise. However due to losses in the inductor, the output power fed to the grid is fairly small. This can be increased by selecting an inductor with low losses. Further, the THD of output current waveform is fairly high due to harmonics introduced by switching of the inverter. This requires a tuned filter to be connected across the grid terminals.

10. References

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