Power Optimized Energy Efficient Hybrid Circuits Design by Using A Novel Adiabatic Techniques

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ABSTRACT

The never ending need for low-power and low-noise digital circuits has intrigued designers to explore new options in the world of circuit design. One approach that seems to be very promising is the famous energy-recovering (adiabatic) logic. Adiabatic circuits pursue low energy dissipation by restricting the current to flow across devices with low voltage drop and by recycling the energy stored in the capacitors. The energy consumption is analyzed by variation of parameters. In the analysis, two logic families, ECRL (Efficient Charge Recovery Logic) and PFAL (Positive Feedback Adiabatic Logic) are compared with conventional CMOS logic for inverter and 2:1 multiplexer circuit and Ring counter. The results show that adiabatic technique is a good choice for low power and low area application in specified frequency range.

Keywords – **Adiabatic, Efficient Charge Recovery Logic, Multiplexer, Positive Feedback Adiabatic Logic, Ring Counter**

I. INTRODUCTION

The explosive growth in laptop and portable systems and in cellular networks has intensified the research efforts in low power microelectronics. Today there is an ever-increasing number of portable applications requiring low power and high throughput than ever before. For example, notebook and laptop computers, representing the fastest growing segment of the computer industry, are demanding the same computation capabilities as found in desktop machines. Equally demanding are developments in personal communication services (PCS's), such as the current generation of digital cellular telephony networks which employ complex speech compression algorithms and sophisticated radio modems in a pocket sized device. Even more dramatic are the proposed future PCS applications, with universal portable multimedia access supporting full motion digital video and control via speech recognition [1].

Thus, designing low-power digital systems especially the processor is becoming equally important to designing a high performance one. Fully adiabatic operation of a circuit is an ideal condition. It may be only achieved with very slow switching speed. In practical cases, energy dissipation with a charge transfer event is composed of an adiabatic component and a non-adiabatic component

II. DISSIPATION MECHANISMS IN ADIABATIC LOGIC CIRCUITS:

Fig.1 shows the equivalent circuit used to model the conventional CMOS circuits during charging process of the output load capacitance. But here constant voltage source is replaced with the constant current source to charge and discharge the output load capacitance. Here R is on resistance of the PMOS network, CL is the load capacitance [1].

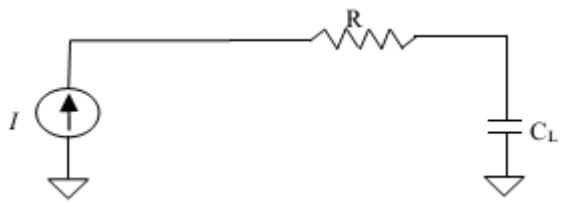


Figure-1

Energy dissipation in resistance R is

$$E_{diss} = I^2.R.T = \left(\frac{C_L V_{DD}}{T}\right)^2 .R.T = \left(\frac{RC_L}{T}\right).C_L V_{DD}^2$$

Since E_{diss} depends upon R, by reducing the on resistance of PMOS network, the energy

dissipation can be minimized. The on resistance of the MOSFET is given by the first order approximation

$$R = \left[\mu C_{OX}\frac{W}{L}(V_{GS} - V_{th})\right]^{-1}$$

The energy stored at output can be retrieved by reversing the current source direction during discharging process instead of dissipation in NMOS network. Hence adiabatic switching technique offers less energy dissipation in PMOS network and reuses the stored energy in the output load capacitance by reversing the current source direction.

III. ADIABATIC LOGIC FAMILIES:

Many adiabatic logic design techniques are given in literature, but here two of them are chosen-ECRL [10] and PFAL [11]. These techniques show that there is good improvement in energy dissipation and are mostly used as reference in new logic families.

a) Efficient Charge Recovery Logic (ECRL) : INVERTER GATE DESIGN USING ECRL:

The schematic and simulated waveform of the ECRL inverter gate is shown in figure-2 and figure-a. Initially, input 'in' is high and input '/in' is low and power clock (pck) rises from zero to VDD and F is at output (out) remains at ground level, output '/out' follows the pck.

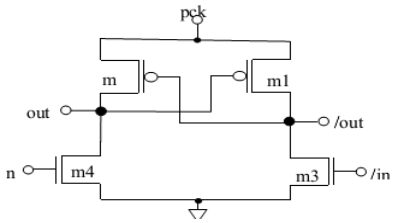


Figure-2

The output values can be used for next stage as inputs. Now pck falls from VDD to zero, '/out' returns its energy to pck due to which delivered charge is recovered. ECRL uses four phase clocking technique to efficiently recover the charge delivered by pck. When pck reaches at VDD, outputs (out) and (/out) hold logic values zero and VDD respectively.

2:1 MUX DESIGN USING ECRL

The schematic of the ECRL 2:1 Multiplexer is shown in figure-3 and figure-b respectively. If select input 's' is high and power clock (pck) rises from zero to VDD, then the output 'out' will select input 'b'.

If select input 's' is low and power clock (pck) rises from zero to VDD, then the output (out) will select the input 'a'. When pck reaches at VDD, outputs (out) and (/out) hold logic values. This output values can be used for the next stage as inputs. If pck falls from VDD to zero, high outputs return its energy to pck thereby delivered charge is recovered.

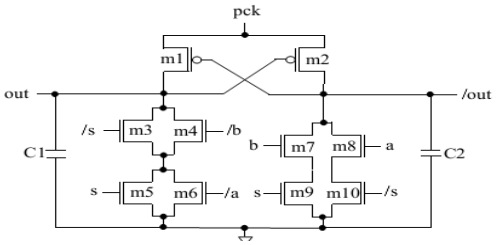


Figure-3

b) Positive Feedback Adiabatic Logic (PFAL)

INVERTER DESIGN: The schematic of PFAL inverter gate is shown in figure-4 and figure-a respectively. Initially, if input 'in' is high and input '/in' is low and power clock (pck) rises from zero to VDD, then F and m4 are at output (out) remains at ground level, output '/out' follows the pck.

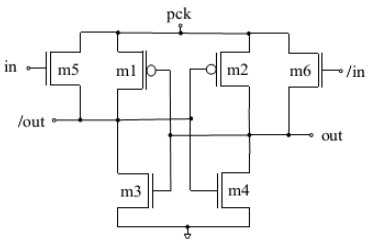


Figure-4

When pck reaches at VDD, outputs 'out' and '/out' hold logic values zero and VDD respectively. These output values can be used for the next stage as inputs. If pck falls from VDD to zero, '/out' returns its energy to pck thereby delivered charge is recovered. PFAL uses four phase clocking technique to recover the charge delivered by pck efficiently.

2:1 MUX DESIGN USING PFAL

The schematic of the PFAL 2:1 Multiplexer is shown in figure-5 and figure-b. If select input 's' is high and power clock (pck) rises from zero to VDD, then output 'out' will select the input 'b'. If select input 's' is low and power clock (pck) rises from zero to VDD, output 'out' will select the input 'a'. When pck reaches at VDD, outputs 'out' and '/out' hold logic values.

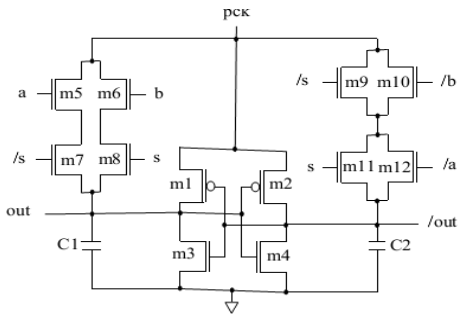


Figure-5

This output values can be used as inputs for the next stage. If pck falls from VDD to zero, high outputs return the energy to pck and hence delivered charge is recovered.

IV. RING COUNTER

A ring counter is a type of counter composed of a circular shift register. The output of the last shift register is fed to the input of the first register.

- A straight ring counter or Over beck counter connects the output of the last shift register to the first shift register input and circulates a single one (or zero) bit around the ring. For example, in a 4-register one-hot counter, with initial register values of 1000, the repeating pattern is: 1000, 0100, 0010, 0001, 1000... . Note that one of the registers must be pre-loaded with a 1 or 0 in order to operate properly. In the study provision is made for loading data into the parallel-in/ serial-out shift register configured as a ring counter. Any random pattern may be loaded. The generally useful pattern is single 1.

RING COUNTER USING ECRL:

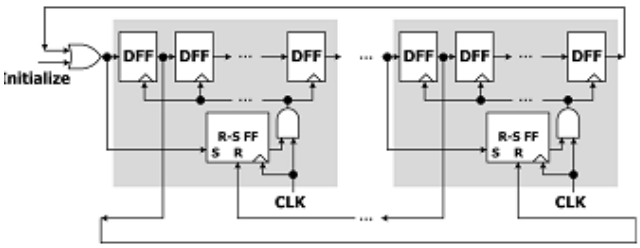


Figure-6

The above block diagram shows the power controlled Ring counter. First, the total block is divided into two sub blocks and each block contains one SR FLIPFLOP controller.

RING COUNTER USING PFAL:

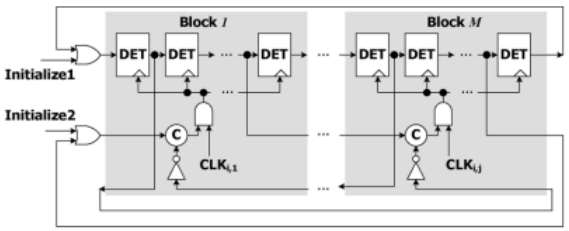


Figure-7

DET: (Double edge triggered flip-flops): Double-edge-triggered (DET) flip flops are utilized to reduce the operating frequency by half. The logic construction of a double-edge-triggered (DET) flip-flop, which can receives input signals at two levels of the clock, is analyzed and a new circuit is designed namely CMOS DET. In this paper, we propose to use double-edge-triggered (DET) flip flops instead of traditional DFFs in the ring counter to halve the operating clock frequency. Double edge-triggered flip flops are becoming a popular technique for low-power designs since they effectively reduce the clock frequency by half. The paper by Hossain et al[1] showed that

while a single-edge triggered flip flop can be implemented by two transparent latches in series, a double edge-triggered flip-flop can be implemented by two transparent latches in parallel; the circuit in Fig. 1 was given for the static flip flop implementation.

V. C ELEMENT:

A conclusion section must be included and should indicate clearly the advantages, limitations, and possible applications of the paper. Although a conclusion may review the main points of the paper, do not replicate the abstract as the conclusion. A conclusion might elaborate on the importance of the work or suggest applications and extensions.

VI. CONCLUSION

The Muller C-element, or Muller C-gate, is a commonly used asynchronous logic component originally designed by David E. Muller. It performs logical operations on the inputs and has hysteresis. The output of the C-element reflects the inputs when the states of all inputs match. The output remains in this state until the inputs all transition to the other state.

This model can be extended to the Asymmetric C-element where some inputs only effect the operation in one of the transitions (positive or negative). The figure shows the gate-level and transistor-level implementations and symbol of the C-element.

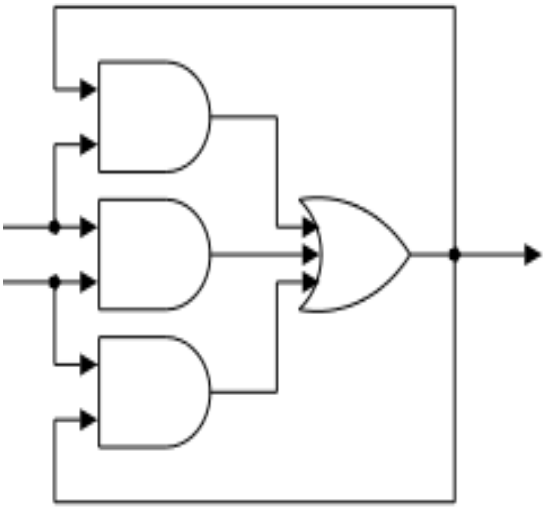


Figure-8

VII. SIMULATION RESULTS:

FIGURE-A: INVERTER

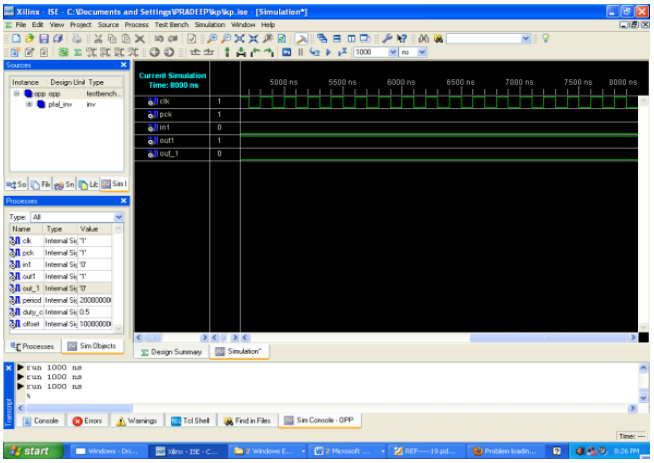


FIGURE-B: MULTIPLEXER:

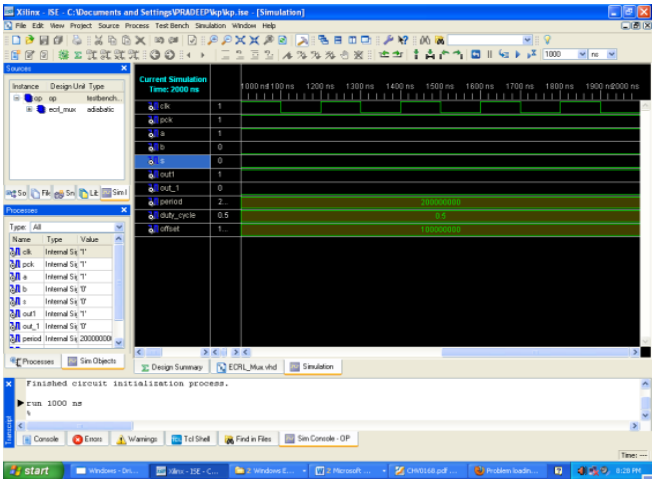
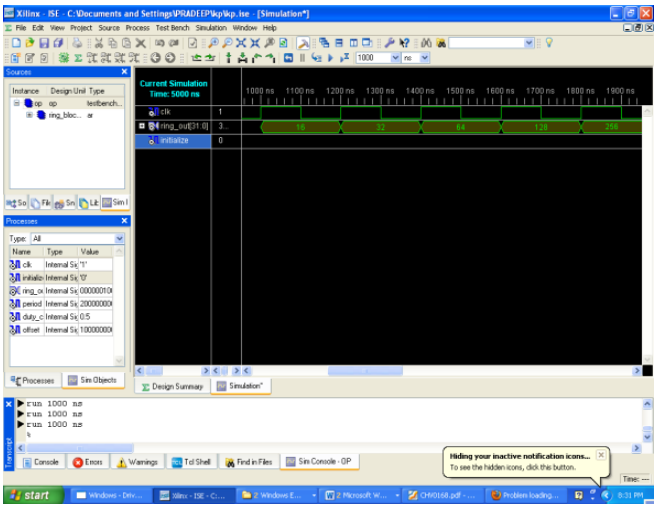


FIGURE-C: RING COUNTER:



VIII. SYNTHESIS REPORT:

TARGET DEVICE : XC4VLX15-12-FF676SION

Component	ECRL		PFAL	
	Area (GC)	Power (mw)	Area (GC)	Power (mw)
Inverter	145	239	120	225
Multiplexer	269	268	241	213
Ring counter	358	447	298	435

IX. CONCLUSION

Up to 200MHz adiabatic logic presents an alternative to conventional static CMOS for the realization of low-energy electronics. By means of inverter, multiplexer, ring counter, different adiabatic logic families have been compared with respect to energy consumption, area occupation and frequency range. At f=1MHz, PFAL and 2N-2N2P implementations reduce energy dissipation by a factor of 10, ECRL by a factor of 5.1 compared to a standard static components. The influence of the supply voltage scaling on the energy dissipation was also investigated. For adiabatic component a reduction of the dissipated energy could also be observed. At VDD = 1.2V, adiabatic adders still dissipate between 2.9 and 5.7 times less than the standard CMOS implementation. The sensitivity to technological parameter fluctuations and the dependency of energy dissipation on inter-die (global) and intra-die (local) threshold voltage variations have been characterized. For local threshold voltage variations, there is no compensation effect in case of statistical variations, as it occurs in static CMOS circuits.

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