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Power Quality Enhancement Based on Multilevel STATCOM for High Power Applications

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***Abstract*— A multilevel static compensator (STATCOM) based on cascaded two level inverter is proposed in this paper. The main aim is reactive power compensation with improved power quality.The cascaded two level inverter based topology has better utilization of dc link voltage and low harmonic content. It includes two conventional three phase two level inverters connected in cascade through a three phase transformer. The cascaded inverter uses 12-sided polygonal voltage space vectors. To realize 12-sided polygonal voltage space vectors, the dc link voltage of inverter-2 must be maintained at 0.366 times dc link voltage of inverter-1. The dc-link voltages of the inverters are regulated at asymmetrical levels to achieve four-level operation. In high power applications, VAR compensation is achieved using multi-level inverters. The intention of this study was to mitigate voltage sag problem using proposed STATCOM along two controlling methods namely FIS(Fuzzy inference system) and PI.Simulation studies are carried out to predict the system performance. A laboratory prototype is also developed to validate the results obtained by simulation.The performance of the scheme is analyzed through MATLAB/SIMULINK.**

Keywords*— DC-Link Voltage Balance, Multilevel Inverter, Power Quality (PQ), Static Compensator (STATCOM).

I. INTRODUCTION

Power Generation and Transmission is a complex procedure, requiring the working of many components of the power system in tandem to maximize the output. One of the main components to form a key part is the reactive power in the system. It is required to maintain the voltage to distribute the active power through the lines. Loads like motor loads and other loads require reactive power for their operation. To improve the performance of ac power systems, we have to control this reactive power in an efficient way and this is known as reactive power compensation. There are two aspects to the problem of reactive power compensation: load compensation and voltage support. Load compensation consists of improvement in power factor, balancing of real power drawn from the supply, better voltage regulation, etc. of large fluctuating loads. Voltage support consists of reduction of voltage fluctuation at a given terminal of the transmission line. Two types of compensation can be used: series and shunt compensation. These modify the parameters of the system to give enhanced reactive power compensation. In recent years, static VAR compensators like the STATCOM have been developed. These quite acceptably do the job of absorbing or generating reactive power with a faster time response and come under Flexible AC Transmission Systems (FACTS). This allows an increase in transfer of apparent power through a transmission line, and much improved stability by the adjustment of parameters that rule the power system i.e. current, voltage, phase angle, frequency and impedance. When ac loads are fed through inverters it is required that the output voltage of desired magnitude and frequency should be achieved. A variable output voltage can be obtained by varying the input dc voltage and maintaining the gain of the inverter constant. Alternatively, if the dc input voltage is fixed and it is not controllable, a variable output voltage can be obtained by varying the gain of the inverter, which is normally accomplished by pulse-width-modulation (PWM) technique within the inverter.

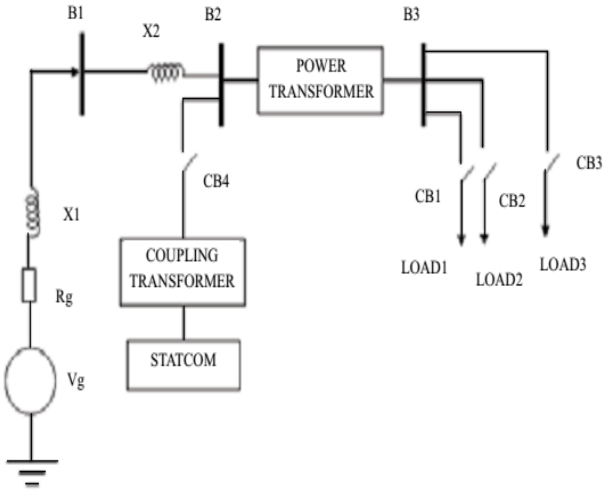

Fig. 1.Single line diagram representing STATCOM.

The inverters which produce which produce an output voltage or a current with levels either 0 or $\pm V$ are known astwo level inverters. In high-power and high-voltage applications these two-level inverters however have some limitations in operating at high frequency mainly due to switching losses and constraints of device rating. This is where multilevel inverters are advantageous. Increasing the number of voltage levels in the inverter without requiring higher rating on individual devices can increase power rating. The unique structure of multilevel voltage source inverters' allows them to reach high voltages with low harmonics without the use of transformers or series-connected synchronized-switching devices. The harmonic content of the output voltage waveform decreases significantly.

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II. CASCADED TWO-LEVEL INVERTER-BASED MULTILEVEL STATCOM

The power system and STATCOM model is shown in Fig.2. This model represents the connection point of STATCOM in the power system

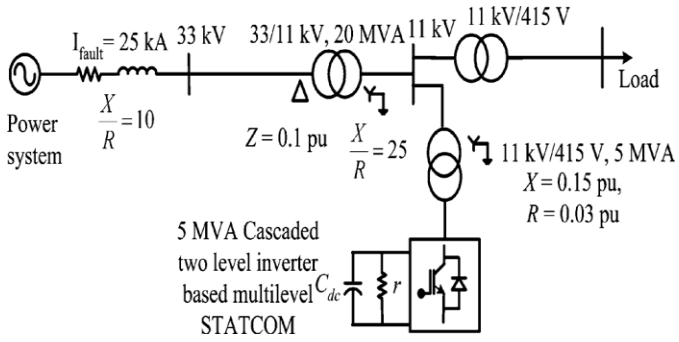

Fig. 2.Power system and the STATCOM model

The schematic diagram of cascaded two-level inverter based multi-level STATCOM is shown in Fig.3. In which the low-voltage (LV) side and high voltage (HV) side of a transformer is connected to inverter and transmission line respectively.

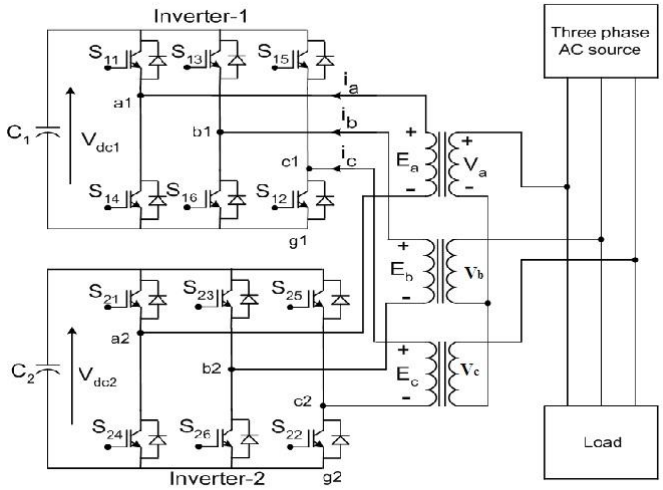

Fig. 3.Cascaded two-level inverter based STATCOM

From the Fig.3, the three phase RMS source voltages V_a' , $V_b'$and V_c' are referred to the low-voltage side of the transformer. The leakage inductances of low-voltage side windings of the transformer areL_a, L_b and $L_c$respectively. The transformer losses are represented in terms of resistances arer_a r_b and r_c respectively. The output voltages of inverter1 and inverter2 are $e_{a1}, e_{b1}, e_{c1}$and e_{a2}, e_{b2}, e_{c2}. Finally leakage resistances of dc-link capacitors $C_1$and$C_2$are $r_1$and$r_2$respectively.

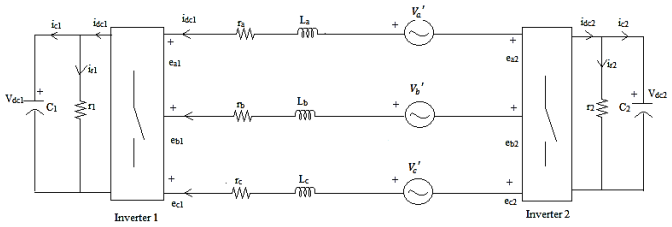

Fig. 4.Equivalent circuit of two-level inverter based STATCOM

A. *Phase Equivalent Circuit*

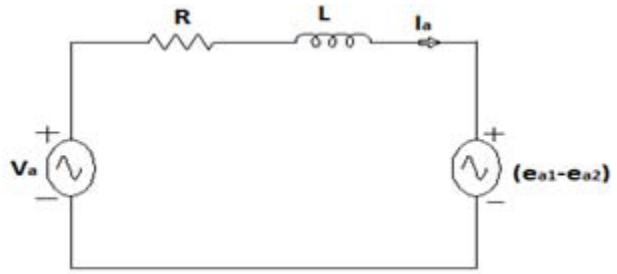

Fig. 5.Equivalent circuit of phase a

Equivalent circuit of phase "a" is shown in Fig.5. In the figure, the RMS source voltage is represented as v_a' total loss in the system is represented as R, the transformer winding leakage inductance is represented as L, the voltage across primary side of the transformer of inverter1 and inverter2 is$(e_{a1} - e_{a2})$.

Applying KVL to the loop

$$-v_a' + R_a I_a' + L_a \frac{di_a'}{dt} + (e_{a1} - e_{a2}) \qquad (1)$$

Similarly for b and c phases

$$-v_b' + R_b I_b' + L_b \frac{di_b'}{dt} + (e_{b1} - e_{b2}) = 0 \qquad (2)$$

$$-v_c' + R_c I_C' + L_c \frac{di_c'}{dt} + (e_{c1} - e_{c2}) \qquad (3)$$

By assuming resistances R_a= R_b= R_C= R and inductancesL_a= L_b=L_C= L, the above can be written in mathematical model form as,

$$\begin{bmatrix} \frac{di_a'}{dt} \\ \frac{di_b'}{dt} \\ \frac{di_c'}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-r}{L} & 0 & 0 \\ 0 & \frac{-r}{L} & 0 \\ 0 & 0 & \frac{-r}{L} \end{bmatrix} \begin{bmatrix} i_a' \\ i_b' \\ i_c' \end{bmatrix} + \frac{1}{L} \begin{bmatrix} V_a' & - & (e_a^1 & -e_a^2) \\ V_b' & - & (e_b^1 & - e_b^2) \\ V_c' & - & (e_c^1 & -e_c^2) \end{bmatrix} \qquad (4)$$

The equation (4) is known as mathematical model in the stationary reference form of cascaded two-level inverter based STATCOM. To control both the active and reactive currents independently, above stationary reference frame equations can be converted into rotating reference frame equations. The source voltage of q-component is set to be zero so that the source voltage of d-component can be align with the synchronously rotating reference frame.

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The dynamic model in the synchronously rotating reference frame is given as

$$\begin{bmatrix} \frac{di'_d}{dt} \\ \frac{di'_q}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-r}{L} & w \\ -w & \frac{-r}{L} \end{bmatrix} \begin{bmatrix} i'_d \\ i'_q \end{bmatrix} + \frac{1}{L} \begin{bmatrix} v'_d & (e_{d1} & - e_{d2}) \\ - & (e_{q1} & - e_{q2}) \end{bmatrix} \quad (5)$$

Here v'_drepresents the direct (d)-axis voltage component of ac source andi'_d, i'_qrepresents d-axis and q-axis current components of cascaded two-level inverter.

B. Control Strategy

The block diagram of control circuit is shown in Fig. 5. The d-axis and q-axis voltages can be controlled as follows

$$e_d^* = -x_1 + wLi'_q + v'_d \quad (6)$$

$$e_q^* = -x_1 - wLi'_d + v'_q \quad (7)$$

Where $e_d^*$and e_q^*represents d-axis and q- axis reference voltage components of the inverter. The parameters x_1 and x_2 are known as control parameters and these can controlled as

$$x_2 = \left(k_{p1} + \frac{k_{i1}}{s}\right)(i_d^* + i'_d) \quad (8)$$

$$x_2 = \left(k_{p2} + \frac{k_{i2}}{s}\right)(i_q^* + i'_q) \quad (9)$$

Where $i_d^*$is the direct (d)-axis reference current and is given by

$$i_d^* = \left(k_{p3} + \frac{k_{i3}}{s}\right)[(V_{dc1}^* + V_{dc2}^*) - (V_{dc1} - V_{dc2})] \quad (10)$$

WhereV_{dc1}^*andV_{dc2}^*represents the reference voltages of dc-link capacitors of inverter 1 and inverter2. The reference reactive current component i.e q-axis component i_q^* is obtained either from load, when used for load compensation or from voltage regulation loop when used in transmission lines.

Fig.6. Shows that the three phase voltages v_a, v_b, v_c are given to phase-locked loop (PLL) to generate the unit signals cos $\omega t$and sin ωt. Phase lock loop or phase locked loop (PLL) is a type of control system, which is used to generate output signal to match the phase of input signal. These unit signals are used to transform the converter currentsi'_a, i'_b, i'_c into synchronously rotating reference frame currents. So that it is easy to control reactive and active current components. These currents consist of large switching frequency ripples and which are eliminated by using low-pass filters (LPF). The reference voltages to the converter are e_d^*, $e_q^*$are generated from controller using $(V_{dc1}^* + V_{dc2}^*)$and i_q^*. The inverter supplies desired reactive component of current $i_q^*$and draws active component of current $i'_d$by considering these reference current components. Which can be further used to regulate total dc-link voltage $(V_{dc1}^* + V_{dc2}^*)$of the inverter.

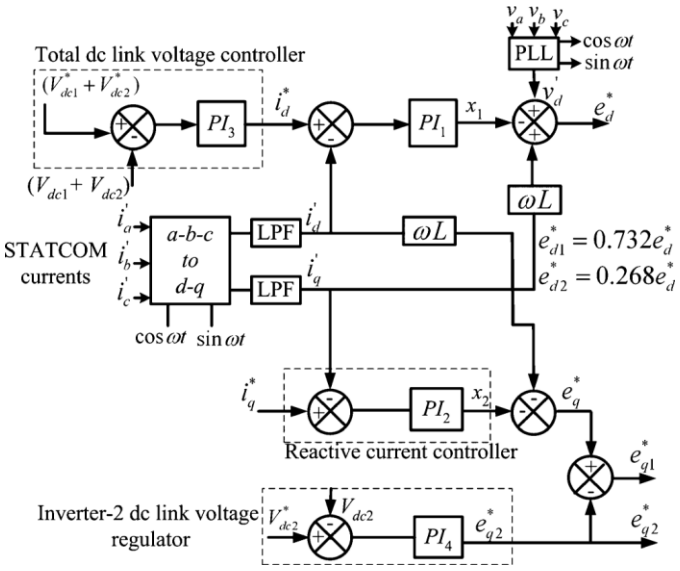

Fig. 6.Control circuit diagram

C. DC-LINK Balance Controller

The total dc-link balance controller is used to provide magnitude and phase of resultant voltage supplied by the cascaded inverter. The active power sharing between the inverter and grid is depends on angle δ.From the figure, the reference voltage components of q-axis of the two inverters e_{q1}^*, $e_{q2}^*$is obtained as

$$e_{q1}^* = e_q^* - e_{q2}^* \quad (11)$$

$$e_{q2}^* = \left(k_{p4} + \frac{k_{i4}}{s}\right)(V_{dc2}^* + V_{dc2}) \quad (12)$$

Where e_{q1}^*controls the inverter1 dc-link voltage, e_{q2}^*controls the inverter2 dc-link voltage. The dc-link voltage of inverter 2 is controlled at 0.366 times dc-link voltage of inverter 1, so four level operation is obtained and output voltage harmonic spectrum is improved. The inverter1 dc-link voltage and inverter2 dc-link voltage is expressed in terms of total dc-link (V_{dc}) voltage.

$$V_{dc1} = 0.732V_{dc} \quad (13)$$

$$V_{dc2} = 0.268V_{dc} \quad (14)$$

The power transfer to inverter1 is indirectly controlled and for inverter2, power transfer is directly controlled. Therefore inverter2 attain its reference value quickly when compared to inverter1. The control circuit uses the sinusoidal pulse width modulation (SPWM) technique to generate gate signals from the obtained reference voltages.

III. CASCADED H-BRIDGE MULTILEVEL INVERTER

The cascaded H-bridge multilevel Inverter uses separate dc sources (SDCSs). The multilevel inverter using cascaded-inverter with SDCSs synthesizes a desired voltage from several independent sources of dc voltages, which may be obtained from either batteries, fuel cells, or solar cells. This configuration recently becomes very popular in ac power supply and adjustable speed drive applications. This new

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inverter can avoid extra clamping diodes or voltage balancing capacitors. Again, the cascaded multilevel inverters are classified depending the type of DC sources used throughout the input. A single-phase structure of an m-level cascaded inverter is each separate dc source (SDCS) is connected to a single-phase full-bridge, or H-bridge, inverter. Each inverter level can generate three different voltage outputs, $+V_{dc}$, 0, and $-V_{dc}$by connecting the dc source to the ac output by different combinations of the four switches, S_1, S_2, S_3, and S_4. To obtain $+V_{dc}$, switches $S_1$and $S_4$are turned on, whereas $-V_{dc}$can be obtained by turning on switches $S_2$and S_3. By turning on $S_1$and S_2or $S_3$and S_4, the output voltage is 0. The ac outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs as shown in Fig.6. One more alternative for a multilevel inverter is the cascaded multilevel inverter or series H-bridge inverter. The series H-bridge inverter appeared in 1975. Cascaded multilevel inverter was not fully realized until two researchers, Lai and Peng. They patented it and presented its various advantages in 1997. Since then, the CMI has been utilized in a wide range of applications. With its modularity and flexibility, the CMI shows superiority in high-power applications, especially shunt and series connected FACTS controllers.The CMI synthesizes its output nearly sinusoidal voltage waveforms by combining many isolated voltage levels. By adding more H-bridge converters, the amount of Var can simply increased without redesign the power stage, and build-in redundancy against individual H-bridge converter failure can be realized. A series of single-phase full bridges makes up a phase for the inverter.A three-phase CMI topology is essentially composed of three identical phase legs of the series-chain of H-bridge converters, which can possibly generate different output voltage waveforms and offers the potential for AC system phase-balancing.This feature is impossible in other VSC topologies utilizing a common DC link. Since this topology consists of series power conversion cells, the voltage and power level may be easily scaled. The dc link supply for each full bridge

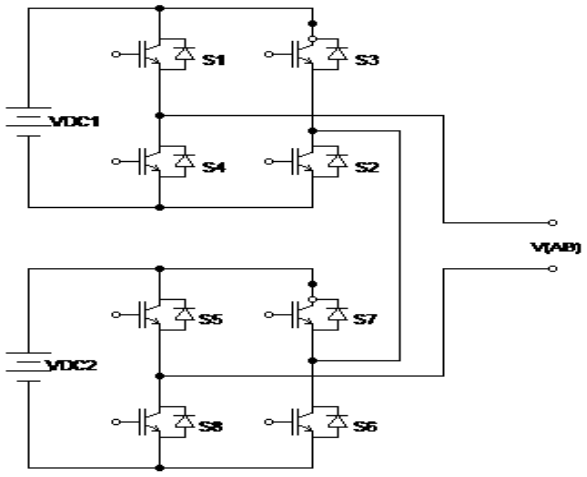

Fig.7. CHB inverter

converter is provided separately, and this is typically achieved using diode rectifiers fed from isolated secondary windings of a three-phase transformer. Phase-shifted transformers can supply the cells in medium-voltage systems in order to provide high power quality at the utility connection.

IV. FUZZY LOGIC CONTROLLER

The control system is based on fuzzy logic. Fuzzy logic controller is a one type non linear controller and automatic. This type of the control approaching the human reasoning that makes the use of the acceptance, uncertainty, imprecision and fuzziness in the decision-making process, manages to offer a very satisfactory performance, without the need of a detailed mathematical model of the system, just by incorporating the experts' knowledge into the fuzzy. Fig 5 shows the fuzzy logic controller block diagram. The fuzzy logic control system is based on the MAMDHANI fuzzy model. This system consists of four main parts. First, by using the input membership functions, inputs are fuzzified then based on rule bases and the interfacing system, outputs are produced and finally the fuzzy outputs are defuzzifiedand they are applied to the main control system. Error of inputs from their references and error deviations in any time interval are chosen as MATLAB. The output of fuzzy controller is the value that should be added to the prior output to produce new reference output as shown in Figs.8 to 9.

Fig.8. selection of input and output variables.

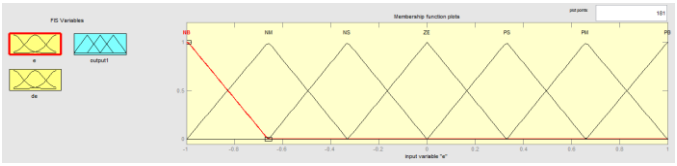

Fig.9. Input1 membership function

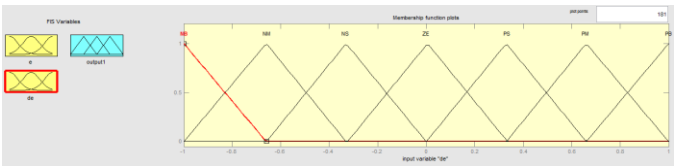

Fig.9. Input2 membership function.

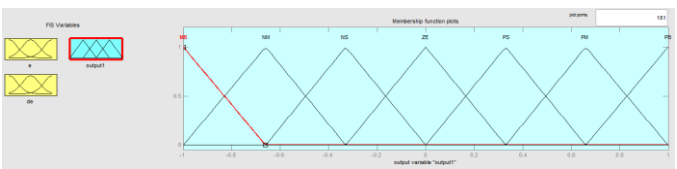

Fig.10. Output membership function

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TABLE I
SYSTEM PARAMETERS

PARAMETERS	Values
Rated power	5MVA
Transformer voltage rating	11KV/400
AC supply frequency,f	50Hz
Inverter-1 dc link voltage, Vdc1	659 V
Inverter-2 dc link voltage, Vdc2	241 V
Transformer leakage reactance, X_l	15%
Transformer resistance, R	3%
DC link capacitances, C1, C2	50 mF
Switching frequency	1200 Hz

V. SIMULATION RESULTS

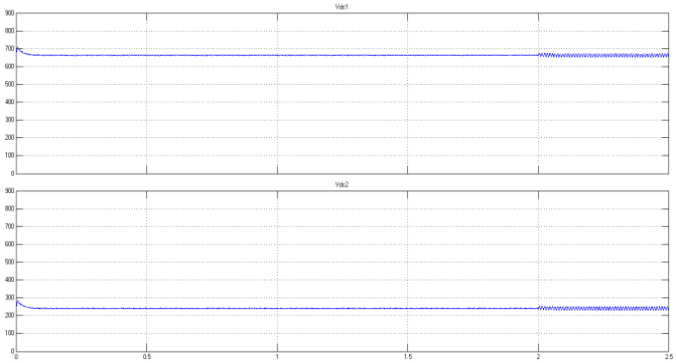

Fig. 8. DC-link voltages of two inverters

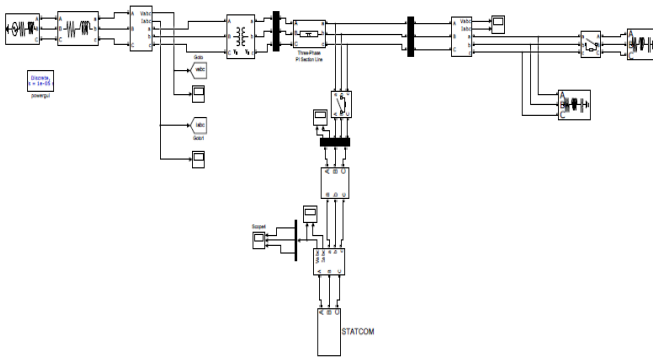

Fig. 9.Simulink model of Cascaded two-level inverter-based multilevel STATCOM

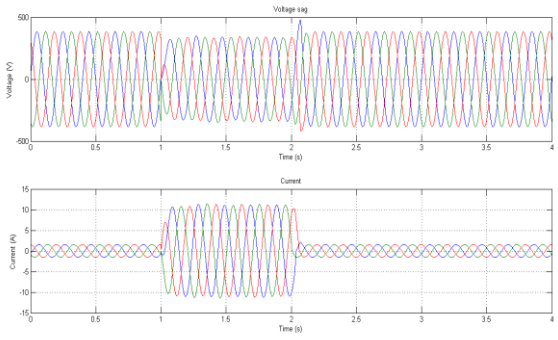

Fig. 10. Voltage and Current during sag condition.

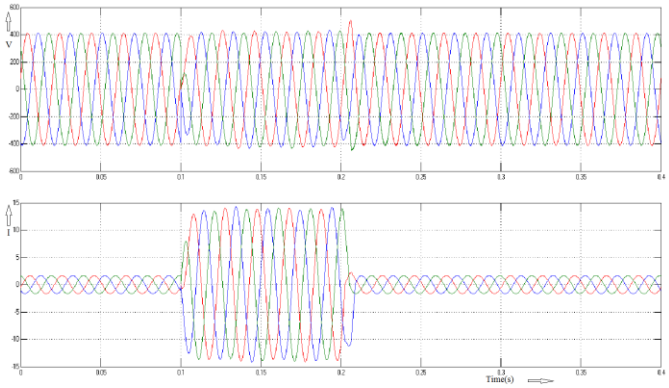

Fig. 11.Voltage compensation and corresponding current.

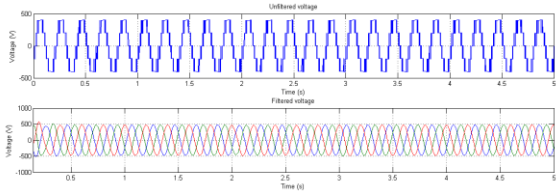

Fig. 12.Five Level Output Voltage

Fig.12 shows the Five Level Output Voltage of 5-Level Cascaded Based Multilevel Statcom.

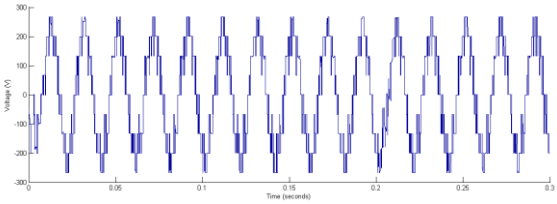

Fig. 13. 7-Level Output Voltage

Fig.13 shows the 7-Level Output Voltage of -7 Level Cascaded Based Multilevel Statcom

TABLE II
SUMMARY OF THD VALUES

S.No	THD
Without STATCOM	11.23%
With two Level STATCOM	4.73%
With 5-Level STATCOM	2.75%
With 7-Level STATCOM	151%

VI. CONCLUSION

In this paper, a multilevel STATCOM based on cascadedtwo level inverter is proposed. The cascaded inverter uses12-sided polygonal voltage space vectors. Using 12-sided polygonal voltage space vectors, dc bus utilization is increasedand better THD is obtained at high values of modulationindex. The dc link voltage of inverter-2 must be maintained at0.366 times dc link voltage of inverter-1 to obtain polygonalvoltage space vectors. A simple control strategy for reactive power compensation as well as to maintain dc link voltagesat the required levels is proposed. This control strategy isverified with simulation studies. Experimental results are alsopresented to validate the simulation results.DC-link

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voltage balance is one of the major issues in cascaded inverter-based STATCOMs. In this paper, a simple var compensating scheme is proposed for a cascaded two-level inverter-based multilevel inverter. The scheme ensures regulation of dc-link voltages of inverters at asymmetrical levels and reactive power compensation. The performance of the scheme is validated by simulation and experimentations under balanced an unbalanced voltage conditions.

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