

Power Supply Noise Rejection Circuit using Active Inductor and Active Capacitor in Mixed Signal Systems

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Abstract- System integrity is emerging as an important issue as very large scale integration (VLSI) technology advances to nanoscale regime. This rise to system-on-chip (SoC) concept, due to this several systems is included such as rf, optical, etc. In mixed-signal system, both analog and digital circuits are being integrated in to a same chip. In this case power-supply noise is a significant problem in mixed-signal systems on a chip. This is due to the impulse like currents drawn by the CMOS gates during transitions cause noise in the sensitive analog circuits via power supply/ground (PG) and substrate. These unwanted variations in PG network is found to be most dominant source of substrate noise currents injected into the substrate. The switching noise generated by the CMOS gates also couple into sensitive analog blocks via the bonding wires and the shared PG buses. A noise-localization technique using on-chip active inductors along with an active decoupling capacitance using nmos is proposed. This would make the noise current generated by the digital gates to remain local in the region of the digital gates as well as reduction in the area of the circuit. This active inductor and active capacitor is designed using GDPK 90nm and 45nm CMOS technology.

Index Terms — Mixed-signal, System-On-Chip (SoC), Power-supply noise, Active inductors, Active Capacitor, CMOS inductance circuit, inductor simulation.

I. INTRODUCTION

CMOS technology has continuously evolved toward smaller feature sizes, allowing more electronic circuits to be integrated on a single silicon die. Hence, more complex circuits can be implemented on the same silicon area if replacing one technology with a newer. Now a day it is possible to implement very large subsystems or even a complete system on a chip (SoC). A SoC have many advantages compared with systems implemented in several integrated circuits (ICs). In such systems, circuits such as amplifiers, filters, digital-to-analog and analog-to-digital converters and high speed processing elements share the same silicon die in a SoC implementation. In such systems-on-a-chip (SoCs), power supply noise is an increasingly significant issue, which can lead to reduction in resolution for data converter and increased phase noise in voltage-controlled oscillators (VCOs) [1], [2] and [3].

In this paper, an attempt to manage the switching transients generated by digital CMOS gates by localizing them in the same region of their origin [9], thus preventing them from coupling to other analog systems on the same substrate.

Fig.1. illustrates how switching transient currents flow through the PG buses. In Figure 1(a), during the output pull-up operation in a typical CMOS gate (inverter is chosen for illustration) the transient impulse current is drawn from the supply bus which then continues to flow through the ground bus. This impulse-like current flowing through the ground bus causes ground bounce, which affects the analog blocks on the same substrate.

This variation injects current into the substrate through the p substrate [4] & [5]. The pull-down operation [Figure 1(b)] is a local phenomenon where the load capacitance is simply discharged, without affecting the power and ground buses.

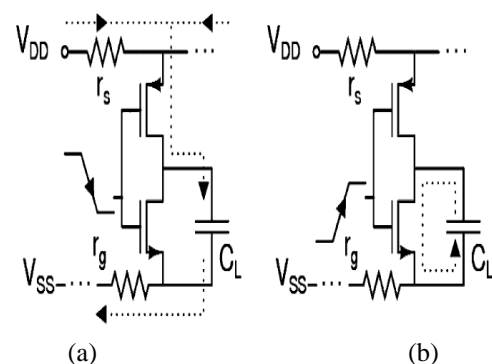


Fig.1. Supply current flow during the output pull-up and pull-down operation in digital CMOS gates.

Section II describes the various active inductor topologies. Section III describes the proposed active inductor circuit [1] which reduces the power supply noise, and the section IV describes the simulation results and analyses. Section V concludes the paper.

II. ACTIVE INDUCTOR TOPOLOGIES

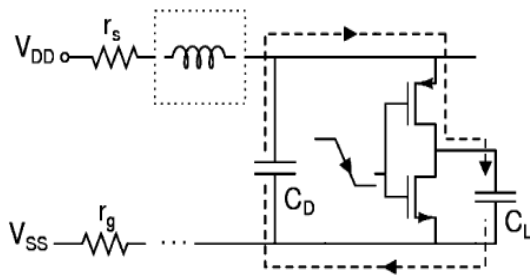


Fig. 2. Localization of the supply transients by using an inductor and capacitor [1]

Fig. 2. Illustrates the use of an inductor to provide high impedance for the higher frequency components contained in the impulse-like current so that these do not flow in the power-supply bus. It is necessary to provide low impedance for these transients to flow via the decoupling capacitor. This is a well-known and commonly employed technique for reducing the supply noise in PC boards. If only decoupling capacitors are used, the filtering is only partially effective, and a residual part of the noise always flows through the PG bus owing to its inherent low impedance. The series inductor should have low output impedance at low frequencies to act as a good dc voltage source [1].

As passive inductors require large chip area, active inductors are considered. Active inductors are popular in widely tunable VCOs [8] and tunable filters. The basic parameter required for those applications is a high-Q factor. Such an active inductor circuit is shown in Fig. 3. [1]. Assume standard reference directions for the port currents as flowing into the ports. It has an inverting trans-conductor consisting of M1 and a unity-gain current mirror (M3, M4) providing a current at the output port proportional to the voltage applied at the input port. The output port is loaded by a capacitor (C1). The non-inverting trans-conductor consists of a single transistor operating in the common-source configuration [1].

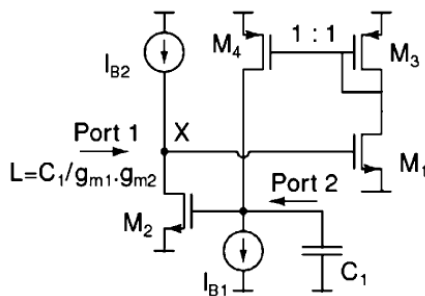


Fig. 3. Capacitor-loaded gyration circuit used to obtain a high-Q active inductor [1]

It converts the voltage across to a current and makes it flow at the input as shown. This realizes an inductor of value $C_1/g_{m1} \cdot g_{m2}$, where g_{m1} and g_{m2} are the small-signal transconductances of the transistors M1 and M2 respectively. The small output conductance at the two ports causes the Q to be finite but large. Both the value of the inductance L and the Q are dependent on the bias currents I_{B1} and I_{B2} flowing in the transistors M1 and M2, respectively. Such a high Q inductor would cause the system to be highly under-damped and thus cannot be used for decoupling as it would cause a lot of ringing on the power supply bus. A Q of 0.5 would lead to critical damping and the best settling [8]. Instead circuits with inherently low Q are proposed [1].

Fig. 4 shows a few possible inductor circuits which offer a low Q. The two transconductance needed for gyrators are obtained using two p-channel transistors M1 and M2. In high-Q inductors (Fig. 3), [1] both the transistors are in common-source configuration. Since one of the transconductance must be non-inverting, additional transistors (typically a current mirror) will be needed to do the inversion. In designing a low-Q inductor, we use one of the transistors in its common-gate configuration.

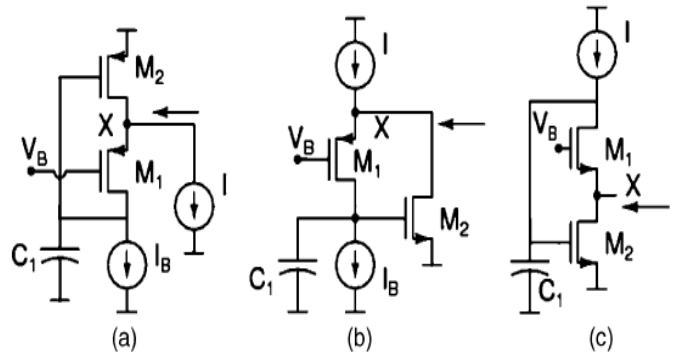


Fig. 4. Low-Q inductor realizations which could be used for localizing the impulse-like current from flowing into the supply buses [1]

This way, we can realize an inductor with just two devices. This makes the input impedance finite and causes the necessary low Q. All of the three circuits [Fig. 4(a)-(c)] have low input impedance owing to the transistor M1 operated in the common-gate configuration. All of them provide inductive behavior as each of the circuits act as a gyrator [7]. The voltage at node X (Fig. 4) is converted into a small-signal current by M1, which is then integrated by the capacitor C1, and, finally, a current proportional to the voltage across the capacitor is delivered back into node X by the transistor M2 operating in its common-source configuration.

Circuits in Fig. 4(a) and (b) require only small-voltage headroom to operate, which would typically be around 100 mV. The circuits in Fig. 4(b) and (c) are also not chosen because of a fixed current I flowing from the supply, even in the absence of any digital switching activity. The circuit in Fig. 4(c) has an added disadvantage in terms of a larger headroom requirement [1].

III. PROPOSED ACTIVE INDUCTOR

The circuit in Fig. 4(a) [1] supplies the current as demanded by digital gates and does not have a fixed rationed current I . In addition, the current I flows through the device M_2 as well. Note that this current varies as per the current demanded at the node X , thus minimizing static power dissipation. The circuit in Fig. 4(a) is the best choice for power-supply decoupling based on headroom and bias current requirements. Choosing an inductor topology based on noise attenuation will be discussed in the following sections. Let us analyze the circuit in Fig. 4(a) in some more detail. Here the noninverting transconductance is provided by the common-gate transistor M_1 , the inverting transconductance by the common-source transistor M_2 and the gyration by capacitor C_1 . Neglecting the output resistances of M_1 and M_2 , the inductive component of the input impedance can be written as

$$Z_{IN} = \frac{sC_1}{gm_1 gm_2} \quad (1)$$

where gm_1 and gm_2 are the transconductance of pMOS devices M_1 and M_2 , respectively. The inductor realized is directly proportional to the size of the capacitor C_1 used. C_1 is predominantly composed of the CGS of M_2 and any additional capacitor used at the output port II. M_2 is a relatively large device compared with M_1 , as it supplies the current demand of the digital gates. Contribution to C_1 by M_1 is comparatively small. The inductance is also inversely proportional to the product of both of the transconductances. This would mean, for a smaller bias current I_B , that a large inductor can be synthesized. It will be shown in simulation results that relatively large (few μH 's) of inductor can easily be synthesized.

The potential at node, which acts as the local power supply for a group of digital CMOS gates, by design is required to be as close to the global supply as possible. In the circuit in Fig. 4(a) [1], it is primarily set by the bias voltage V_B , whose generation is discussed later in this section. A source-drain voltage, enough to keep in the device M_2 in saturation, is required (100 mV). The device M_2 is responsible to deliver the current demanded by the digital blocks connected at node X . For minimum power overhead (1%), the device M_2 should deliver a current of about 100 times more than the static current I_B drawn by the inductor itself. For 1 μA of, the maximum current through the inductor would be 100 μA .

The two other important parameters of an inductor are its self-resonant frequency f_{SR} and Q . The self-resonant frequency (f_{SR}) is the frequency up to which the circuit has inductive impedance and beyond which it is capacitive. The self-resonant frequency can be written as

$$f_{SR} = \frac{1}{2\pi\sqrt{LC}} \quad (2)$$

Where, C is the parasitic capacitance at node X [1].

The Q of the active inductor can be written as follows (when seen as a parallel R-L-C) neglecting the output conductance of M_1 [7]:

$$Q = \frac{1}{\omega L(gm_1 + go_2)} \quad (3)$$

Where, gm_1 is transconductance of M_1 and go_2 is output conductance of M_2 . A loaded Q of 0.5 makes the system critically damped and thus would have a good settling behavior [1].

TABLE I

DEVICE SIZES FOR THE DECOUPLING INDUCTOR

| Device | Dimensions (W μm / L μm) |
|----------|---|
| M1 | 0.42/0.18 |
| M2 | 10/0.18 |
| M21 | 0.42/0.18 |
| M22 | 0.5/1.2 |
| M3,M4,M5 | 2/1 |

Table I shows the dimensions of the devices used to implement the proposed [1] active inductor used as the decoupling inductor to reduce the power supply noise.

IV. AREA EFFICIENT ACTIVE CAPACITOR

On-chip decoupling capacitors (decaps) are widely used to reduce power supply noise by placing them at the appropriate locations on the chip between blocks. While passive decaps can provide a certain degree of protection against IR drop, if a problem is found after the physical design is completed, it is difficult to implement a quick fix to the problem.

In (11), A modified active decap design is proposed for ASIC applications operating up to 1 GHz. Active Capacitor being introduced due to the fact that passive capacitor consumes area in μm but active capacitor consumes only in nm. Due to that the area of overall layout of the circuit reduced to a larger amount which is an important factor VLSI design.

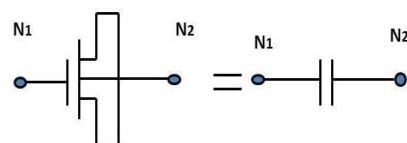


Fig.5. Equivalent Capacitance

Capacitance can be modelled using NMOS (nmoscap) by shorting drain and source (10) as given in Fig.5. The capacitance between gate and the source/drain is then

$$C_{Total} = C_{ox} = C_{ox}.W.L.(Scale)^2 \quad (4)$$

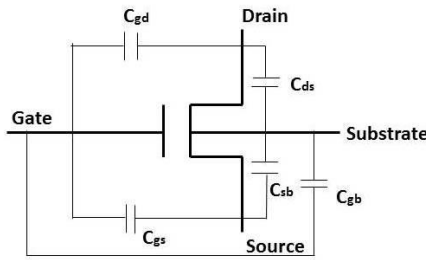


Fig.6.MOSFET Capacitance

The total capacitance from fig.6. comprises of following capacitance such as gate to source, gate to substrate connection and gate to drain given in equation (5),

$$C_{Total} = C_{gs} + C_{gb} + C_{gd} \quad (5)$$

V. SIMULATION RESULTS

To test the functionality of the active inductor, a test chip was fabricated by the GDPK foundry in 90nm and 45nm technology. Fig. 7. Shows the test setup to observe the functionality of the active inductor and the simulation is carried out using GPDK 90nm and 45nm CMOS devices. The bias current I_B is set as $1\mu A$, bias voltage V_B is set as $100mV$. The load current I_L and the noise current I_{ac} is set as $100\mu A$ and $5\mu A$ respectively. The value of the decoupling capacitor is $10\mu F$.

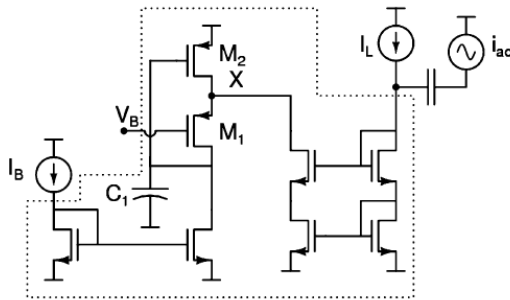


Fig. 7. Test setup to observe the functionality of the active inductor.

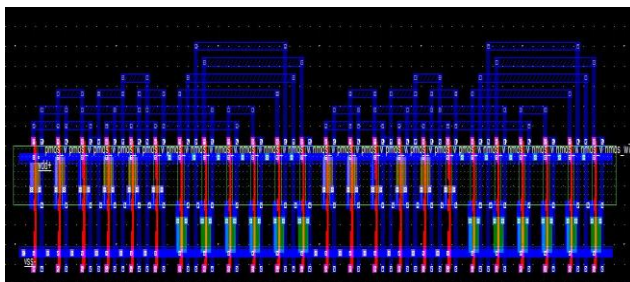


Fig. 8. Layout of the test set up circuit.

Fig.8. shows that the layout of the test set up circuit in 90nm CMOS technology in Cadence@Virtuoso Tool.

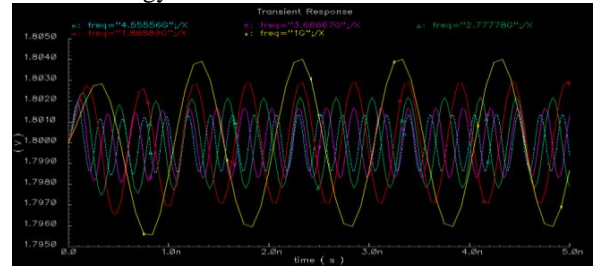


Fig.9. Variation of Noise Amplitude as frequency changes

Fig.9. shows that the noise amplitude changes as frequency level increases in GHZ, its value is shown in table II and its graph is represented as fig.10.

TABLE II
FREQUENCY VERSUS NOISE

| Frequency (GHz) | Average Noise Amplitude (μV) |
|-----------------|-------------------------------------|
| 1 | 5.890 |
| 3 | 1.770 |
| 5 | 1.764 |
| 7 | 1.290 |
| 9 | 0.010 |

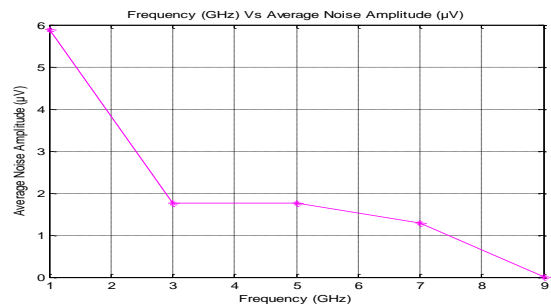


Fig.10. Representation of Noise Amplitude

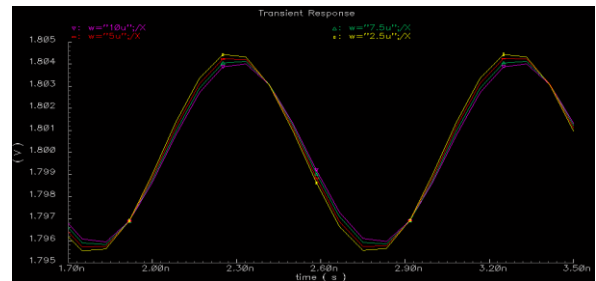


Fig.11. Dependency of Noise Amplitude with g_{m1}

Fig.11. shows the dependency of the noise amplitude with respect to the transconductance g_{m1} of the transistor M_1 . It shows that the amplitude of the noise is increases as the transconductance g_{m1} of the transistor M_1 increases. Fig.11. shows the dependency of the noise amplitude with respect to the transconductance g_{m2} of the transistor M_1 . It shows that the amplitude of the noise is increases as the transconductance g_{m2} of the transistor M_1 increases.

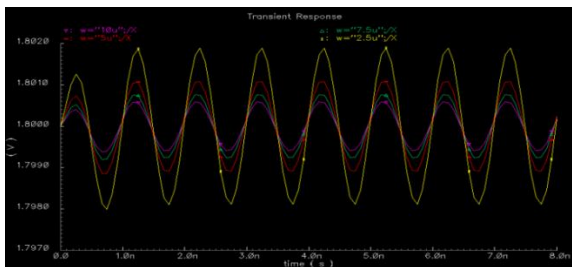


Fig.12. Dependency of Noise Amplitude with gm₂

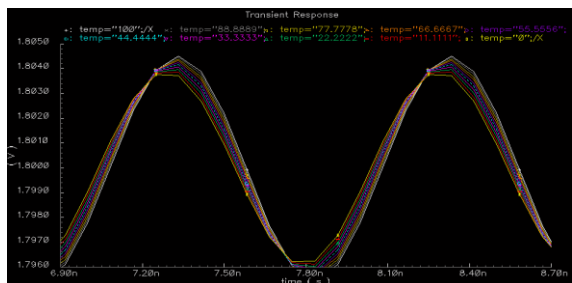


Fig.13. Dependency of Noise Amplitude with Temperature

Fig.13. shows the dependency of the noise amplitude with respect to the operating temperature. It shows that the amplitude of the noise is increases as the temperature increases and its values in table III.

TABLE III
TEMPERATURE VERSUS NOISE

| Temperature (Celsius) | Noise Amplitude (µV) |
|-----------------------|----------------------|
| 27 | 5.890 |
| 30 | 5.910 |
| 40 | 5.990 |
| 50 | 6.100 |
| 60 | 6.260 |
| 70 | 6.520 |
| 80 | 6.840 |
| 90 | 7.380 |
| 100 | 8.840 |

TABLE IV
POWER CONSUMPTION OF THE DECOUPLING INDUCTOR

| Temperature (Degree Celsius) | Power (µW) |
|------------------------------|------------|
| 27 | 327.599 |
| 30 | 328.554 |
| 40 | 331.764 |
| 50 | 334.984 |
| 60 | 338.240 |
| 70 | 342.512 |
| 80 | 344.809 |
| 90 | 348.127 |
| 100 | 351.469 |

Fig. 14. shows the variation of the power consumption with respect to the variation of operating temperature of the active decoupling inductor. The power consumption increases as the operating temperature of the active decoupling inductor increases.

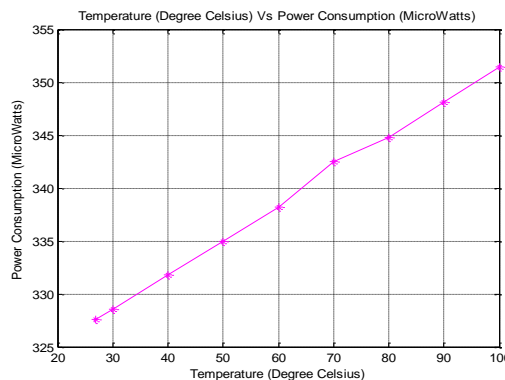


Fig. 14. Variation of Power Consumption with Temperature

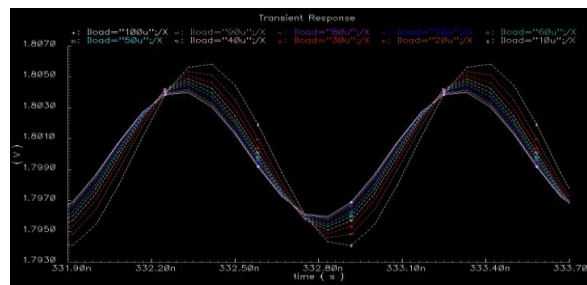


Fig.15. Dependency of Noise Amplitude with Load Current (I_{Load})

Fig.15. shows the dependency of the noise amplitude with respect to the load current which dc in nature. It shows that the amplitude of the noise decreases as the load current increases.

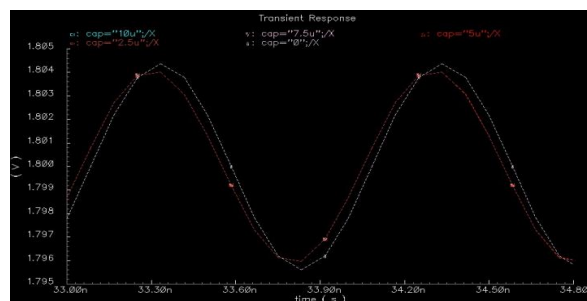


Fig.16. Dependency of Noise Amplitude with Decoupling Capacitor

Fig.16. shows the dependency of the noise amplitude with respect to the decoupling capacitor which is connected to the inductor. It shows that the amplitude of the noise decreases as the value of Decoupling Capacitor increases. But it doesn't have much impact on the inductance.

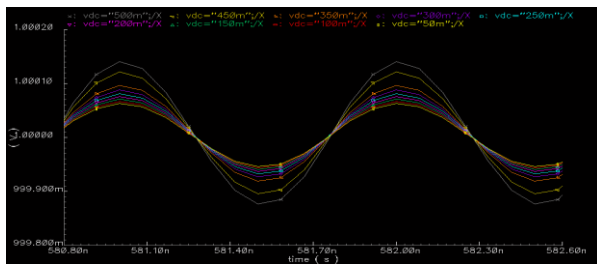


Fig.17. Dependency of Noise Amplitude with Bias Voltage

Fig. 17. shows the dependency of the noise amplitude with respect to the Bias Voltage VB. It shows that the amplitude of the noise increases as the Bias Voltage VB increases.

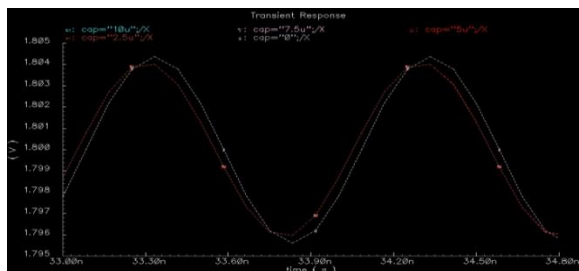


Fig. 18. Dependency of Noise Amplitude with Decoupling Capacitor

Fig. 18. shows the dependency of the noise amplitude with respect to the decoupling capacitor which is connected to the inductor. It shows that the amplitude of the noise decreases as the value of Decoupling Capacitor increases. But It doesn't have much impact on the inductance.

VI. CONCLUSION

Thus the simulation results from the test setup shows that the active inductor consumes very less power of 351.469 μ W when the temperature is 100 degree Celsius. The power supply noise is reduced by the active decoupling inductor as the frequency of the noise increases. The implementation of active capacitance in the circuit consumes area only in nm and not in μ m. The average value of the power supply noise at 1 GHz is 5.890 μ V and it reaches 10nV at 9 GHz. This shows that the proposed active decoupling inductor circuit works properly. The temperature dependency of the noise shows that it increases as the temperature increases. Hence the operating temperature of the active inductor should be maintained to get better power supply noise rejection.

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