

Privacy Preserving Throughput and Packet Classification for Network Efficiency

S. Thirumurugan, D. Suchitra, S. Neelavathi, R. Mary Antoinette
Computer Science and Engineering,
Christ College of Engineering and Technology Puducherry, India

Abstract— Packet classification is one of the core functions for performing efficient networking functionalities in network infrastructure. Most of the packet classification algorithms are based upon rulesets [14]. Rulesets must be independent in order to provide high throughput and low latency during packet classification. If the rulesets features are dependent it affects the performance of the network. In order to avoid these problems we proposed a packet classification technique which is rule set independent, and also provides routing and security functionalities. StrideBV algorithm is used for efficient packet classification [15] and we incorporate a bio-inspired algorithm called ACO for finding shortest path [13], to avoid congestion in the network. The transmitting packet is secured using HMAC algorithm [7]. The main aim is to maintain maximum lifetime of the network by increasing the throughput and avoid network congestion and minimized consumption of energy.

Keywords: Packet classification, network security, ACO, HMAC, packet latency, throughput.

I. INTRODUCTION

Secure networking becomes more crucial due to various attacks on networks. To protect networks from attacks various software tools and equipments were used. Packet classification is one of the processes used as the initial filter for classifying network traffic into flows based upon rulesets. Rulesets inspect the fields in packet header which compare the source IP address with destination IP address. The main problem with the hardware is that, packet classification engines require more space to store the

rulesets. To achieve this various techniques have been proposed but most of the techniques don't provide efficient memory management. For high-speed networking throughput and Quality of Service are the basic requirements. To provide both memory efficiency and high throughput in the same solution is difficult due to many reasons. Hence in this work we mainly concentrate on improving throughput and not mainly concern about memory efficiency. We present a packet classification scheme called StrideBV which tends to yield high throughput which is based upon field split algorithm. Using hardware chip FPGA we compare the performance of proposed with the existing work. We have inferred the ACO technique to different network models with various number of nodes and different structure to obtain the optimum throughput and to find out the shortest path. Various experiments have been carried out by differing the loads of the network. Here the network performance factor is taken by the reliability and throughput of the network. Even though the packets are classified efficiently, security issues should also be taken in concern. To increase the life time of the network, data has to be transmitted safely. In order to provide security to the network HMAC algorithm is used.

To summarize, we subsidize our work as follows:

- Packet classification is performed using strideBV method, which is rule set independent.
- To find the optimal path ACO algorithm is incorporated to increase the throughput of the network.

- For secure data transfer HMAC algorithm has been used for increasing life span of the network.

II. RELATED WORK

Many packet classification algorithms have been introduced in the past decade and can be found in [14]. Modular bit vector architecture for efficient packet classification was presented by Thilanga Gedara, Viktor K. Prasanna called strideBV which is rule set independent. The performance analysis of the proposed system is based on different configurations. FPGA has been used for packet classification in earlier stages which achieves 100G+ throughput on classifying a packet. But the proposed work is the first classification engine which yields 400G+ throughput, which is comparatively more efficient than all existing work [5]. Throughput of the network gradually decreases as the rule set size increases. Hence rule set independent features are adopted for better throughput. In this proposed work rules are represented as ternary string. For more efficiency range-to-prefix conversion has to be followed.

By experimenting various ant colony optimization techniques by Debasmita Mukherjee and Sriyankar Acharya they proposed various ant colony techniques called ACO1, ACO2 and ACO3 has been proposed and applied on various network standards and models. They compared the performance of each algorithm and a tabular list is maintained and collected to find the optimum solution. In their work reliability and throughput of the network is considered as the major performance factor.

The security is considered as the major issue in evaluating the performance of the network. Many techniques have been introduced in the past decade and one of the most efficient techniques is that HMAC which ensures message authentication and security. The technique is proposed by Marcio Juliato and Catherine Gebotys in which FPGA based HMAC technique is proposed and presented in this paper. The proposed system can attain 1.5 Gbps throughput. The energy consumption is found to be better by this proposed method. These methods are used to provide higher security levels for both mobile devices and servers which manage memory and speed efficiently.

III. EXISTING SYSTEM

In existing system a novel modular Bit-Vector architecture is proposed using range-to-prefix conversion which yields poor memory efficiency [9][3]. And in this work the main disadvantages are considered to be security and energy efficiency. Accuracy and security is very low in this network. Latency rate can be high when applying this technique to the larger network. The data that are transferred in this network is copied or hacked by some other network because of poor privacy of the network. This affects the lifetime and energy efficiency of the network.

IV. PROPOSED SYSTEM

The main aim of our project is to improve network lifetime by considering one of the basic network parameters called packet classification. Packet classification is done by FPGA based strideBV technique [6] which uses pipeline architecture for classifying the packets. Secondly the shortest and efficient path for transferring the packet is determined using ACO technique. Finally data in the network is secured using HMAC algorithm.

1. Packet classification using strideBV method:

The input packet header contains c bits which are matched to c bits of x bit rule which perform matching process independently. We can divide the x bit rule into x/c of c bits subfields. Input header is matched with x bit rule, every c bits of the input packet is matched with corresponding memory whose depth is 2^c . The input packet is undergone bitwise AND operation in a pipelined fashion and find the matching with the entire classifiers.

Algorithm 1:

Packet Classification Process.

Require: A x -bit packet header: $P_x-1 P_{x-1} \dots P_0$.

Require: $2k * x/c$, N bit-vectors:

$$A_{i,j} = B_{i,j}, N-1 B_{i,j}, N-2 B_{i,j}, 0,$$

$$i = 0, 1, \dots, x/c-1, \text{ and } j = 0, 1, \dots, 2^c-1$$

Require: A N bit-vector A_m to indicate match result

```

Ensure: N bit-vector Am
indicates all match results

1: Initialize Am: Am <- 11...1
All rules match initially

2: for i <- 0 to X = X/C - 1 { bit-
wise AND }
3: j = [Pi * C : P(i+1) * C]

4: Am <- Am AND Ai,j

5: endfor

```

2. Finding shortest path using ACO

We have inferred the ant colony optimization technique to different network models with various numbers of node and different structure to obtain the optimum throughput and to find out the shortest path. Various experiments have been carried out by differing the load of the network. Here the network performance factor is taken by the reliability and the throughput of the network. Routing protocols are used to calculate, choose and select the appropriate path in order to transfer the packet from source to destination more efficiently. There exist more number of routing algorithms in order to find the shortest path and thus to increase the network throughput. This is a routing algorithm proposed and applied to big network structure with the heavy load. This algorithm selects the path of data packet probably guided by the shortest path. The aim of all network routing algorithms is to reduce the congestion during packet transfer from source to destination thereby maximizing the performance of network. The performance could be measured by the throughput (i.e. the number of bits delivered per unit time) and the amount of data packets reached at the destination i.e. the reliability of the network. The ant selects the nodes randomly at the initial state by getting the information from the routing table. The ants which have successfully reached the destination update the pheromone secretion at the edges visited.

```

Algorithm 2: Finding shortest path Procedure ACO
(source, destination)
{
    assign initial positions to a set of
    packets at the given source; while (source
    != destination)
    {
        call findnextnode(source);

        set newsource =
        selectednode; source
        = newsource;
    }

    update the pheromone table using
    the paths selected by the successful packets;
    send a next set of packets guided by the
    information left by all the previous
    visitor packets;
}

Procedure findnextnode(source)
{
    Check the routing table
    entries corresponding to the source if a link
    exists with the source
    {
        If (the node is already visited)
        {
            Cancel the node;

            Else if (the node not already visited) {
                Mark the node as eligible
                for being selected
            }
        }

        Using the pheromone information,
        select a node from the list of eligible nodes;
        return the selected node;
    }
}

```

3. Ensuring security using HMAC:

The main reason for choosing the HMAC algorithm is that, we can use the hash functions without modifications. The hash function for HMAC code is freely and widely available. The main disadvantage of HMAC algorithm is that we can use and handle keys in a very simple way.

the XOR with $opad$ results in flipping one-half of the bits of m . Similarly, the XOR with $ipad$ results in flipping one-half of the bits of m , but a different set of bits. In effect, by passing l_i and l_o through the compression function of the hash algorithm, you have pseudo randomly generated two keys from m . HMAC should execute in approximately the same time as the embedded hash function for long messages. HMAC adds three executions of the hash compression function (for m_i , m_o , and the block produced from the inner hash).

3. The HMAC Algorithm

1. Append zeros to the left end of m to create a b -bit string m^+ (for example, if m is of length 160 bits and $b = 512$, then m will be appended with 44 zero bytes $0x00$).
2. XOR (bitwise exclusive OR) m^+ with $ipad$ to produce the b -bit block l_i .
3. Append M to l_i .
4. Apply H to the stream generated in Step 3.
5. XOR m^+ with $opad$ to produce the b -bit block l_o .
6. Append the hash result from Step 4 to l_o .
7. Apply H to the stream generated in Step 6 and output the result.

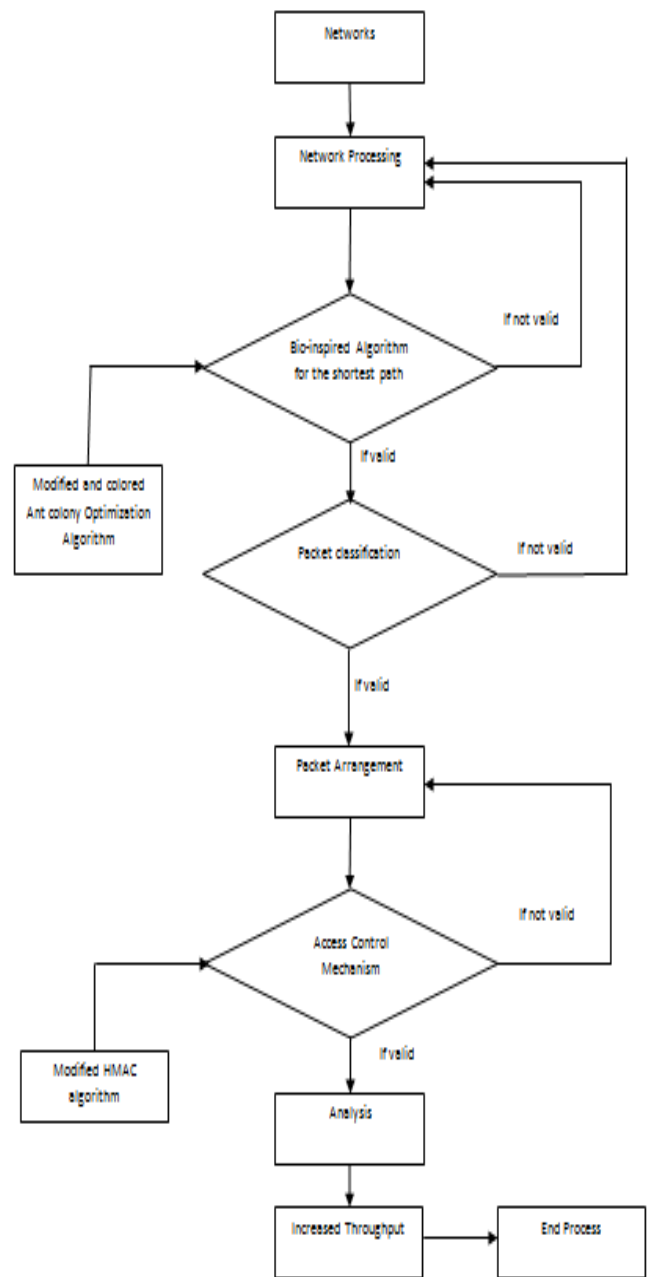


Fig: overall architecture of the process

V.CONCLUSION

We have conferred the modular architecture for high speed packet classification by using the field programmable gate array (FPGA). The throughput has been increased with the help of pipelined architecture but the memory efficiency has not been concentrated and which has to be employed in the future. The data control is the majorly focused and implemented criteria of this paper. Access control is not contemplated in our work. The clustering concept can be utilized for achieving the access control. In our work we have provided the better security with the assistance of HMAC algorithm. The optimal path is constructed using the dynamic algorithm and thereby increasing the throughput of the network.

REFERENCES

- [1] L. Bianchi, L.M. Gambardella, M. Dorigo (2010) "An ant colony optimization approaches to the probabilistic traveling salesman problem. In proceedings of PPSN-VII, seventh International conference on parallel problem solving from nature", Lecture notes in computer Science. Springer Verlag, Berlin, Germany, pp.883-892
- [2] I.D. Chakeres and E.M. Beldind-Royer. "The Utility of Hello Message for Determining Link connectivity in AODV protocol. In Proceedings of the 15th International Symposium on Wireless Personal Multimedia Communication (WPMC)", pages 505-508, Honolulu, Hawaii, October 2010.
- [3] M. Faezipour and M. Nourani, "Wire-Speed TCAM- Based Architectures for Multi-Match Packet Classification," IEEE Trans comput., vol.58, no.1, pp.5- 17, jan.2009.
- [4] T.Ganegedara and V.Prasanna, "Stride BV:400G+ Single chip packet classification," in Proc.IEEE conf.HPSR,2012,pp.1-6.
- [5] G.Jedhe, A.Ramamoorthy, and K.Varghese, "A Scalable High Throughput Firewall in FPGA," in proc.16th int'l Symp. FCCM Apr.2008, pp.43-52.
- [6] W. Jiang and V.K. Prasanna, "Field-Split Parallel Architecture for high performance Multi-match packet classification using FPGAs," in proc.21st Annu.SPAA, 2009, pp.188-196.
- [7] S. Kelly and S. Frankel. "Using HMAC-SHA-256, HMAC-SHA-384, and HMAC-SHA-512 with IPsec". RFC 4868, IETF Network Working Group, May 2007.
- [8] T.V.Lakshman and D.Stiliadis, "High-Speed policy- Based Packet Forwarding Using Efficient Multi- Dimensional Range Matching," SIGCOMM comput. Commun. Rev., vol.28, no. 4, pp. 203-214, Oct.1998.
- [9] C.R. Meiners, A.X. Liu, and E. Torng, "Hardware Based Packet Classification for High Speed Internet Routers". Berlin, Germany Springer- Verlag, 2010
- [10] C.E. Perkins, E. M. Belding-Royer, and S. Das. "Ad hoc On- Demand Distance Vector (AODV) Routing". RFC 3561, July 2010.
- [11] A. Sanny, T. Ganegedara, and V. Prasanna, "A Comparison of Rule Set Feature Independent Packet Classification Engines on FPGA," in Proc. IEEE IPDPS RAW, 2013, pp.124-133.
- [12] H.Song and J.W. Lockwood, "Efficient Packet Classification for Network Intrusion Detection Using FPGA," in Proc.ACM/SIGDA 13th Int'l Symp.FPGA, 2005, pp.238-245.
- [13] S. Singh and Meenaxi, "COMPARATIVE ANALYSIS OF QoS SENSOR NETWORKS USING ANT COLONY OPTIMIZATION. Control, communication and computer Technology (2013).
- [14] D.E. Taylor, "Survey and Taxonomy of Packet Classification Techniques," ACM Comput. Surv., vol.37, no. 3, pp. 238-275, Sept.2005.
- [15] Thilana Ganegedara, Weirong Jiang, and Viktor K. Prasanna, "A Scalable and Modular Architecture for High- Performance Packet Classification", in Proc.IEEE.
- [16] C.A.Zerbini and J.M. Finochietto, "performance Evaluation of Packet Classification on FPGA-Based TCMA Emulation Architecture," in Proc.IEEE GLOBECOM, 2012, pp.2766-2771.