Proposed Technique of Sub-threshold wireless BFSK Transmitter

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Abstract

This paper is to demonstrate a sub-threshold circuit design approach for use in designs which demand extreme low power consumption. There are currently no validated design flows or proved design methodologies for designing sub-threshold circuits. The main contribution of this paper is to design sub-threshold circuits and to design the required circuit.

Keywords: Binary Frequency Shift Keying (BFSK), Binary Phase Shift Keying (BPSK), Numerically Controlled Oscillator (NCO), Digital to Analog Converter (DAC), Numerically Controlled Oscillator (NCO), Programmable Logic Arrays (PLAs).

1. Introduction

The main concern which hampers the additional scaling of transistorsis the issue of power dissipation. A Very Large Scale Integrated (VLSI) chip consists ofmany energy storage elements, mainly capacitors, some that are required for calculation (MOSFET device capacitances) and some that are a hindrance to circuit operation (parasiticcapacitances). These capacitors are continually charged and discharged through resistiveelements during circuit operation, resulting in energy dissipation in the form of heat. Theamount of heat dissipated puts a restriction on the computational performance of the circuit,or the number of times transistors in the circuit can switch for a given power budget.One could argue that the shrinking of devices has reduced the amount of parasitic capacitanceand this alleviates power dissipation problems. However the increase in the numberof devices due to the increase in device density has more than compensated for the decreasein the parasitic capacitance of a single device.

As circuits shrink and more transistors and circuit functions are integrated on a singlechip, the sub-threshold leakage current is becoming an important determinant of powerconsumption. This leakage current occurs when transistors are not switching. Leakagecurrents therefore dissipate power even when there is no useful computation going on.Increased power consumption in the chipmeans that there is more energy being dissipated as heat. The MOSFET threshold voltage$V_T$decreases with increase in the device junction temperature caused by this heat dissipation. The sub-threshold leakage currents are exponentially dependent on V_T, increasingwith decrease in V_T. Thus increased on-chip temperatures cause more power dissipationdue to increased leakage currents and increased dissipation of heat. Another problem withaggravated on-chip temperatures is that they can result in reduced operating lifespans forthe chip [1]. Also any chip that consumes power beyond a certain degree needs to becooled. This is a significant problem in the case of commercial electronic products such asservers, desktop computers, graphics processors, some high performance gaming devices,etc. Increased cooling solution costs are an additional bane of increased power consumption.High power consumption is thus a growing problem in the ever expanding world ofelectronic devices.There are many applications that use VLSI circuit technology where low power isessential but the speed of operation of the device is non-critical. Examples include sensornetworks, wearable computers, certain portable electronic devices, etc. Here speed is a secondarydesign goal, whereas low power consumption is a primary design requirement. Forexample [2, 3, 4] show that sensor networks have the capability to accumulate, process andcommunicate information under various operating conditions. These networks are spatiallydistributed in nature and have the need for each sensor in the network to be as maintenancefreeas possible. Further, low-power consumption in these applications would reduce theamount of headroom needed for battery supplies. Also the weight of the product would belower since smaller batteries will be sufficient to power these devices, and complex coolingsolutions would not be required.Thus a robust methodology for designing extreme low power circuits will be usefulfor a large class of applications in which larger circuit delays are tolerable but low powerconsumption is a primary design

requirement. The circuit design methodology of choicein this case would be sub-threshold circuit design. Here the $V_{DD}$of the circuit in questionis set at a value lower than or equal to the threshold voltage of that particular processtechnology. The circuit will thus operate with only sub-threshold leakagecurrents, since the transistors in the circuit will never be in the linear or saturation region.This approach not only results in very low power consumption but it also utilizes leakagecurrents for computation and thus capitalizes on the problem that traditional VLSI designmethodologies are faced with (that of an exponential increase in leakage with successiveprocess generations). The only source of power dissipation of the chip (in case of subthresholdcircuits) is due to sub-threshold leakage currents.Sub-threshold circuits yield significantly lower power consumption compared to theirsuper-threshold counterparts. However the sub-threshold current has an exponential dependenceon process, temperature and supply voltage variations. As a result any practicalsub-threshold design methodology must be immune to these PVT variations.

2. Design of the chip

The design of the chip will be targeted for the TSMC [5] 0.25µm process, which is a triple well CMOS process.

2.1 Test Vehicle

There is a large and growing application space that requires a very low power consumption without the need for high speed. One application that does not need high speeds is a wireless radio transmitter, where the signal to be transmitted occupies a small bandwidth (such as voice). An ultra-low power implementation of a radio transmitter will have broad implications for the class of applications that demand very low power consumption. For example this wireless transmitter can be used in sensor networks. The radio transmitter will be realized with digital circuits as far as possible, since digital circuits are preferable to analog circuits when operating in the sub-threshold region. The digital circuits will be implemented using a Network of PLA (NPLA) based approach. A simple digital modulation scheme has to beused for the radio transmitter. Binary Frequency Shift Keying (BFSK) and Binary Phase Shift Keying (BPSK) are two well-known digital modulation schemes. BPSK is 3dB more power efficient than BFSK. However BFSK has the advantage of being easy to implement. Hence BFSK will be used as the modulation scheme for radio transmitter.

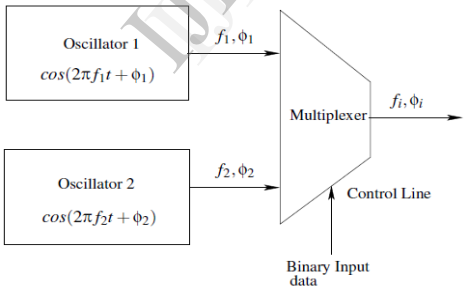

Fig.1. BFSK Transmitter Architecture

2.2 BFSK Radio Transmitter Architecture

A typical BFSK transmitter generates a frequency tone at the output and shifts the frequencyof the output tone to pre-determined values depending on the value of the inputwhich can be a logical HIGH or LOW. A generic digital BFSK transmitter block diagramis shown in Fig.1. The input to the transmitter is assumed to be digitized and suppliedto the transmitter at a rate of RB bits/s. The frequencies of the two tones that will beproduced by the BFSK transmitter are given by f_1 and f_2. Φ_1 and Φ_2 are phase offsets thatthe two tones could have. Depending on the value of the binary input, one of the tones ismultiplexed to the output. A BFSK transmitter can be coherent or non-coherent. In a coherentBFSK modulation scheme, $\Phi_1 = \Phi_2$ and in a non-coherent BFSK modulation scheme,$\Phi_1 \neq \Phi_2$. In practice coherent BFSK modulation is extremely hard to demodulate sincethere is a synchronization required between the transmitter and the receiver. Hence we willuse a non-coherentmodulation scheme. For non-coherent modulation, if the BFSK modulationhas the condition that f_1-f_2 is an integer multiple of the input bit rate, RB then themodulation is called orthogonal FSK (since the two signals used for modulating

the binarydata are orthogonal if this condition is met). If this condition is not met the FSK schemeis called non-orthogonal. The difference between the two schemes is that, non-orthogonal.

2.3 System Architecture

The BFSK transmitter architecture consists of a digital BFSK modulation circuit, a DAC, an amplifier and an antenna for wireless transmission. This is shown in Fig.2. The BFSK modulator is implemented as a digital circuit, using a network of Programmable Logic Arrays (PLAs). We will give a brief introduction to PLAs and how they are used in a network to do computations. We will also discuss in detail about each of the digital and analog components that make up the design of the system. FSK requires more transmit power than orthogonal FSK for the same error performance atthe receiver side. The receiver for an both schemes can be constructed using a couple ofbandpass filters with their pass band frequencies centered around f_1 and f_2 respectively.While designing a BFSK transmitter, the two oscillators in Fig.1 can be realizedusing digital circuits as a Numerically Controlled Oscillator (NCO). In order to do wireless transmission of a signal, we need a Digital to Analog Converter (DAC) and an antenna. The entire system level architecture is explainedin below.

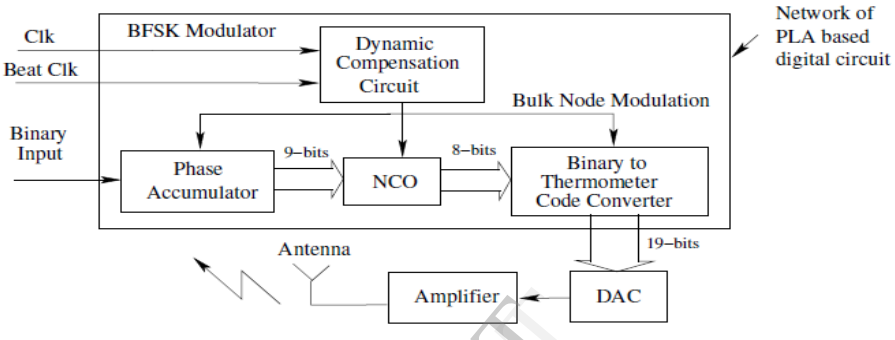

Fig.2. System Architecture

2.4 PLA Basics

This section describes the structure and operation of PLAs which are the basic circuit modules used in this design. Note that the PLAs in this design operate in their sub-threshold region of conduction. Consider a PLA consisting of n input variables x1; x2; …. ,xn, and m output variables y1; y2;….. ym. Let k be the number of rows in the PLA. A literal $l_i$is defined as an input variable or its complement.

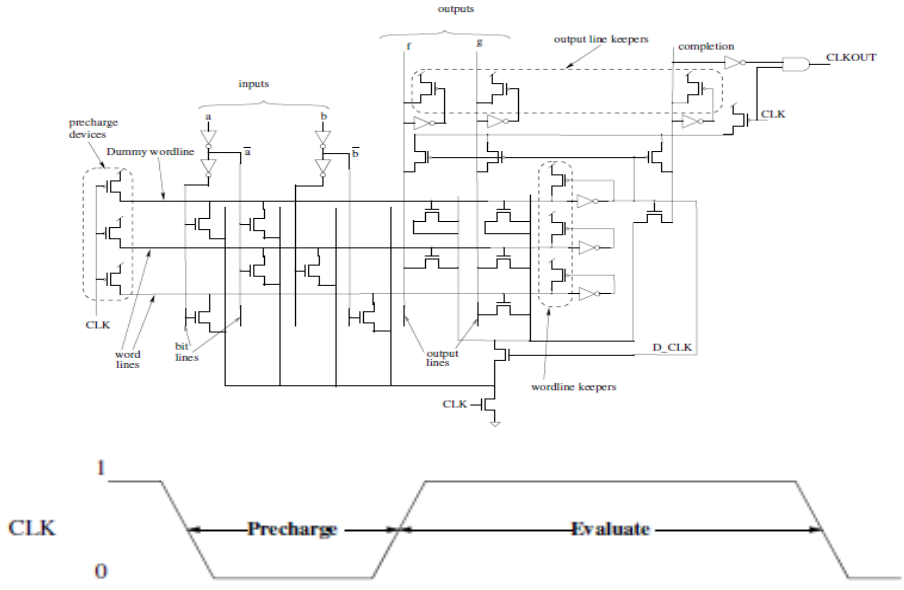

Fig.3. Schematic View of PLA

Suppose we want to implement a function f represented as a sum of cubes f = c1 +c2+….+ck. We consider PLAs which are of the NOR-NOR form. Literals of the PLA are implemented using vertical-running bit-lines.

For each input variable, there are two bit-lines, one for each of its literals. The outputs of the PLA are implemented by output lines, which also run vertically. This portion of the PLA is called the OR plane.Fig.3 illustrates the schematic of the PLAs used in this design. All the PLAs in the designs are of the precharged NOR NOR type, and have a fixednumber of inputs (8), outputs (6) and cubes (12). This was found to be a good size for the design based on logic synthesis results using medium sized PLAs (5-15 inputs, 3-8 outputs and 10-20 rows). Also, a technique called folding is used, to enhance a PLA to hold more logic without increasing the area used. This is doneby running two unconnected bit-lines corresponding to two different inputs on the same track. One of the bit-lines start from the top of the PLA and the other one starts from the bottom and stops clear of the first bit-line. In this way, more cubes can be fitted into the PLA in compact way.

2.5 Network of PLA Operation

A network of PLAs, NPLA is nothing but a multilevel network of PLAs. Each of the digital components that make up the digital BFSK modulator, i.e. the Dynamic Compensation circuit, NCO and the Binary to Thermometer Code Converter are made of NPLAs. Each of these blocks are implemented as combinational circuits and the outputs of each of these blocks are registered using negative edge triggered flip-flops clocked by Clk.The flip-flops are negative edge triggered as the outputs of the flip-flops need to be stable when the Clk signal is HIGH when the PLAs are evaluating. The timing diagram of NPLAsin a single combinational circuit is shown in Fig.4. From this figure allthe PLAs in a network precharge at the same time and start evaluating one after anotherin a cascading fashion. Hence an evaluation period has to be provided, that is sufficientfor all the PLAs to evaluate. Each PLA in the network is clocked by the previous PLAsCLKOUT signal except for thefirst PLA in the chain which is clocked by the CLK signal.The CLKOUT signal of each PLA is the logical AND of its completion signal and the CLKsignal. The maximum throughput that can be achieved depends on the delay of the slowestcombinational block. When implemented as a network of PLAs, the throughput of the circuit can be approximately written as:

$$Throughput = \frac{1}{T_{pchg} + N * T_{eval}}$$

Here N is the number of levels of PLAs needed in the multilevel network of PLAs.

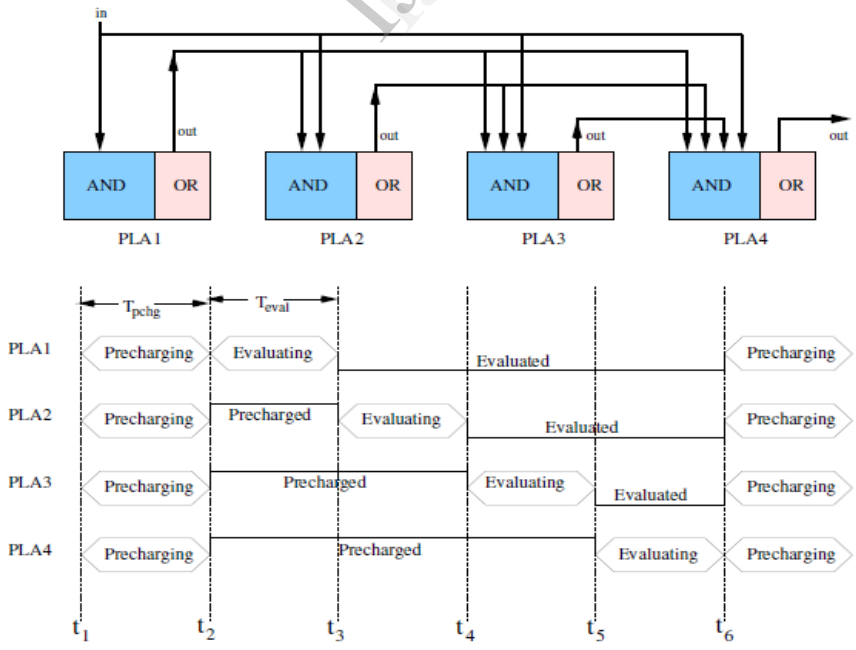

Fig.4. Timing Diagram of a NPLAs

3. The Digital BFSK Modulator

The function of the digital BFSK modulator is to produce either of two frequency tones depending on the logical value of a binary input signal. The digital BFSK Modulator seen in Fig.1 has two oscillators, but we have reduced this complexity of having two oscillators by using a Numerically Controlled Oscillator (NCO). The modulator is implemented using three combinational circuits namely, the phase accumulator, the NCO and the binary to thermometer code converter. These combinational circuits have negative edge triggered registers between them, which are clocked by the CLK signal.

3.1 Digital to Analog Converter (DAC)

The circuit diagram of the DAC is shown in Figure III.8. The DAC has a reference current mirror, M1 biased by resistor R_{cm}. It also has many current mirrors reflecting the reference as the number of input bits. The input to the DAC is a 19bit digital signal. The top 15 MSBs are thermometer encoded and the 4 LSBs are binary encoded. Hence the DAC will have 19 current mirror legs. Figure III.8 shows two of the current mirror legs of the DAC. The inputs T_i and T_{ib} are the i^{th} thermometer encoded bit and its complement. The inputs Bi and Bib are the ith binary encoded bit and its complement. The DAC works by switching the current mirrors ON depending on the value of the input bits and measuring the voltage across the Rout resistor due to this current. The input bits control the NMOS transistors, M3,M4,M6 and M7. If the input bit is HIGH, then the NMOS on the right turns ON and allows the leg to mirror thecurrent in the reference transistor M1. The difference between the current mirrors for thethermometer code and the binary code is in the size difference between M2 and M5.

3.2 Common Source Amplifier

A common source amplifier is needed at the output of the DAC to amplify the signal and drive the antenna. The common source configuration is shown in Fig.5. The common source amplifier is an inverting amplifier. In this configuration, note that there are no bias resistors biasing the gate of the transistor M1. The gate of M1 is connected to the output of the DAC. The gate is thus biased by the DC component of the sinusoidal voltage from the output of the DAC. The amplifier is powered by a very low V_{DD}.

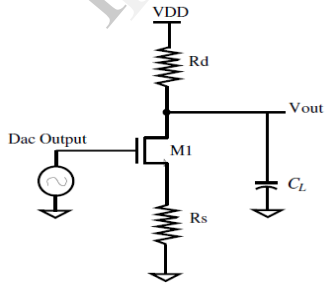

Fig.5Common Source Amplifier

3.3 Antenna

An onchip antenna is used to transmit the signal from the amplifier. However due to the low frequency of operation, the length of the antenna coil needs to be comparable to half the wavelength of the transmitted signal which is around 300 meters. We have used an antenna coil of a length of only 0.2 meters due to area constraints on the chip. However, an external antenna will be used to transmit the signal if needed.

4. Conclusion

In this paper the design considerations of the wireless BFSK transmitter chip were discussed and also the architecture of the chip and analyzed each of the modules separately. The CLKOUT signal of each PLA is the logical AND of its completion signal and the CLK signal. The maximum throughput that can be achieved depends on the delay of the slowest combinational block and a network of PLAs, the throughput of the circuit can be approximately written based on the through put calculation.

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