Realization of Optimized OFDM System using FPGA on Altera Quartus 3.0

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Abstract

Orthogonal Frequency Division Multiplexing (OFDM) is a multicarrier modulation technique which divides the available spectrum into many carriers. OFDM uses the spectrum efficiently as compared to FDMA by spacing the channel much closer together. Interference between closely spaced carriers is prevented as all the sub-carriers are orthogonal to each other. This technique has found enormous applications in high speed mobile and wireless communication systems. The main advantage of OFDM is their robustness to channel fading in wireless environment. In this paper the FPGA implementation of optimized OFDM system on Altera Quartus 3.0 platform using VHDL (Very High Speed Integrated Circuit Hardware Descriptive Language) will be illustrated. The system performance will be analyzed from resource summary and simulation waveform of individual module through detailed timing simulation. The design and analysis of different module of OFDM system such as mapping module, Serial to Parallel Converter, Parallel to Serial Converter, 8-point IFFT (Inverse Fast Fourier Transform) and FFT (Fast Fourier Transform) using Decimation-in-Frequency (DIF) radix-2 algorithm will be highlighted in this paper.

1. Introduction

The need for high speed communication has become an utmost priority due to growing demands of current generation. In order to cater these demands various multicarrier modulation techniques have evolved, few notable among them being Code Division Multiple Access (CDMA) and Orthogonal Frequency Division Multiplexing (OFDM). Due to robustness to channel fading and orthogonal property of carriers which prevents interference between closely spaced carriers OFDM is widely used in fixed Wi-Fi System (IEEE802.11 a standard), fixed Wi-Max system (IEEE802.16 a standard), mobile Wi-Fi system (IEEE 802.11 b standard) and mobile Wi-Max system(IEEE 802.16 e standard) etc.

The primary objective of this paper is to realize optimized OFDM system to be suitable for wireless communication. Functionality is programmed in FPGAs by designer rather than device manufacturer which provide flexibility and ability to reconfigure as per the need. FPGAs can be reprogrammed multiple times, even after deployment, the facility which is lacked in Application Specific Integrated Circuits (ASICs). Flexibility provided by FPGAs leads to its implementation in many high speed digital processing application such as networking, video and image processing and communications.

This paper will illustrate the basics of OFDM system, its implementation and the analysis of obtained results of simulation testing in Altera Quartus platform. This OFDM system is carried out with BPSK modulation scheme as this scheme is a constant energy scheme and easier to realize. The next of this paper is organized as follows: section-2 provides related work, section-3 introduces OFDM overview, section-4 presents simulation results, section-5 VHDL simulation and conclusions.

2. Related Work

Chris Dick [1] shows a high-level overview of FPGA implementation with some detail description of synchronization, packet detection, preamble and equalization at OFDM receiver. It lays emphasis on advantage of designing FPGA systems over ASIC to realize the SDR "Software Defined Radio" concept. The approach for implementing FPGA technique to solve problem of OFDM system implementation is presented by M.A. Mohamed [2].

Ma. José Canet [3] emphasizes on the solutions for OFDM signal generation in baseband andin intermediate frequency. The work carried out by Canet

also indicates implementation issues of a digital transmitter for an OFDM based WLAN systems. Dusan Matiae [7] investigated the suitability of OFDM for multimedia application. Eric Cosby [8] explains the analysis of OFDM systems and its concepts.

Moisés Serra [5] demonstrated the design of an OFDM transmitter as a part of an OFDM demonstrator Hiperlan/2 based. Paul Guanming Lin [6] investigated the change of performance by varying some of the major parameters of an OFDM system and demonstrated the concept and feasibility of an OFDM system.

3. OFDM Overview

OFDM is a special case of multicarrier modulation which is particularly suited for transmission over a dispersive channel. Here different carriers are orthogonal to each other, that is, they are totally independent of one another. This is achieved by placing the carriers exactly at the nulls in the modulation spectra of each other. OFDM signal can be presented as shown in Figure 1.

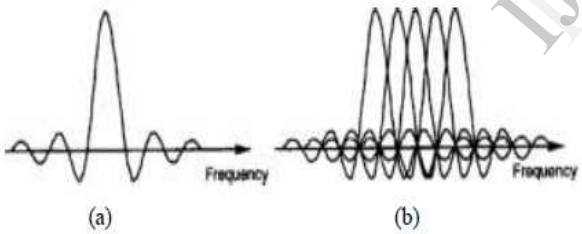

Figure 1 Spectra of (a) OFDM sub-channel and (b) OFDM signal

OFDM is a Frequency Division Multiplexing scheme utilized as a digital multi-carrier modulation method. The data is divided into several parallel streams of channels, one for each sub-carrier. Each subcarrier is then modulated with a conventional modulation scheme (such as BPSK, QPSK etc.) at a low symbol rate. Figure 2 (a) shows the simple conventional method in which the bandwidth used to transmit the signal is more than OFDM as shown in Figure 2(b).

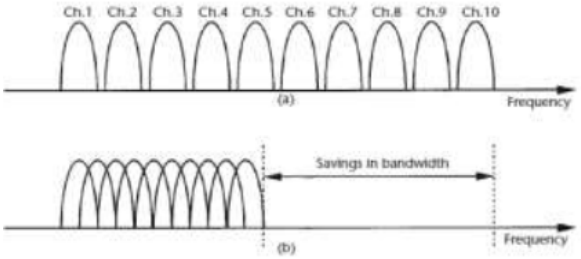

Figure 2 Transmission Techniques

3.1. OFDM Advantages

OFDM system has the following advantages: (i) high spectral efficiency due to orthogonally placing the sub-carriers, (ii) Addition of guard band almost removes ISI and ICI in the system, (iii) immune to frequency selective fading, (iv) can recover lost symbols due to frequency selectivity of channels, (v) computationally efficient, (vi) channel equalization.

3.2. OFDM Disadvantages

OFDM systems have the following disadvantages: (i) Large peak-to-mean power ratio due to superposition of all sub-carriers with varying amplitude, (ii) Multipath propagation should be avoided so that orthogonality is not getting affected.

3.3. OFDM Transceiver

The block diagram of an simple OFDM transceiver is shown in Figure. 3. The basic component will be discussed in the next few subsections.

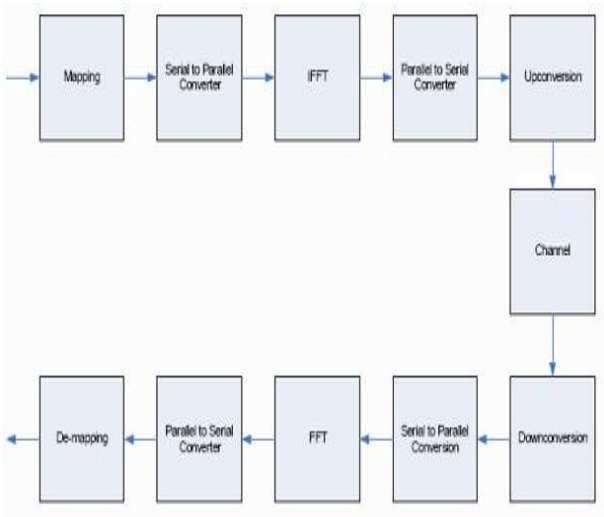

Figure 3 OFDM Transceiver

3.3.1. OFDM Transmitter

The simplified block diagram of OFDM Transmitter module is shown in Figure 4. It can be seen that the block is divided into several parts with each block function differently and this is to ensure that the system works effectively. Since the main component is processing block, so, the work is started from this part. All block set function is implemented in the FPGA development board. Cyclic prefix is a module, which is used to concatenate partial end of information bit and put at the beginning of the information frame. But in this project cyclic prefix is not included in this design. The generation of OFDM signal started from amplitude modulation mapping bank. The serial input data is mapped to appropriate symbol to represent the data bits. These symbols are in serial and need to convert into parallel format since IFFT module requires parallel input to process data. The serial to parallel module does the conversion. These parallel symbols are transformed from frequency domain into time domain using IFFT module. These signals are converted into serial format and add a cyclic prefix to data frame before being transmitted.

3.3.2. OFDM Receiver

The simplified block diagram of OFDM Transmitter module is shown in Figure 5. There are five modules in the receiver block and cyclic prefix removal will not be included into the design. The received data is in serial format, thus, since FFT input is in parallel, a module which use to converts from serial to parallel is required. Output from FFT is converted back to serial format through parallel to serial converter. The conversion is required since the serial data need to be transmitted. Finally the serial output is demodulated using de-mapping module to get the transmitted data.

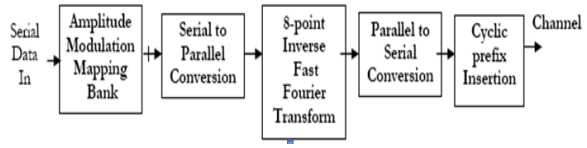

Figure 4 OFDM Transmitter Module

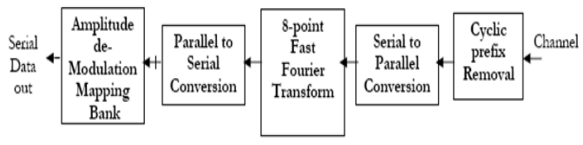

Figure 5 OFDM Receiver Module

4. Simulation Results

OFDM Transceiver system is designed using VHDL and synthesized using Altera Quartus 3.0 simulator tool. The system performance is analyzed from resource summary and simulation waveform of individual module obtained through detailed timing simulation. Internal RTL Schematic, simulation waveform and resource usage summary of individual module of OFDM system is analyzed through the following experiments.

4.1. Analysis of Serial To Parallel converter Module

A serial to parallel converter is reverse of the operation of parallel to serial converter. The data comes serially from input port SERIN. The parallel data is output from output port 'Q'. The internal RTL schematic and simulation waveform of serial to parallel converter module are presented in Figure 6 and Figure 7 respectively.

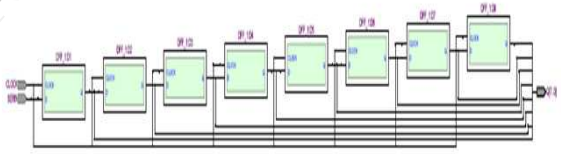

Figure 6 Internal RTL Schematic of Serial To Parallel Converter

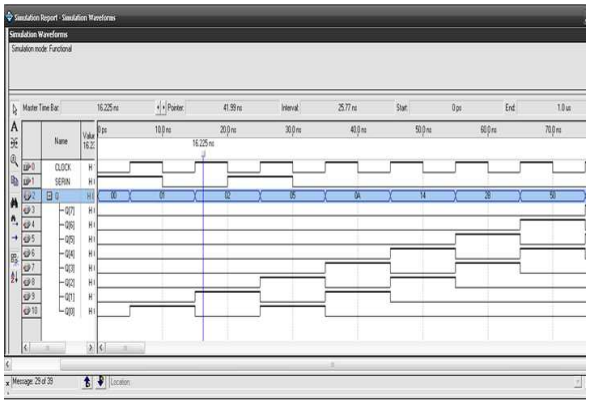

Figure 7 Simulation Waveform of Serial To Parallel Converter

4.2. Analysis of Parallel To Serial converter Module

A parallel to serial converter is a special function of shift register. The data is parallel loaded to the shift register and then shift out bit by bit. This parallel to serial module is designed such that the data to be

transmitted is first parallel loaded then transmitted bit by bit by a start bit of value '1'. The internal RTL schematic and simulation waveform of parallel to serial converter module are presented in Figure 8 and Figure 9 respectively.

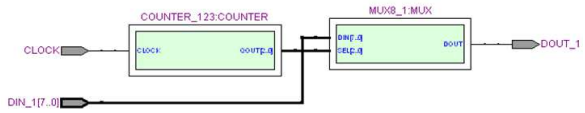

Figure 8 Internal RTL Schematic of Parallel To Serial Converter

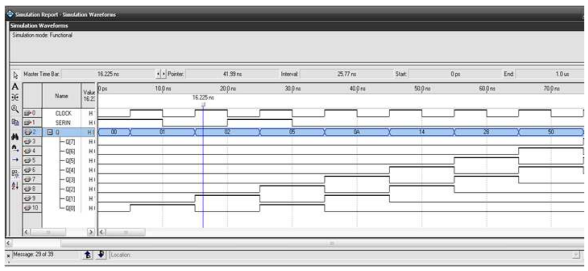

Figure 9 Simulation Waveform of Parallel To Serial Converter

4.3. Analysis of IFFT Module

IFFT module does the inverse operation of FFT module. Here input to IFFT module are clk, reset, in_x0 to in_x7 (each of 8 bit). Using IFFT algorithm for different path real and imaginary output are found in terms of outré and outim respectively. The internal RTL schematic and simulation waveform of IIFT module are presented in Figure 10 and Figure 11 respectively.

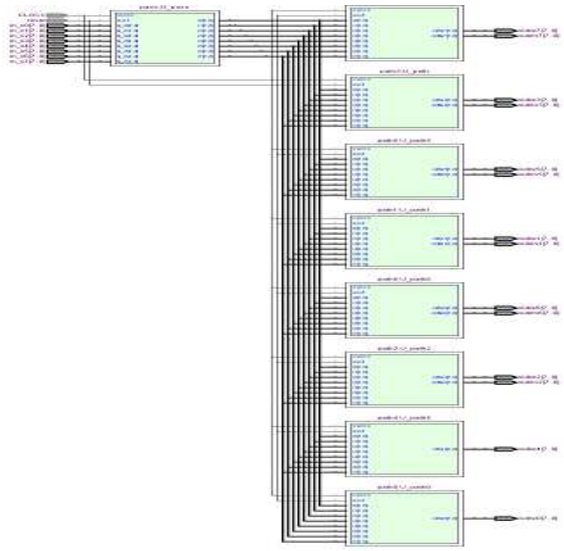

Figure 10 Internal RTL Schematic of IFFT

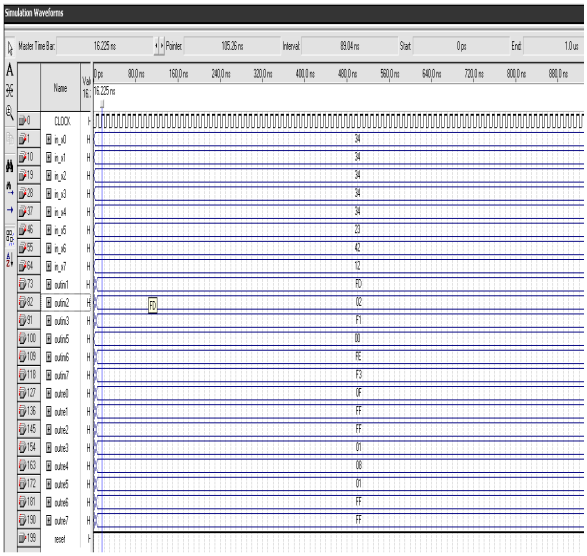

Figure 11 Simulation Waveform of IFFT

4.4. Analysis of FFT Module

It is the inverse operation of IFFT.Here input to FFT module are clk,reset,in_x0 to in_x7(each of 8 bit).As described earlier by using FFT algorithm for different path , real and imaginary output are found in terms of outré and outim respectively.Here decimation in frequency FFT is used and binary value of twiddle factor is taken. The internal RTL schematic and simulation waveform of IIFT module are presented in Figure 12 and Figure 13 respecti

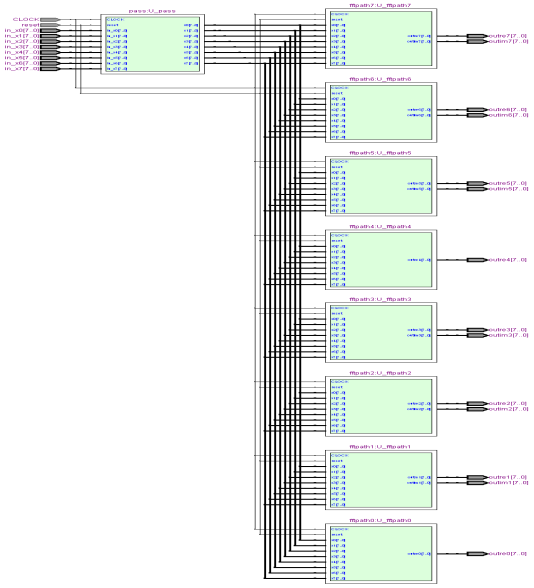

Figure 12 Internal RTL Schematic of FFT

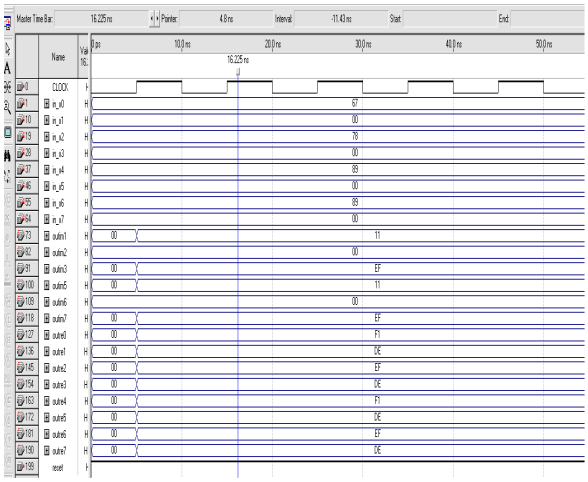

Figure 13 Simulation Waveform of FFT

4.4. Analysis of BPSK Module

The mapping module used is BPSK type of modulation. BPSK is used because module is much easier to design compared to QPSK or other modulation method. If the input is '1' then the value is mapped with '1' while if the input is '0' the value is mapped with '0'. This type of modulation is monopodal type. The internal RTL schematic and simulation waveform of BPSK module are presented in Figure 14 and Figure 15 respectively.

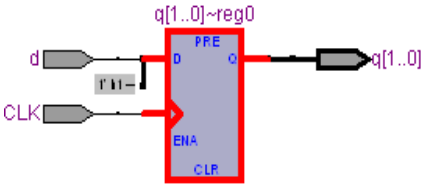

Figure 14 Internal RTL Schematic of BPSK

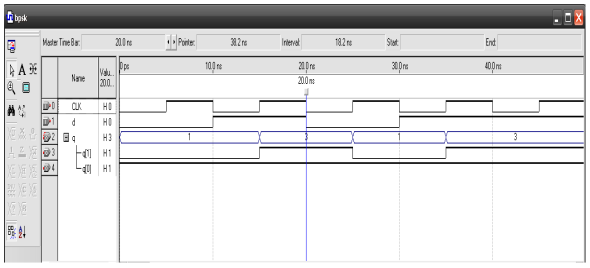

Figure 15 Simulation Waveform of BPSK

4.5. Analysis of OFDM Transmitter

The system performance of OFDM Transmitter module is analyzed from RTL Schematic, Simulation waveform and resource usage summary obtained through timing simulation as shown in Figure 16, Figure 17 and Figure 18 respectively. Transmitter module combines mapper, IFFT, serial to parallel and parallel to serial converter in a single module and serially out its output.

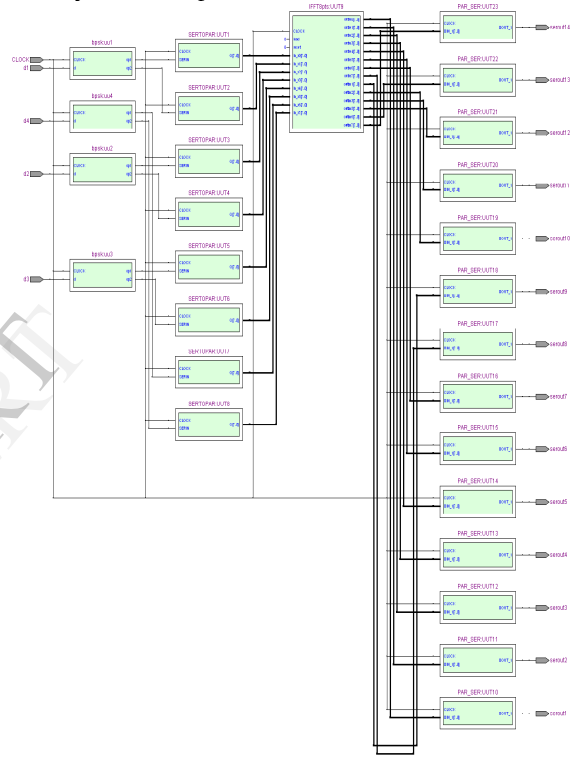

Figure 16 Internal RTL Schematic of OFDM Transmitter module

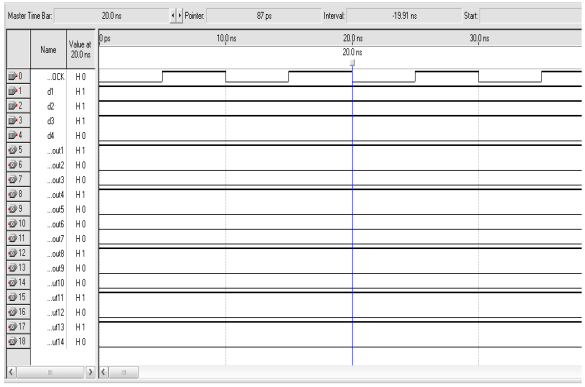

Figure 17 Simulation Waveform of OFDM Transmitter module

Analysis & Synthesis Resource Usage Summary		
	Resource	Usage
1	Estimated Total logic elements	1,220
2		
3	Total combinational functions	1156
4	⊟ Logic element usage by number of LUT inputs	
5	-- 4 input functions	70
6	-- 3 input functions	727
7	-- <=2 input functions	359
8		
9	⊟ Logic elements by mode	
10	-- normal mode	389
11	-- arithmetic mode	767
12		
13	⊟ Total registers	64
14	-- Dedicated logic registers	64
15	-- I/O registers	0
16		
17	I/O pins	178
18	Maximum fan-out node	CLOCK
19	Maximum fan-out	64
20	Total fan-out	3427
21	Average fan-out	2.45

Figure 18 Resource Usage Summary of OFDM Transmitter

4.5. Analysis of OFDM Receiver

The system performance of OFDM Receiver module is analyzed from RTL Schematic, Simulation waveform and resource usage summary obtained through timing simulation as shown in Figure 19, Figure 20 and Figure 21. Receiver module combines serial to parallel, FFT and parallel to serial converter in a single module and serially out its output.

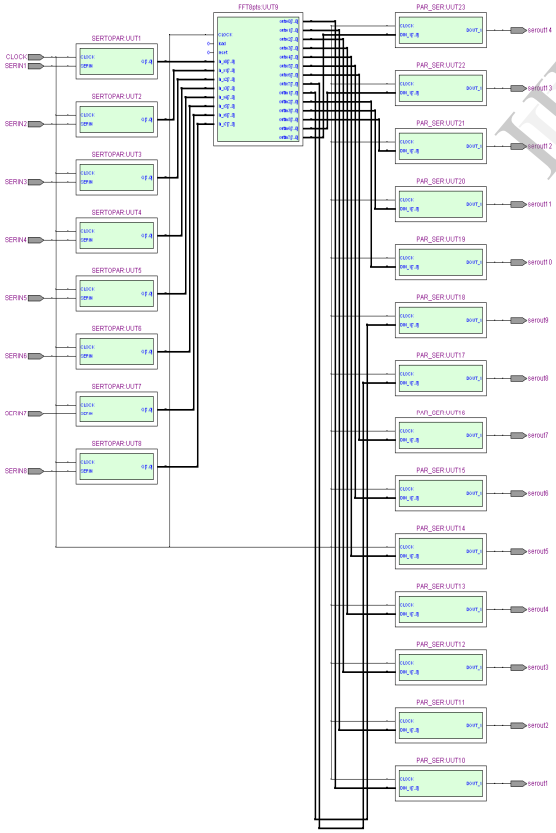

Figure 19 Internal RTL Schematic of OFDM Receiver module

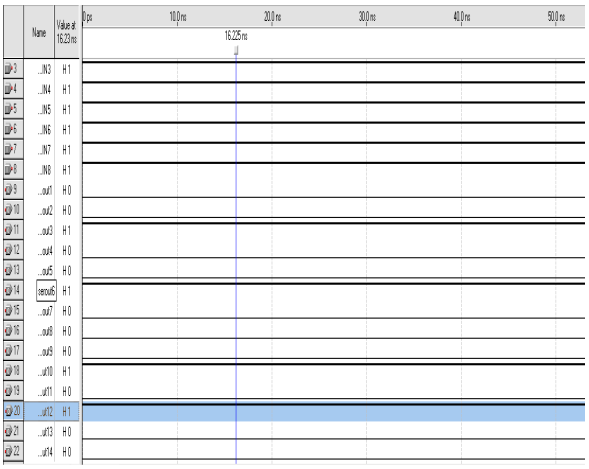

Figure 20 Simulation Waveform of OFDM Receiver module

Analysis & Synthesis Resource Usage Summary		
	Resource	Usage
1	Estimated Total logic elements	732
2		
3	Total combinational functions	668
4	⊟ Logic element usage by number of LUT inputs	
5	-- 4 input functions	60
6	-- 3 input functions	497
7	-- <=2 input functions	111
8		
9	⊟ Logic elements by mode	
10	-- normal mode	133
11	-- arithmetic mode	535
12		
13	⊟ Total registers	64
14	-- Dedicated logic registers	64
15	-- I/O registers	0
16		
17	I/O pins	178
18	Maximum fan-out node	CLOCK
19	Maximum fan-out	64
20	Total fan-out	2248
21	Average fan-out	2.47

Figure 21 Resource Usage Summary of OFDM Receiver

5. Conclusions

The main focus of this work is to realize an optimized OFDM system using FPGA which is evident from obtained resource usage summary of OFDM Transmitter and Receiver module. The design implementation is done using VHDL coding on Altera Quartus 3.0 platform. The Fast Fourier Transform (FFT) and Inverse Fast Fourier Transform (FFT) have been chosen to implement the design instead of the Discrete Fourier Transform and Inverse Discrete Fourier Transform because they offer better speed with less computational time.These methods requires the odd and even samples inputs are process separately before they are combine to give the final output. The result of the computation is in integer bits which might comprises of real and imaginary components. The decimal value of the output if greater than 0.5 is approximated to 1 and vice versa. Direct mathematical

method is adopted because it is an efficient and optimized method instead of the structural implementation which is based on butterfly operation. In this work the objective of implementing the optimized core processing blocks of an Orthogonal Frequency Division Multiplexing (OFDM) is successfully achieved. After VHDL simulation of this OFDM system is observed on Altera Quartus, we could implement this system on FPGA.

6. References

[1] C. Dick and F. Harris, "FPGA Implementation of an OFDM PHY" Signals, Systems and Computers, 2003. Conference Record of the Thirty-Seventh Asilomar Conference, Vol.1,pp: 905–909, Nov. 2003.

[2] M. A. Mohamed, "FPGA-BASED DESIGN OF OFDM SYSTEM", the Mediterranean Journal of Computers and Networks, Vol. 7, No. 1, pp: 163-170, 2011.

[3] Ma. J. Canet, F. Vicedo, J. Valls and V. Almenar, "Design of a Digital Front-End Transmitter For OFDM-WLAN Systems Using FPGA", Control, Communications and Signal Processing 2004, First International Symposium on, pp:503–506, 2004.

[4] Y. Awad, L. H. Crockett and R. W. Stewart, "OFDM TRANSCEIVER FOR IEEE 802.20 STANDARDS".

[5] M. Serra, J. Ordiex, P. Marti and J. Carrabina, "OFDM Demonstrator: Transmitter" in Proc 7th International OFDM Workshop 2002, Sep 2000.

[6] P. G. Lin, "OFDM simulation in MATLAB", a senior project, faculty of California Polytechnic State University, San Luis Obispo, June 2010.

[7] Dusan Matiae, "OFDM as a possible modulation technique for multimedia applications in the range of mm waves," TUD-TVS, 30-10-1998.

[8]Erich Cosby, "Orthogonal Frequency Division Multiplexing (OFDM): Tutorial and Analysis", 11-12-2001, Virginia Tech. Northern Virginia Center.

[9] K. A. Kadiran, "Design and implementation of OFDM transmitter and receiver on FPGA hardware", Master thesis, Universiti Teknologi Malaysia, 10 November 2005.

[10] A. Cortés, I. Vélez, I. Zalbide, A. Irizar, and J. F. Sevillano,"An FFT Core for DVB-T/DVB-H Receivers," VLSI Design, vol. 2008, Article ID 610420, 9-pages , 2008.

[11] M. Helaoui, S. Boumaiza, A. Ghazel, and F. M. Ghannouchi, "On the RF/DSP design for efficiency of OFDM transmitters" IEEE Trans. Microw. Theory and Tech., vol. 53, no. 7, pp. 2355-2361, Jul. 2005.

[12] Jae-Kwon Lee, Jeong-Sang Park and Jin-Up Kim, "A convolution coding scheme for PAR reduction in WLANOFDM system", IEEE International Conference on Intelligent Pervasive Computing, pp. 98-100, 2007.

[13] Ahmed Sghaier, Shawki Areibi and Bob Dony, "A pipelined implementation of OFDM transmission on reconfigurable platforms", IEEE Canadian conference on Electrical and Computer Engineering, pp. 801-804, May 2008.

[14] Robin Hoel, "FEC implementation", Texas Instruments, Design note DN504, 2007.

[15] Joaquin Gracia and Rene Cumplido, "On the design of an FPGA-based OFDM modulator for IEEE 802.11a", 2nd International conference on Electrical and Electronics Engineering (ICEEE) and XI conference on Electrical Engineering (CIE), pp.114-117, Sep. 2005.