Reconfigurable Architecture for Video Codec Supporting Advanced Video Standard HEVC

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***Abstract* - For the rationale of motion estimation, recent trends handle many video compression standards, such as MPEG-2, MPEG-4, H.264, and WMV-9. These compression standards are entrenched with a reconfigurable architecture. This paper is concerned with introduction of HEVC compression standard in addition to the other video standards to regulate a multi-standard architecture.**

Keywords* - *MPEG-2, MPEG-4, H.264, WMV-9,HEVC ,reconfigurable architecture

1. INTRODUCTION

The advent of inventions of various commodities that exhibits visual representations ranging from cellular phones and other portable devices such as laptops, tablets to High Definition Televisions are in prerequisite to process high resolution video information. Although various common video compression standards have been implemented such as MPEG-2, MPEG-4, H.264 and WMV-9, improvisation in order to rectify the dissipation of power is necessary. Moreover, for reliability the ME (motion estimation) is implemented on full scale in System-on chip SoC. The intention of this paper is to provide a newly single reconfigured architecture, with an extension to HVC in addition to the existent video compression standards, possessing the capacity to handle a broad spectrum of video standards. The paper is bifurcated in to various sections. Section 2 gives an outlook about the video standards and their motion estimation requirements. Section 3 discusses about the structure of a reconfigurable architecture for multi-handling of various video standards. The schematic view of HEVC architecture and their method of implementation are discussed in section 4. Section 5 discusses about the performance level of the newly configured architecture comparing the efficiency of the various video standards with it and their level of efficiencies. Conclusions of the paper are described in section 6.

2. AN OVERVIEW OF HEVC

HEVC abbreviated a High Efficiency Video Coding is a successor version of H.64 and AVC versions of compression standards and it is a Joint standard of ISO-IEC/MPEG and ITU-T/VCEG: JCTVC, in order to improve efficiency and better resolution aspects. The betterment in the HEVC standards is of exhibiting ultra high resolution video interface, providing a block size ranging from 8*8 to 64*64. The prediction unit of the coding technique is of 2N*2N, N*N for the intra levels and 2Nx2N, NxN, dNxN, NxdN for inter levels. Shown in fig 1. Considering the transform levels of techniques employed for the HEVC, Discrete cosine Transform is utilized. Moreover, for the intra levels, in addition to the discrete cosine transform (DCT), a concatenation of discrete sine transform (DST) is also used. [8] [9]

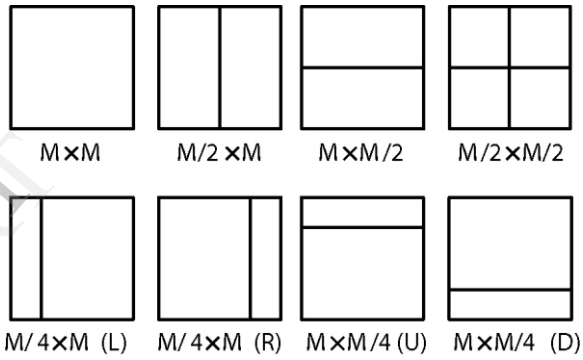

Fig: 1 Blocking of prediction units.

While observing the features of HEVC, there is a constant improvement in its speed, thereby reducing its levels of memory requirements. There is no necessity of interlacing tools, while field coding is sufficient. For the purposes of motion estimations, Advanced Motion Vector Prediction (AMVP) which is of both spatial and temporal is deployed. While establishing the quality levels of the coding, for the entertainment purposes, an average savings of 35% is observed. The levels of performances tend to increase beyond 39% for the High Definition Videos. The bit rate savings is pragmatic to be 40% for the applications of low delay. 50% savings for perceived quality videos and up to 67 % levels of 1080 pixels content is noticed. As an improvisation to the next levels, they are also been researched for implementation to the three dimensional structures of images and motion pictures and implementation in professional tooling. [1] [2]

3. SCHEMATIC ARCHITECTURE OF HEVC

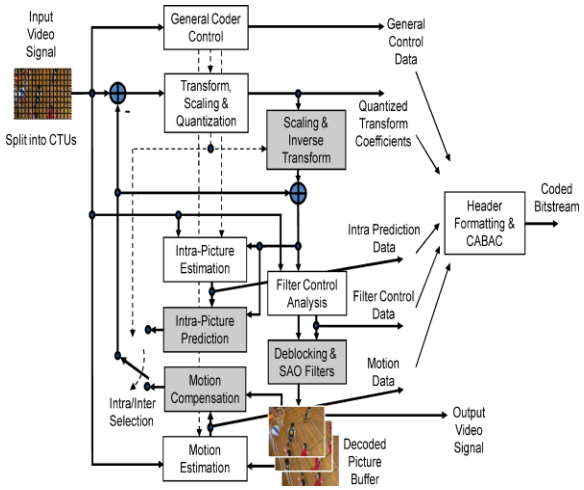

Fig : 2 Basic architecture

The above structure is a hybrid outcome of HEVC consisting of both encoder and decoder employed. Initially, the image that is to be processed is divided into sequential blocks and sent to encoder. The encoding process is done by selection of motion information that constitutes the image of reference and the motion vector to be applied. The residual signal is transformed spatially thereby scaled and quantized of its co-efficient. Duplication of the encoder is performed by the decoder for identical subsequent of data. Later, the residual is then added to the prediction, and combined result is then applied to loop filters for the purpose of smoothing out artifacts induced by block-wise processing and quantization. Then the final output image is stored in a decoded buffer that will be utilized for the predicting subsequent pictures. HEVC is a hybrid video codec. Some existing tools from H.264/AVC have only been revisited in this standard. HEVC has been designed to target ultra high resolution with higher framerates compared to H.264/AVC. Taking this into consideration, HEVC has introduced a new partitioning image scheme concept based on a quadtree structure with larger block size – a 64x64 Coding Unit (CU). A Coding Unit can be recursively divided into 4 CUs (Quadtree). Optionally, all the samples based processing and the reference pictures storage may be made using 10 bits precision (Internal Bit Depth Increase, IBDI).

4. A MODEL ME ARCHITECTURE FOR VIDEO COMPRESSION STANDARDS

General motion estimation architecture is very efficient when the proposed architecture is reconfigurable so that, it enables the addition of various video compression standards with inclusive of its design standards. The common structure consists of a motion estimator through with, the movements or the dynamic propagation of the video structure is subjected observation and acquisition. For the purpose of arithmetic calculation, several IP cores are implemented.[7][8]. Memory structure as Random Access and Read only memories are utilized. The standard functions of acquisition are fed in to ROM since there is no necessity for alteration, whereas for determination and modification of standards, the input is fed in to the RAM. A fully fledged architecture for HEVC is given in the following fig 3.

Process element architecture

The process element architecture of HEVC consists of a load and a control, which are the provision for the input signal for the architecture. The provided structure is of 8 pixel values, ranging from 0 to 7, with the maxima of (L-1). For processing of data, the 8*8 block elements are stored in the Cx registers respectively. On considering every cycles, a set of 8*8 absolute difference array units are operated in parallel. The first stage includes processing of 8*1 SAD values. The 8 SADs are passed through the shift registers to summate the 8*8 SAD value blocks.

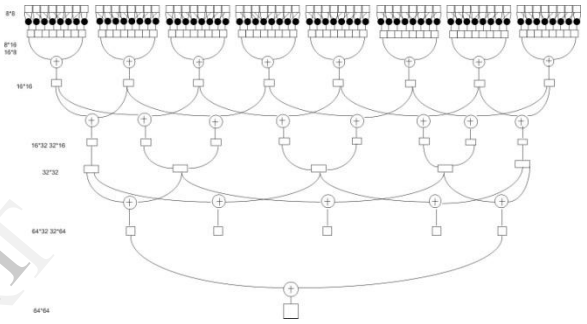

Fig : 3 A model ME architecture for video compression standards

it is possible to divide a frame into slices, as in H.264/AVC. Slices are groups of LCUs in scan order. Slice can be used both for network packetization and for parallel processing. However, a severe penalty on rate distortion performance is incurred when using slices, due to the breaking of all dependencies at their boundaries and to the slice header size, a set of parameters that has to be transmitted at the beginning of each slice. Because of this, new approaches aiming at facilitating parallel processing have been adopted in HEVC

Coding tools

The Coding Unit Quantization Group (CUQG) is specified as a superset of CU for conveying Quantization Parameter (QP) values. Each CUQG is composed of single or multiple CUs, all of which have same QP values. Average QP of left and top CUQG (if available) are used as predictor for current CU quantization parameter. The significance map (SM) of a TU indicates the positions of non-zero coefficients in the TU. For the largest TU size, a two level structure allows for splitting the SM into 4x4 SMs for coding. Transforms are DCT 4x4, 8x8, 16x16 or 32x32, and 64x64 except for Intra 4x4 that is DST (Mode Dependant Decoding Transform). In case of Asymmetric Motion Partitioning (AMP), Non-Square Transform

(NSQT) is used. Band offset (BO) classifies all pixels of a region into multiple bands where each band contains pixels in the same intensity interval. The intensity range is equally divided into 32 intervals from zero to the maximum intensity value (e.g. 255 for 8-bit pixels), and each interval has an offset. Next, the 32 bands are divided into two groups. One group consists of the central 16 bands, while the other group consists of the rest 16 bands. Only offsets in one group are transmitted.

In this paper, a reconfigurable architecture for multi-standard video motion estimation is presented included witrh HEVC (high efficiency video coding). Re-use of the partial 4×4 block SAD values combined to be configured simple control logic and flexibility in the size of search range. Importantly, this reconfigurable architecture requires only slightly more
power and area of the chip .Tto achieve this flexibility when compared with equivalent dedicated circuits. This flexibility can also be used at run-time to adapt the system to real time constraints.

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