# Reduction of Harmonics of a Three Level Indirect Matrix Converter using Space Vector Pulse Width Modulation Technique- A Simulation Study

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## *Abstract*

*Variable voltage and variable frequency AC drives are widely used in commercial applications in order to control motion, improve efficiency of an Induction Motor. Space Vector Pulse Width Modulation (SVPWM) Technique has become the most popular and important PWM techniques for three phase Voltage Source Inverters for the control of AC Induction motor. The major disadvantage of traditional AC-DC-AC power converter is the need for a bulky and limited lifetime energy storage electrolytic capacitor in the DC link. Alternatively, a matrix converter can be used, which is a forced-commutated AC-AC power converter topology that directly converts energy from an AC source to an AC load without the usage of an energy storage element. Three level-Indirect Matrix Converter is the most performing topology from the family of matrix Converters that can synthesize three-level voltage to improve the output performance in terms of reduced harmonic contents. Simulation results prove the ability of this converter topology to produce better output voltages. This paper also presents comparison of SPWM and SVPWM techniques when implemented on three level indirect matrix converter.*

## 1. Introduction

The three-level-Indirect matrix converter is a multilevel matrix converter topology that applies the three-level neutral-point-clamped voltage source inverter concept to the inversion stage of an indirect matrix converter topology. A new modulation method called Space Vector PWM technique is used for controlling the proposed topology to generate a set of sinusoidal, balanced input and output waveforms. Having the ability to generate multilevel outputs, the three-level indirect matrix converter has a better output performance than the indirect matrix converter in terms of waveform harmonic content.

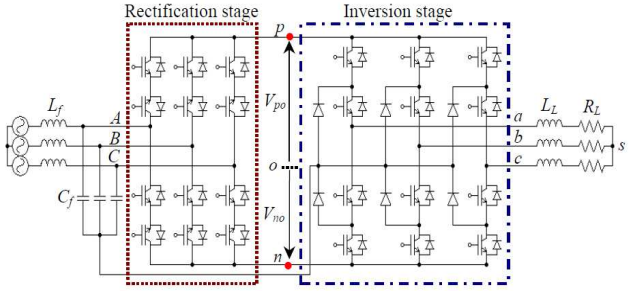


**Fig.1. The schematic diagram of the three-level-Indirect matrix converter**

This topology offers significant advantages: adjustable power factor, capability of regeneration, high quality input/output waveforms and the lack of bulky energy storage electrolytic capacitor. However, it has several disadvantages: limited voltage transfer ratio (0.86), low immunity to power grid disturbance and requires a high number of power semiconductor devices.

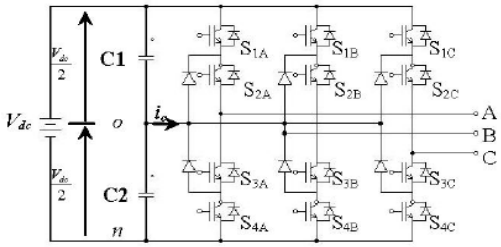


**Fig.2. The Three-level Neutral-Point-Clamped Voltage Source Inverter**

During the recent years, the rapid development of the multilevel converter technology and its ability to produce high quality output voltages has inspired the idea of applying the concept of multilevel converter topology on the MC for synthesizing multilevel voltage at the outputs. The principle of the three-level-Indirect matrix converter topology (IMC3) was proposed in [7], but no modulation/control method was proposed. Its design consists of a four-quadrant current source

rectifier and a three-level neutral-point-clamped VSI (NPC VSI). In order to use the NPC VSI in the inversion stage, the rectified voltage $V_p$, is transformed into a differential DC-supply by tapping the neutral-point of the star-connected input capacitors for providing the required dual-voltage supplies with a zero voltage center- point.

This paper proposes a new SVPWM scheme for the I3MC topology being able to provide three-level voltage at the outputs as well as to maintain sinusoidal inputs. The standard NPC VSI topology and its SVM scheme are firstly reviewed in section II, while section III presents the proposed SVM scheme verifying the ability of the I3MC to produce desired inputs and outputs. Finally, MATLAB/SIMULINK simulation results of I3MC and the output performance comparisons between the SPWM based and SVPWM modulated three level diode clamped NPC VSI are presented in section IV.

## 1. Review of Three-Level Neutral-Point-Clamped Voltage Source Inverter and its Space Vector Modulation Scheme

Space vector modulation (SVM) is an algorithm for the control of pulse width modulation (PWM).[1] It is used for the creation of alternating current (AC) waveforms; most commonly to drive 3 phase AC powered motors at varying speeds from DC using multiple class-D amplifiers. There are various variations of SVM that result in different quality and computational requirements. One active area of development is in the reduction of total harmonic distortion (THD) created by the rapid switching inherent to these algorithms. It is an advanced, computation-intensive PWM method and is possibly the best among the all other PWM techniques. To implement this modulation strategy to the

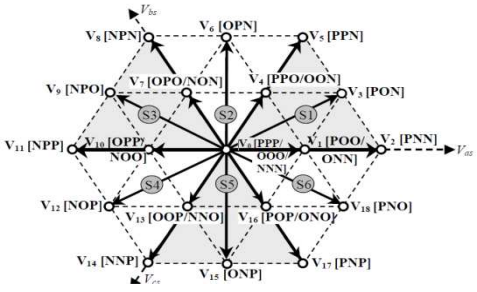


**Fig.3 The space vector diagram for the three-level neutral-point-clamped voltage source inverter**

NPC VSI, the output phase voltages generated by the switching states of the NPC VSI have to be converted into space vectors using the following transformation:

$$V = \frac{2}{3}\left(V_{as} + V_{bs}e^{j\frac{2}{3}\pi} + V_{cs}e^{-j\frac{2}{3}\pi}\right) \quad \ldots.(1)$$

For the NPC VSI, all the switching state combinations can be transformed into eighteen distinct voltage space vectors with fixed directions. Based on their magnitudes, these voltage space vectors can be divided into four groups: zero voltage vector ZVV (V0), small voltage vectors SVV (V1, V4, V7, V10, V13 and V16), middle voltage vectors MVV (V3, V6, V9, V12 and V15) and large voltage

Vectors LVV (V2, V5, V8, V11, V14 and V17). Figure 3 shows the space vector diagram of the NPC VSI that is formed by these voltage space vectors, where the ZVV and SVV obviously have redundant switching states that offer an additional degree of freedom in the synthesize of the output voltage vector.

The desired output for the NPC VSI is a set of sinusoidal and balanced output voltages. Using the space vector transformation this set of time-varying signals is transformed into a reference output voltage vector, $V_{out}$ that rotates along a circular trajectory with frequency $\omega o$ in the space vector diagram. This reference output voltage vector can be expressed as:

$$V_{out} = V_{om}e^{j(\omega_o t - \varphi_o)} = V_{om}\angle\theta_o \quad \ldots..(2)$$

where $V_{om}$ is the magnitude and $\theta o$ is the direction of the reference vector. The variable $\theta o$ is equal to $\omega_o t - \varphi_o$, where $\omega_{ot}$ is the angle of the output phase voltages and $\phi o$ is an arbitrary angle. The reference vector, $V_{out}$ , can be synthesized with three nearest voltage space vectors, which are selected based on the triangle in which the reference vector is located at the sampling instant. Referring to Figure 3, the space vector diagram of the NPC VSI is divided into six sectors (S1 – S6), where each sector consists of four triangles.

**Table 1**
**The switching combination of the NPC VSI**

| $S_{1x}$ | $S_{2x}$ | $S_{3x}$ | $S_{4x}$ | $V_{xo}$ | Switching State |
|---|---|---|---|---|---|
| ON | ON | OFF | OFF | $V_{dc}/2$ | P |
| OFF | ON | ON | OFF | 0 | O |
| OFF | OFF | ON | ON | $-V_{dc}/2$ | N |

Due to the circular symmetry of a three-phase system, it is sufficient to analyze the procedures for synthesizing the reference vector, *V out* , that is located in S1 ($0 \leq \theta o < 60$) to derive the duty cycle equations for the selected vectors in each triangle.

$$V_{out} = d_x V_x + d_y V_y + d_z V_z \quad \ldots(3)$$

Where $d_x$, $d_y$ and $d_y$ are the duty cycles that represent the active times of the selected vectors within the switching period, $T_{sw}$. By determining the duty cycles of the selected voltage vectors, the duty cycles for the

switches, over a switching period, can be determined. To complete the modulation process, the selected voltage vectors are applied to the output according to a switching sequence. Ideally, a switching sequence is formed in such a way that high quality output waveform is obtained with minimum number of switching transitions.

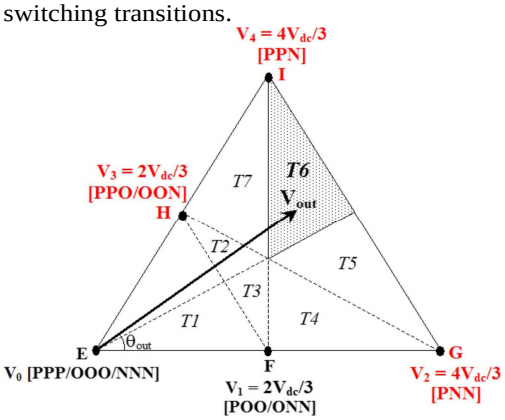


**Fig.4 Definition of triangles within the sector 1 of the space-vector diagram of the three-level neutral-point-clamped VSI**

## 2. Space Vector Modulated Three Level Indirect Matrix Converter

As presented in Fig.1, the I3MC topology consists of a four-quadrant current source rectifier and a NPC VSI. The rectified voltage Vpn is converted into a differential dc supply with uneven halves by tapping the neutral-point of the star-connected input capacitors in order to provide the required dual-voltage supplies and a zero voltage center-point to the NPC VSI. However, the uneven dc link voltages ($V_{po}$ and $V_{no}$) complicate the modulation process but the proposed SVM scheme is able to solve this problem and still generate high quality sinusoidal inputs and outputs. A novel SVM scheme for the I3MC is derived based on the Indirect SVM scheme applied on the indirect MC [3, 4]. Based on the proposed SVM, the rectification stage and the inversion stage of the I3SMC is controlled with SVM separately. In each stage, the SVM produces a combination of vectors to synthesize a reference vector of various amplitude and angle. Detailed explanation of the SVM applied on each stage is further explained in the following subsections. After determining the vectors and its duty cycles, the modulation pattern of the I3SMC combines the switching states of the rectification stage and the inversion stage uniformly in order to obtain a correct balance of the input currents and output voltages in the same switching period.

### 3.1 The Rectification Stage

The rectification stage of the three level- Indirect matrix converter is modulated using SVM to maintain a set of sinusoidal, balanced input currents as well as generating a switching DC-link voltage, *Vpn*, for the inversion stage. The input current vector,
*I in* , is the reference vector for the rectification stage. To synthesize a reference vector, *I in* , that rotates in the space vector diagram, as shown in Figure 5 , two adjacent current vectors ($I\gamma$ and $I\delta$) and a zero current vector ($I0$) are selected based on the sector that the *I in* is located at the sampling instant. As illustrated in Figure 5, the proportion between the duty cycles of $I\gamma$ and $I_\delta$ defines the direction and the duty cycle of $I_o$ determines the magnitude of the reference vector. The duty cycles for the vectors $I\gamma$ $I_\delta$and $I_o$ can be determined using

$$d_\gamma = m_R \cdot \sin\left(\frac{\pi}{3} - \theta_{in}\right), \quad d_\delta = m_R \cdot \sin(\theta_{in}),$$
$$d_o = 1 - d_\gamma - d_\delta.$$

where $m_R$ is the modulation index of the rectification stage and $\theta_{in}$ is the angle of the reference vector within the sector. For the three-level-Indirect matrix converter, the rectification stage is modulated to generate maximum DC-link voltage to inversion stage so that maximum overall voltage transfer ratio can be achieved. As a result, the modulation index, $m_R$, is set to unity (=1) and input displacement factor is controlled to zero (unity power factor). To simplify the overall modulation process, only the modulation on the inversion stage produces zero vectors. Hence, the zero current vector is eliminated and the rectification stage's switching sequence only consists of $I\gamma$ and $I_\delta$. By determining the duty cycles $d\gamma$ and $d_\delta$ with the modulation index $m_R$ = 1, the rectification stage's duty cycles are then adjusted using $d_\gamma^R = \frac{d_\gamma}{d_\gamma + d_\delta}$,

$d_\delta^R = -\frac{d_\delta}{d_\gamma + d_\delta}$ to occupy the whole switching period.

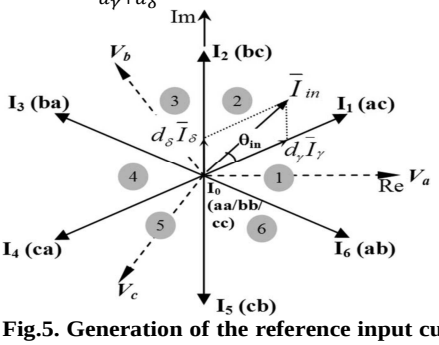


**Fig.5. Generation of the reference input current vector *I*in at the rectification stage**

**Table 2. Duty-Cycle equations for selected vectors of each triangle**

| Triangle | $d_x$ | $d_y$ | $d_z$ |
|---|---|---|---|
| T1[$\Delta EFH$] | $m_u\left(\sqrt{3}\cos\theta_{out} - \sin\theta_{out}\right)$ | $2m_u \sin\theta_{out}$ | $1-m_u\left(\sqrt{3}\cos\theta_{out} + \sin\theta_{out}\right)$ |
| T2[$\Delta FIH$] | $2-m_u\left(\sqrt{3}\cos\theta_{out} + 3\sin\theta_{out}\right)$ | $2-2\sqrt{3}m_u \cos\theta_{out}$ | $3m_u\left(\sin\theta_{out} + \sqrt{3}\cos\theta_{out}\right) - 3$ |
| T3[$\Delta FGI$] | $2-m_u\left(\sqrt{3}\cos\theta_{out} + 3\sin\theta_{out}\right)$ | $\sqrt{3}m_u \cos\theta_{out} - 1$ | $3m_u \sin\theta_{out}$ |
| T4[$\Delta GJI$] | $0.5m_u\left(3\sin\theta_{out} + \sqrt{3}\cos\theta_{out}\right) - 1$ | $2-2\sqrt{3}m_u \cos\theta_{out}$ | $1.5m_u\left(\sqrt{3}\cos\theta_{out} - \sin\theta_{out}\right)$ |
| T5[$\Delta HIJ$] | $0.5m_u\left(3\sin\theta_{out} + \sqrt{3}\cos\theta_{out}\right) - 1$ | $\sqrt{3}m_u \cos\theta_{out} - 1$ | $3 - 1.5m_u\left(\sqrt{3}\cos\theta_{out} + \sin\theta_{out}\right)$ |

Due to the zero-current vector cancellation, the average DC-link voltage is no longer constant and needs to be recalculated so its value can be used to compensate the modulation index of the inversion stage $m_u$.

$V_{pn\_avg} = d_\gamma^R V_{l\_l\gamma} + d_\delta^R V_{l\_l\delta}$ , $m_U = \frac{\sqrt{3}*|V_{out}|}{V_{pn-avg}}$

### 3.2. The Inversion Stage

For the inversion stage, the NTV SVM scheme is applied to control the NPC VSI due to its effective-ness in controlling the neutral-point balancing problem. As shown in Figure 1, the NPC VSI is used as the inversion stage of the three-level output-stage matrix converter. The connection from the DC-link middle point '*o*' to the neutral- point of the star-connected input filter capacitors is essential to provide the required dual voltage supplies and a zero voltage middle point. However, this connection causes the flow of neutral-point current $I_o$when the output phase is connected to the neutral-point o (the neutral-point balancing problem of NPC VSI). Without proper control over the neutral-point current, uneven changing potential level of the star connected input capacitors would directly distort the line to-line output voltage. The NTV SVM scheme is able to maintain zero average value of the neutral-point current over a sampling period so that the neutral-point potential of the star-connected input capacitors can be maintained.

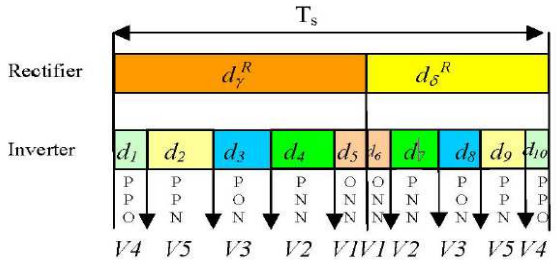


**Fig.6 Switching pattern of the I3MC**

**Table 3. Circuit specifications**

| Circuit specifications | Value |
|---|---|
| Input | $V_{in-line} = 400V_{rms}, f_{in} = 50Hz$ |
| Filter | $L_f = 0.633mH, C_f = 10\mu F$ |
| Load | R=10$\Omega$,L=10mH |
| Output frequency | $f_{out} = 30Hz$ |
| Switching frequency | $f_{sw} = 4kHz$ |

### 3.3. The Switching Pattern for I3MC

In order to maintain the balance of the input currents and the output voltage in the same switching period, the modulation pattern for the SMC3 should combine the switching states of the rectification stage ($I_\gamma$ and $I_\delta$) and the inversion stage ($V_x$, $V_y$ and $V_z$) uniformly, producing a switching pattern presented in Fig 7. Let's consider for example that $I_{in}$is located at sector 2 while $V_{out}$ is located inside triangle 4 of sector 1. For the rectification stage, the selected current vectors are: $I_1\left(=I_\gamma\right)$ and $I_2(=I_\delta)$. On the other hand, selected vectors for the inversion stage are:$V_{MV1}(=V_z)$, $V_{LV1}\left(=V_y\right)$ and $V_{LV2}(=V_x)$. Based on the NTV SVM, these virtual vectors are formed by voltage vectors: VI (ONN), V2 (PNN), V3 (PON), V4 (PPO) and V5 (PPN).

For the inversion stage, selected voltage vectors are arranged in a double-sided switching sequence: V4 - V5 - V3 - V2 - VI - VI - V2 - V3 - V5 - V4, but with unequal halves because each half should apply on a rectifier switching sequence: $I_1 - I_2$. By referring to Fig 7, the duty cycles of the inverter switching sequence can be determined with (5).

$d_1 = d_z * d_\gamma^R * C_7$; $d_2 = d_x * d_\gamma^R$; $d_3 = d_z * d_\gamma^R * C_6$;
$d_4 = d_y * d_\gamma^R$; $d_5 = d_z * d_\gamma^R * C_5$; $d_6 = d_z * d_\delta^R * C_5$;
$d_7 = d_y * d_\delta^R$; $d_8 = d_z * d_\delta^R * C_6$; $d_9 = d_x * d_\delta^R$;
$d_{10} = d_z * d_\delta^R * C_7$…(5)

## 4. Simulation Results

The model of the I3MC presented in Fig.1 has been simulated with MATLAB/SIMULINK. Fig.7 & 8 shows the output phase voltage wave forms and their FFT.Fig.9 & 10 gives the FFT of wave forms. From the results we can observe that %THD of wave forms is 64% approx. when the circuit is modulated using SPWM technique. Fig.11, 12, 13 & 14 represents the phase, line voltages, output current and its FFT when SVPWM technique is implemented on Fig.1.Table 4 gives the comparison of SPWM and SVPWM techniques.

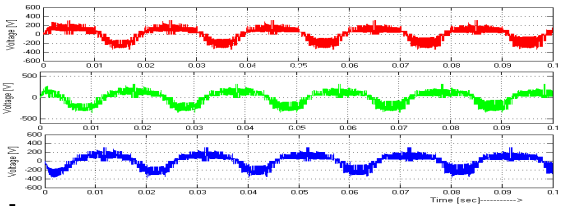


**Fig.7 Output Phase Voltages of Three Level Indirect Matrix Converter-SPWM technique**

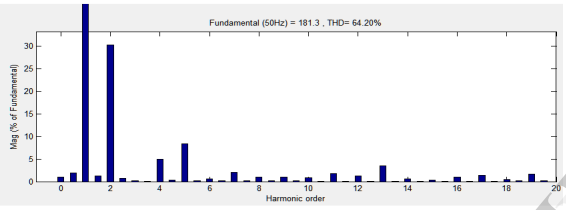


**Fig.8. FFT Analysis of Output Phase Voltages of Three Level Indirect Matrix Converter**

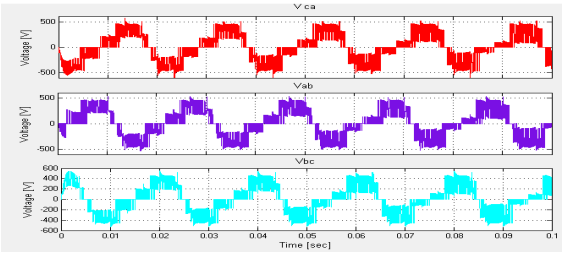


**Fig.9. Output Line Voltages of Three Level Indirect Matrix Converter-SPWM technique**

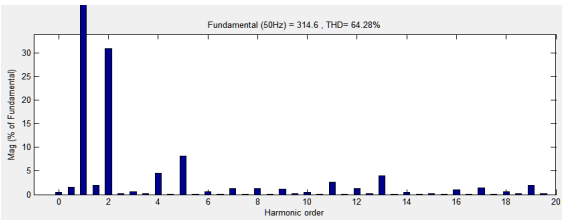


**Fig.10. FFT of output line voltages of three level indirect matrix converter**

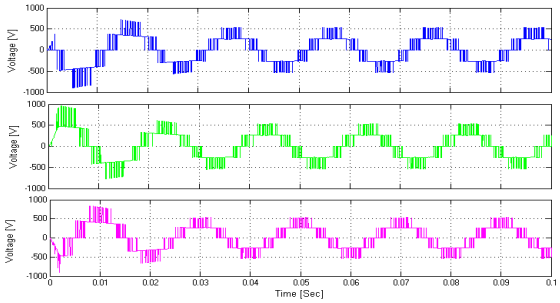


**Fig.11 Output Phase Voltages of Indirect Matrix Converter when Implemented Using SVPWM Technique**

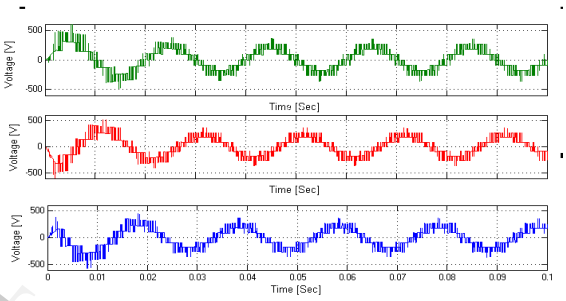


**Fig.12. Output line voltages of indirect matrix converter when implemented using SVPWM technique**

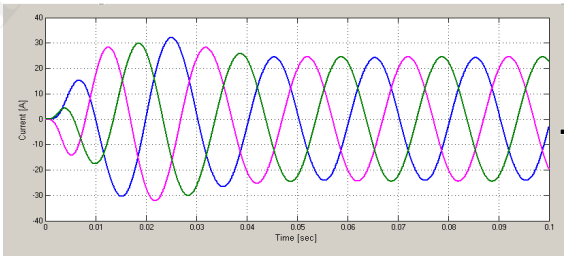


**Fig.13. Output currents of indirect matrix converter when implemented using SVPWM technique**

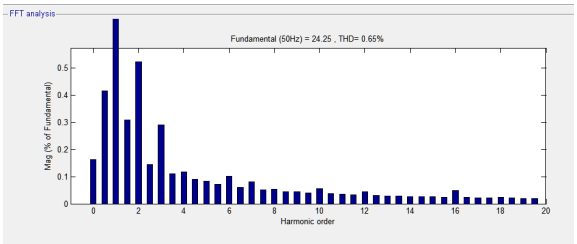


**Fig.14 FFT of output currents of indirect matrix converter when implemented using SVPWM technique**

**Table 4. Comparison of controlling techniques for indirect matrix converter**

| | SPWM technique | | | SVPWM technique | | |
|---|---|---|---|---|---|---|
| | Output voltage (peak) in volts | Output voltage( RMS) in volts | % THD | Output voltage (peak) in volts | Output voltage( RMS) in volts | % THD |
| Phase voltage | 181.3 | 127.98 | 64.2 | 207.4 | 146.6 | 41.37 |
| Filtered phase voltage | 153 | 108.18 | 9.05 | 174.7 | 123.5 | 0.36 |
| Line voltage | 314.6 | 222.45 | 64.28 | 360.7 | 255 | 41.53 |
| Filtered line voltage | 263.8 | 186.53 | 9.88 | 300.6 | 212.5 | 0.33 |

## 5. Conclusion

In this paper, a new space vector pulse width modulation technique for the three-level-indirect matrix converter topology is presented. By applying the proposed modulation technique, the three-level-indirect matrix converter is able to synthesize three-level voltage and also able to maintain sinusoidal input currents. A comparison based on MATLAB/ simulation results reveal that the three-level-indirect matrix converter produces better output performance with SVPWM technique in terms of reduced harmonic contents and increased DC bus utilization when compared to a SPWM technique.

## 6. Appendix A

| Circuit specifications | Value |
|---|---|
| Input | $V_{in-line} = 400V_{rms}, f_{in} = 50Hz$ |
| Filter | $L_f = 0.633mH, C_f = 10\mu F$ |
| Load | R=10$\Omega$,L=10mH |
| Output frequency | $f_{out} = 30Hz$ |
| Switching frequency | $f_{sw} = 4kHz$ |
| Output filter (LP 2nd order) | Cut off frequency=50Hz, Damping factor=0.6 |

## 7. References

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