Scaling Down Area – Delay - Power Efficient of Carry Select Adder Using GDI

[1]S. R. Baliji, [2]Dr. R. Manikandan, [3] V. Vasudhevan
[1] Assistant Professor (Grade-1), [2] Professor, [3]Assistant Professor
Department of Electronics and Instrumentation Engineering
Panimalar Engineering College,Chennai,India

ABSTRACT— The Modified Gate Diffusion Input logic (Mod-GDI) is a novel technique for low power digital circuit design. This technique reduces the power dissipation, propagation delay, area of digital circuits. One of the fastest adders used in many data-processing processors to perform fast arithmetic function is Carry Select Adder. Simulations are done using Tanner EDA. We have omitted all the redundant logical operations in the conventional Carry Select Adder (CSLA) and proposed a new logic formulation for CSLA. In the proposed system, the carry select (CS) operation is done before the calculation of the final sum, which differs from the other conventional approach. This simulation results shows nearly 45% of reduction in power-delay product using Mod-GDI.
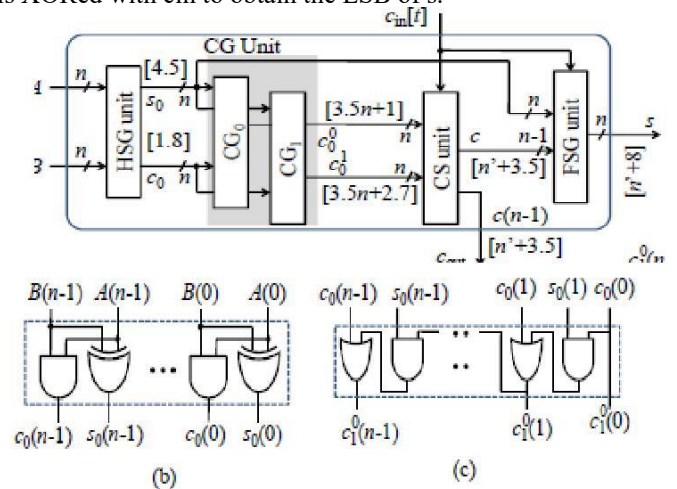
I. INTRODUCTION

LOW-POWER, area-efficient, and high-performance VLSI systems are increasingly used in portable and mobile devices, multi standard wireless receivers, and biomedical instrumentation. An adder is the main component of an arithmetic unit. A complex digital signal processing (DSP) system involves several adders. An efficient adder design essentially improves the performance of a complex DSP system. Power dissipation becomes most important restriction in high performance applications. Optimizations for basic logic gates are fundamental constraint in order to get better the performance of a variety of low power and high performance devices. Morgenshtein et al. investigated a high-speed and multipurpose logic style for low power electronics design, known as Gate Diffusion Input (GDI), with reduced area and power necessities, and proficient of implementing a broad variety of logic functions. But this basic Gate Diffusion Input (GDI) logic style suffers from some practical limitations like swing degradation, fabrication complexity in standard CMOS process and bulk connections. These limitations can be overcome by modified gate diffusion input (Mod-GDI) logic style.

II. EXISTING SYSTEM

The Existing CSLA is based on the logic formulation given in 1(a) to 1(g) and its structure is shown in Fig. 1. It consists of one HSG unit, one FSG unit, one CG unit, and one CS unit. The CG unit is composed of two CGs (CG0 and CG1) corresponding to input-carry '0' and '1'. The HSG receives two n -bit operands (A and B) and generate half-sum word s0 and half-carry word c0 of width n bits each. Both CG0 and CG1 receive s0 and c0 from the HSG unit and generate two n -bit full-carry words c01 and c11 corresponding to input-carry '0' and '1', respectively. The logic diagram of the HSG unit is shown in Fig. 1(b). The logic circuits of CG0 and CG1 are optimized to take advantage of the fixed input-carry bits. The optimized designs of CG0 andCG1 are shown in Fig. 1(c)

respectively.

The CS unit selects one final carry word from the two carry words available at its input line using the control signal cin . It selects c01 when cin= 0 ; otherwise, it selects c11 . The CS unit can be implemented using an n -bit 2-to-l MUX. However, we find from the truth table of the CS unit that carry words c01 and c11 follow a specific bit pattern. If c01 (i) = '1 ', then c11 (i) = 1 ,irrespective of s0(i) and c0(i) , for $0 \le i \le n - 1$. This feature is used for logic optimization of the CS unit. The optimized design of the CS unit is shown in Fig. 1(e), which is composed of n AND –OR gates. The final carry word c is obtained from the CS unit. The MSB of **c is sent to output as cout, and (n − 1) LSBs are XORed with (n − 1) MSBs of half**-sum (s0) in the FSG [shown in Fig. **1(f)] to obtain (n − 1) M**SBs of final-sum(s). The LSB of s0 is XORed with cin to obtain the LSB of s.

(b)   (c)

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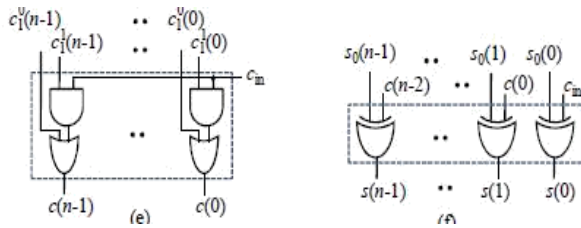**ISSN: 2278-0181**
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Figure 1. (a) Proposed CS adder design, where n is the input operand bit-width, and [ ] represents delay (in the unit of inverter delay), n = max(t, 3.5n + 2.7). (b) Gate-level design of the HSG. (c) Gate-level optimized design of (CG0) for input-carry = 0. (e) Gate-level design of the CS unit.
(f) Gate-level design of the final-sum generation (FSG) unit.

The selected carry word is added with the half-sum (s0) to generate the final-sum (s) .Using this method, one can have three design advantages:1) Calculation of s01is avoided in the SCG unit; 2) the n –bit select unit is required instead of the (n + 1) bit; and 3) small output-carry delay. All these features result in an area–delay and energy-efficient design for the CSLA. The proposed logic formulation for the CSLA
is given as

$s0(i) = A(i) \quad B(i) \quad c0(i) = A(i) . B (i)$ ---- (1a)
$c01 (i) = c01(i − 1) . s0 (i) + c0 (i)$ for _ c01 (0) = 0 ---- (1b)
$c11 (i) = c11(i − 1) . s0 (i) + c0 (i)$ for _ c11 (0) = 1 ---- (1c)
$c (i) = c01(i)$ if (cin= 0)
---- (1d)
$c (i) = c11(i)$ if (cin= 1)
---- (1e)
$Cout = c (n − 1)$ ---- (1f)
$s (0) = s0 (0) \quad cins(i) = s0(i)$ ---- (1g)

$$\oplus \qquad \oplus c(i − 1).$$

III. PROPOSED ADDER DESIGN

The Proposed technique is the Gate Diffusion Input Technique here one of the inputs are directly diffused into the gates of the transistors of N-type and P-type devices so it called the gate diffused input technique. Gate Diffusion Input technique scales down power dissipation, propagation delay, and area of digital circuits. This method is based on the simple cell. basic GDI cell contains four terminals they are G (common gate input of NMOS and PMOS transistors), P (the outer diffusion node of PMOS transistor), N (the outer diffusion node of NMOS transistor), and D (common diffusion node of both transistors). The basic GDI cell, and implementation of AND, OR logics are given in fig 2(a).
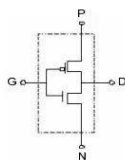

Figure 2. (a)Basic GDI cell

TABLE I. LOGIC FUNCTION OF GDI

N	P	G	D	Function
0	B	A	A*B	F1
B	1	A	A+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
0	B	A	AB+C	MUX
0	1	A	A	NOT

Any logic functions can be implemented using GDI Technique. The Table I gives us the information about the logic functions which are implemented by the Gate Diffusion Input. The working of GDI based AND gate can be explained in comparison to basic GDI cell 'P' of the transistor is given '0' it will cut-off from its operation, thus the logic either '1' or '0' at the input'a' will be reflected at the output 'z'. Hence the output will be z =a*b.
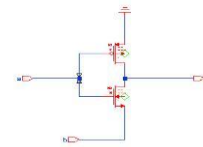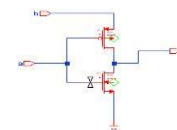

Figure 3. AND Logic

Figure 4. OR Logic

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A. IMPLEMENTATION OF GDI DIGITAL CIRCUITS

We will minimize the power dissipation using GDI technique. Therefore, the 4×1 Multiplexer, 8×3 Encoder, BCD Counter and Mealy Machine were implemented with the Pass Transistor, Transmission Gate and Gate Diffusion Input. Among those, circuits which are implemented using GDI technique are discussed here. The design of 4×1 Multiplexer by GDI Technique was given in 5.
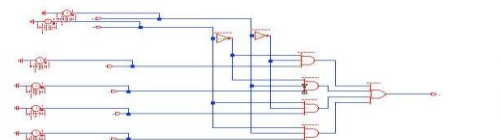

Figure 5. 4x1 Multiplexer using GDI.

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Mealy machine is one of the finite state machine that depend upon the states and given inputs. The main advantage in this state machine is used to reduce the number of states. The mealy machines are developed by using Pass Transistors, Transmission Gates and Gate Diffusion Input. The power dissipation of the Mealy Machine are compared and tabulated. The Mealy machine is given in 6.
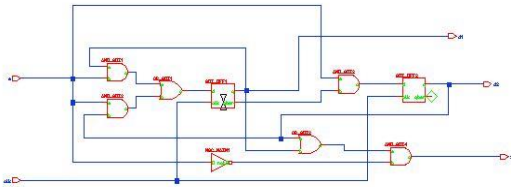

Figure 6.   Mealy machine using GDI

B.   RESULTS

The power dissipation values are analyzed under given different supply voltages of the designed circuits and they were compared with each other. Thus, it was noted that, the designed digital circuits dissipate minimum amount of power using GDI technique.

TABLE II.   POWER DISSIPATION FOR 4x1 MUX

S.NO	Technique used	Power dissipation (µW)
1	Pass Transistor	5.609
2	Transmission gate	18.78
3	GDI	2.477

TABLE III.   POWER DISSIPATION FOR MEALY MACHINE

S.NO	Technique used	Power dissipation
1	Pass Transistor	10.1605 µW
2	Transmission gate	15.0021 µW
3	GDI	185.7002 PW

IV.   PERFORMANCE COMPARISON

We have considered all the gates to be made of 2-input AND, 2-input OR, and inverter (AOI). A 2-input XOR is composed of 2 AND, 1 OR, and 2 NOT gates.

TABLE IV.   AREA AND DELAY OF AND, OR, AND NOT GATES GIVEN IN THE SAED 90-nm STANDARD CELL LIBRARY DATASHEET

Area/ Delay	AND – gate	OR – gate	NOT - gate
Area (um^2)	7.37	7.37	6.45
Delay (ps)	180	170	100

The area and delay of the 2-input AND, 2-input OR, and NOT gates (shown in Table II) are taken from the Synopsys Armenia Educational Department (SAED) 90-nm standard cell library datasheet for theoretical estimation.

The area and delay of a design are calculated using the following relations:

$$A = a. \ Na + r \ . \ No + i. \ Ni \quad (3a)$$

$$T = na. \ Ta + no \ . \ To + ni. \ Ti \quad (3b)$$

where $(Na, \ No, \ Ni)$ and $(na, no, \ ni)$, respectively, represent the (AND , OR , NOT) gate counts of the total design and its

critical path. (a, r, i) and (Ta, To, Ti), respectively, represent the area and delay of one (AND , OR , NOT) gate. We have

calculated the (AOI) gate counts of each design for area and delay estimation. Using (2a) and (3b), the area and delay of each design are calculated from the AOI gate counts (Na,No,Ni), (na, no, ni), and the cell details of Table 2.

The proposed method involves 29% less area and 5% output delay than [6]. And also CSLA of [6] involves 40% higher ADP than proposed CSLA, on average, for different bit widths. Compared with Common Boolean Logic (CBL) based CSLA of [7], the proposed CSLA design has marginally less ADP. However, CBL based CSLA delay increases at greater rate than the proposed method. But proposed method provides multi path parallel carry propagation, whereas CBL based CSLA [7] provides only single path carry propagation path similar to the Ripple Carry Adder (RCA) design. In addition, the proposed design has only 0.4ns less carry output delay than the sum output delay. This happens mainly because of CS unit which gives carry output before Full Sum Generation (FSG) calculate the final sum

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TABLE V. THEORETICAL ESTIMATE OF AREA AND DELAY
COMPLEXITIES OF THE PROPOSED AND EXISTING CSLAs
[4]

Design	width (n)	Area (um^2)	Delay (ns)		ADP ($um^2.us$)	EADP (%)
			fs	c_{out}		
CONV	8	1438.12	3.45	3.35	4.96	35
	16	2934.28	6.25	6.15	18.34	43
CSLA [6]	8	1282.45	4.08	4.08	5.23	42
	16	2587.01	6.88	6.88	17.80	39
CSLA [7]	8	906.56	3.78	3.78	3.42	−7.0
	16	1813.12	7.38	7.38	13.38	4.0
CSLA [8]	8	1654.65	7.30	7.30	12.08	228
	16	3416.17	14.50	14.50	49.55	286
Prop.	8	951.09	3.87	3.42	3.68	——
	16	1924.30	6.67	6.22	12.83	——

CONV: conventional, ADP: area delay product, EADP: excess ADP over
the proposed design, ADP: area× delay, delay of fs represents adder
delay.

V. CONCLUSION

We have concluded all the redundant logic operations of
the conventional CSLA and proposed a new logic
formulation for the CSLA. The proposed system has the CS
operation which is scheduled before the calculation of final-
sum and it is different from the conventional approach. In
this paper an approach is presented for minimizing power
consumption for digital circuits at the logic style level and
DC and Transient analysis of basic logic gates has been done
using Mod-GDI logic style. Simulation results shows up to
45% reduction in power-delay product in Mod-GDI. Mod-
GDI approach allows realization of a broad variety of
multifaceted logic functions by means of only two
transistors. Mod-GDI gates lower the transistor count and in
turn the silicon area required when compared to standard
static CMOS and Domino CMOS based approaches. The
leakage power and switching power of Mod-GDI gates is
lower than the traditional logic styles. The problem of
fabrication of GDI gates in standard nano-scale CMOS
process is overcome by connecting the sources of pMOS and
nMOS to VDD and GND respectively in Mod-GDI logic
style. The problem of threshold drop is not a very serious
issue in deep sub-nm regions. The Mod-GDI logic style
based design adopts interruption of inverter to alleviate the
problem of signal degradation during propagation. The
proposed Mod-GDI logic style based designs can be taken a
better alternative in future.

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