International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 4 Issue 05, May-2015

SDR – Implementation of Low Frequency Trans-Receiver on FPGA

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Abstract— **with the increasing requirements of the wireless industry, software defined radios have been widely used for modulation and coding techniques. For complex design systems of the radio the SDR is the basic element to be considered. The component can be programmed again and again so as to perform many functions making it configurable. To achieve such reprogrammed radio components FPGA is the best suited platform. Design implementation of the low frequency transceiver uses vitrex5 device. System level models and designs can be carried out using system generator. The same can also be used to obtain utilization of resources and timing results before hardware execution.**

Keywords—Quadrature phase shift keying,low pass filter,direct digital synthesis,cosine filters,xilinx.

I. INTRODUCTION

SDR has given an outstanding contribution to the wireless industry with its advanced applications and various tools. The components like transmitter, receiver, carrier frequency, bandwidth of the signal can be implemented using software with the help of software radio. Complex design systems which consist of many frequencies and waveforms can also be designed using SDR. The basic idea behind is to solve the problem of hardware using software analysis. This approach is more advantageous because of its low cost and efficiency. The low frequency transceiver using FPGA is feasible to implement and is easily upgradable. Redesign and reusage of the components is the key factor of the SDR device. The change in the specification is entertained so that the SDR updates the modification and loads back to the FPGA device saving both cost as well and time.

The modulation technique used here is the QPSK digital modulation in which pair of bits represents a symbol and as a result the data rate is increased by a factor of 2. The main reason to adopt this technique is to synchronize the carrier at the receiver. The Inphase and the quadrature components are the 2 bit symbols obtained using qpsk. These components are used for carrier phase modulation. Logical 1's and 0's yield four combinations containing 2 bits and the phase of the carrier can be shifted to one of the four states and then transmitted. The QPSK model is obtained by combining two BPSK signals using two orthogonal carriers with sine and cosine components. Down conversion of the received signal yields the baseband signal.

Efficiency of the modulation scheme decides the radio system performance. The two main important factors that decide the overall efficiency of the modulation scheme are power and bandwidth efficiency. Power efficiency is the ability of a modulation technique to preserve the quality of the signal with minimum signal power. It is defined as the ratio of signal energy per bit to noise spectral density(Eb/No) .Bandwidth efficiency is the ability of a modulation technique to transfer more data at the given bandwidth, which decides the system/channel capacity. It is defined as the ratio of data rate in bits per second to allocated bandwidth in Hertz. There exists a fundamental tradeoff in any communication system between the power efficiency and bandwidth efficiency as one can be achieved only at the expense of the other

II. LITERATURE REVIEW

The author quotes the implementation of the SDR transceiver model in which QAM is the most important key technique necessary for the cellular and wireless system communication [1]. Due to its bandwidth force and power efficiency the QAM is most often used in adaptive modulation. AWGN Wireless channels are used for setting the parameters for random generator, modulation and demodulation. The error rates of QAM against SNR evaluate the QAM system. The transmitter and receiver can transceiver frequency of 40MHZ maintaining the power of FPGA slices limited. The performance and speed can also be enhanced using the efficient software.

The author states the implementation of SDR based wireless system which uses partial reconfigurable FPGA for power reduction [2].ASK and FSK modulation techniques have been widely used. The SDR with partial reconfiguration changes some portions of the FPGA while other keeps functioning. The speed and performance can be improved and the area can be decreased using this technique.

III. DESIGN METHODOLOGY

The main components being used for the design methodology are transmitter and receiver units. The transmitter unit includes the random data generator, Map circuit, digital direct synthesis, the adding unit and the multiplier unit. The receiver unit includes the Band pass filter, Decision making circuit and the Demap circuit. The main modulation used in this methodology is Quadrature phase shift keying.

QPSK Theory:

The information on the baseband signal must be modulated on to a microwave carrier to transmit and receive from the satellite. QPSK signal generates symbols for the phase modulation. Higher PSK signals can also be used to send 3 or 4 bits to increase the data rates to the higher level. The QPSK signal can be represented with the help of a equation as follows.

$$S(t)= \cos(2\Pi fct+\Phi(t))=I(t)\cos(2\Pi fct)-Q(t)\sin(2\Pi fct)$$

Where I and Q are inphase and quadrature components, fc represents carrier frequency. Both I and Q carry information of one bit each.

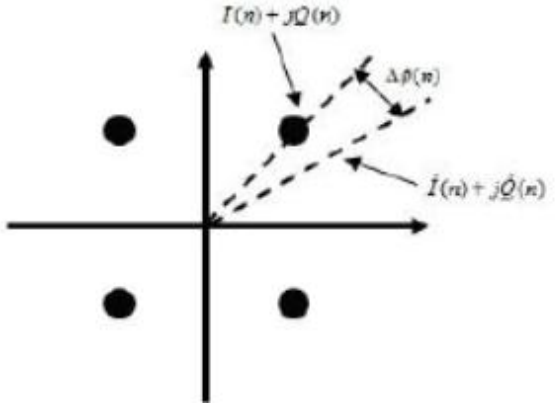

Fig1: Constellation diagram

The signal which is received is demodulated and the data is decoded from the same received signal. This data can be represented in the form of constellation figure on X-Y plane which is represented in terms of symbols. The symbols are represented at 45,135,225 and finally 315 degrees .The 2 bits of information is obtained from each symbol and based on their positions in the constellation the data can be decoded .Since the data can be represented in the quadrant where the symbol resides, this modulation is rightly described as quadrature modulation.

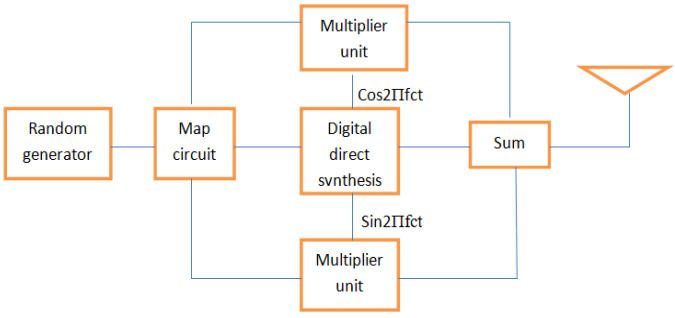

Fig2: Transmitter Unit

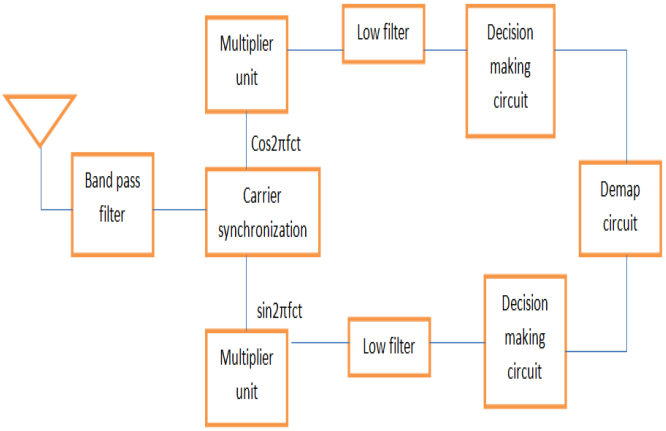

Fig3: Receiver Unit

The transceiver is explained as follows, the data generator generates a random sequence of 32 bits having data rate of 50 kHz which is converted from serial to parallel using demux to obtain quadrature and in phase components. These components are later fed to the unipolar to bipolar converter. Map circuit defines all the functions after generation of the signal. Digital Direct synthesis helps the pulse shaping of the components which uses cosine filters so that the noise components are removed. The streamed signal is then multiplied with the sine and cosine carrier signal of 1 MHz and later summed to obtain the modulated signal which gets transmitted. The data rate reduces to 25 KHz as QPSK modulation needs 2 bits for changes in phase. With the carrier signal multiplication followed by the filtration the Demodulating signal is obtained .FIR filter is used here which provides filtered output with delay being fixed. The filtered signal is then multiplexed and the demodulated data is obtained using down sampling.

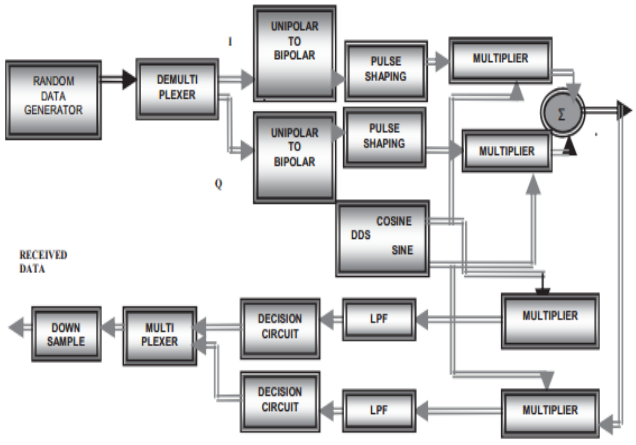

Fig4: Block diagram of transceiver

Fig4 represents the block diagram of the practical working of the low Frequency Transceiver. The analysis of the diagram is already explained with their respective blocks earlier. The modulation of the data as well as demodulation of the same can be obtained with the help of SDR transceiver .the same can also be used for error coding and decoding.

IV. RESULTS

The following results have been obtained from the above analysis after the modulation and demodulation of the baseband signal. The matlab simulink generator has been used as a environment to the Xilinx software to execute the results efficiently

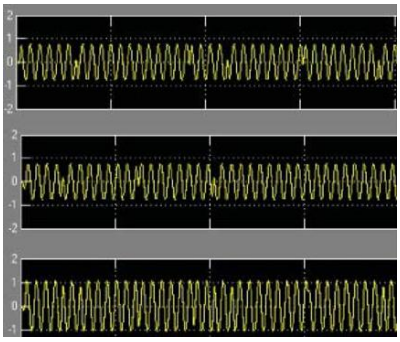

Fig5: phase changes of I, Q and QPSK carrier

Fig5 shows the phase changes in the in phase, quadrature and QPSK carrier after modulation. Fig6 represents the pulse shaping filters frequency response. The noise in the output is removed by pulse shaping of the filter. One most common pulse-shaping filters used in communications systems is raised cosine filter. It minimizes the intersymbol interference by reducing the signal strength of the starting and ending portions of the symbol period.

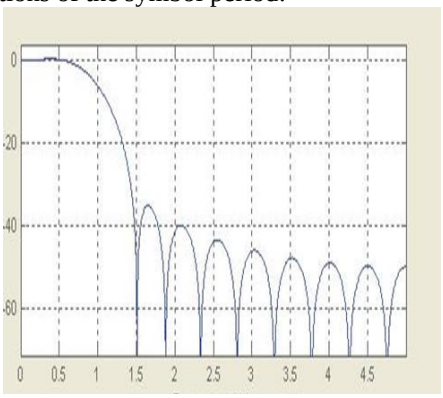

Fig 6: Frequency response of pulse shaping filter

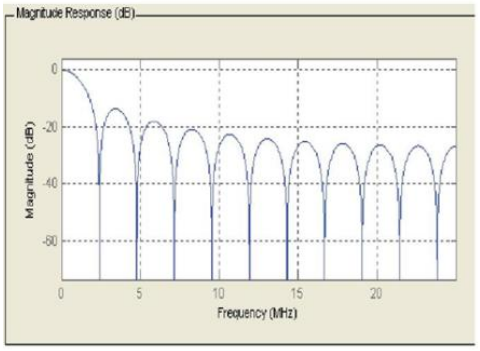

Fig7: Frequency response of low pass filter

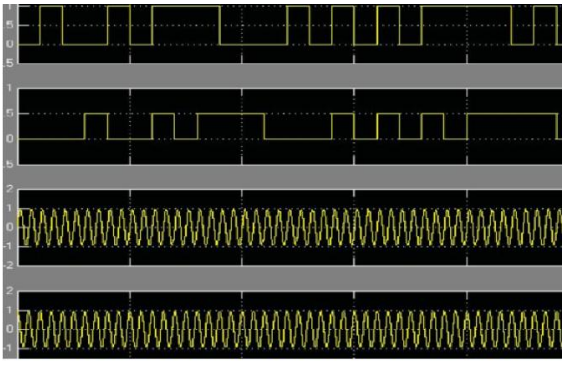

Fig8:Transmitted and received data

Fig7 indicates the frequency response of the low pass filter which is meant to filter high frequency components. Fig8 represents the data being transmitted and received after demodulation with a delay being fixed.

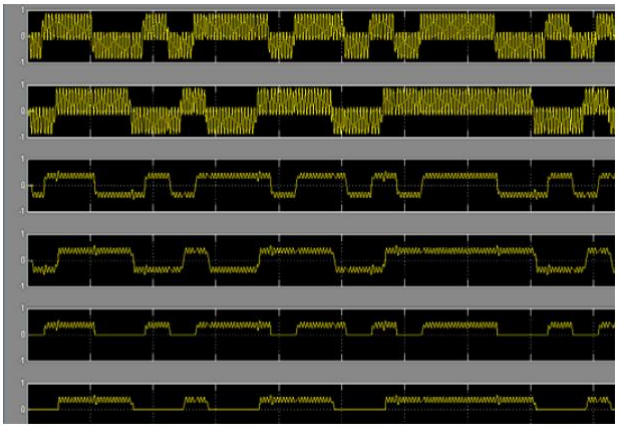

Fig9: Coherent demodulated signals

Fig 9 represents the coherent demodulated signals in which the sine and cosine carriers are multiplied with the modulated carrier and also with the output of low pass filter and the decision circuit.

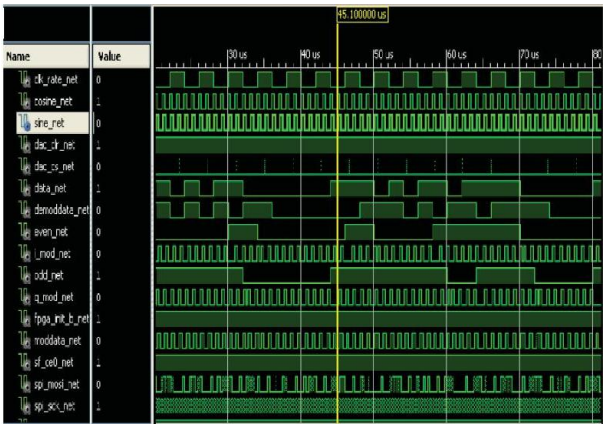

Fig10: Xilinx test bench output

Fig10 represents the Xilinx testbench output with parameters including in phase and quadrature along with the sine and cosine carriers. The data and the demodulated data outputs are also clearly seen using the same test bench.

V. CONCLUSION

The low frequency transmitter and receiver using software radio are implemented on the FPGA platform. The results show that the input of transmitter and output of the receiver match with each other. The overall idea behind this paper is to execute the problem of hardware in to the software. Since it can be reprogrammed it is efficient and requires low cost to implement. Designs with different data rates can also be carried out using FPGA platform.

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