Selective Harmonic Elimination PWM in Cascaded Multilevel Inverter for Harmonic Reduction by Using Controller

P.Thenmozhi
PG Student,Department of EEE
M.Kumarasamy College of engineering
Karur,Tamil nadu,India.
eeethenu@gmail.com

P.Maniraj
Asst.Professor,Dept of EEE
M. Kumarasamy College
of Engineering, Karur,
Tamilnadu,India
maniraj.angu@gmail.com

***Abstract* — Selective Harmonic Elimination Pulse Width Modulation (SHEPWM) method is systematically applied to multilevel Flying Capacitor Type Clamped Inverter Called PWM inverters. The method is implemented based on optimization techniques for reduction of Harmonics of Non Linear Loads. The optimization starting point is obtained using a phase-shift harmonic suppression approach. This paper proposes a hybrid selective harmonic elimination pulse width modulation (SHEPWM) scheme for Harmonics reduction in Non Linear Loads using flying Capacitor Type three Level Inverter. The scheme uses the SHEPWM to control the inverter at low frequency. In this method the Total Harmonic Distortion (THD) is reduced by using SHEPWM in closed loop. Finally the THD is compare with, before and after LCL filtering condition. Here the THD should be reduced in nonlinear loads by using a flying capacitor type clamped inverter topology. This proposed topology involves less number of switches. It dramatically reduces the switches for high number of levels that reduces the switching losses; cost and low order harmonics and thus effectively decreases total harmonics distortion. The Results are simulated using MATLAB Simulink and Outputs are notified and Control Graphs are obtained.**

***Keywords:* selective harmonic elimination pulse width modulation(SHEPWM),Cascaded multi level inverter, total harmonic distortion(THD),PI Controller, Neuro Fuzzy Controller .**

I. INTRODUCTION

The concept of multilevel converters has been introduced since 1975. Multilevel inverter have been gained more attention for high power application in recent years which can operate at high switching frequencies while producing lower order harmonic components, A multilevel inverter not only achieves high power ratings, but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind, and fuel cells can be easily interfaced to a multilevel inverter system for a high power application. There are several topologies such as neutral point clamped inverter; flying capacitor based multilevel, cascaded H-bridge multilevel inverter, hybrid H-bridge multilevel inverter and new hybrid H-bridge multilevel inverter. Under this condition neutral point clamped multilevel inverter is presented, which has a simple structure and good performance .This topology effectively reduce the higher input dc voltage that each device must withstand. The main disadvantage still exists in this topology, which restricts the use of it to the high power range of operation.

Multilevel inverters are significantly different from the ordinary inverter where only two levels are generated. The semiconductor devices are not connected in series to for one single high-voltage switch. In which each group of devices contribute to a step in the output voltage waveform. The steps are increased to obtain an almost sinusoidal waveform. The number of switches involved is increased for every level increment. Figure 1 shows the block diagram of the general multilevel inverter.

Generally, the output waveform of the multilevel inverter is generated from different voltage sources obtained from the capacitor voltage sources. In the past two decades, several multilevel voltage source converters have been introduced. In that some of the topologies are popular and some are not popular.

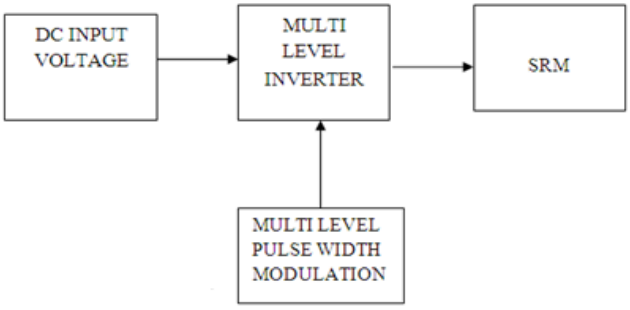

Fig.1.Block Diagram of General Multilevel Inverter

Multilevel inverter have been gained more attention for high power application in recent years which can operate at high switching frequencies while producing lower order harmonic components, A multilevel inverter not only achieves

high power ratings, but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind, and fuel cells can be easily interfaced to a multilevel inverter system for a high power application .There are several topologies such as…

- Diode –clamped Multi-level inverter
- Flying –capacitor Multi-level inverter
- Cascade Multi-level inverter

Multilevel inverter have been gained more attention for high power application in recent years which can operate at high Switching frequencies while producing lower order harmonic components [1]-[4],A multilevel inverter not only achieves high power ratings, but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind, and fuel cells can be easily interfaced to a Multilevel inverter system for a high power application [3]. There are several topologies such as neutral point clamped inverter; flying capacitor based multilevel, cascaded H-bridge multilevel inverter, hybrid H-bridge multilevel inverter and new hybrid H-bridge multilevel inverter [4]. This paper discusses the operation of different topologies for multilevel inverter which can produce multilevel; under this condition neutral point clamped multilevel inverter is presented, which has a simple structure and good performance .This topology effectively reduce the higher input dc voltage that each device must withstand. The main disadvantage still exists in this topology, which restricts the use of it to the high power range of operation.

II. CACADED MULTI LEVEL INVERTER

There is a growing interest in multilevel topologies since they can extend the application of power electronics systems to higher voltages and power ratios. Multilevel inverters are the most attractive technology for the medium to high voltage range, which includes motor drives, power distribution, power quality and power conditioning applications. A cascaded multilevel inverter by Corzine et al (1999) Liu et al (2006) consists of a series of H-bridge inverter units. The general function of this multilevel inverter is to synthesize a desired voltage from several separate DC sources, which may be obtained from batteries, fuel cells, or solar cells. A particular advantage of this topology is that the modulation, control and protection requirements of each bridge are modular. The cascaded inverter has been largely studied and used in the various fields such as drives, transmission system and power conditioning Corzine et al (2002)..

The main drawback of this topology is complicated to track the voltage levels for all of the capacitors. Also the pre charging of all the capacitors to the same voltage level and startup are complex. Switching utilization and efficiency are poor for real power transmission. The large numbers of capacitors are more expensive and bulky than clamping diodes in multilevel diode-clamped converters. Packaging is also difficult in inverters with a high number of levels.

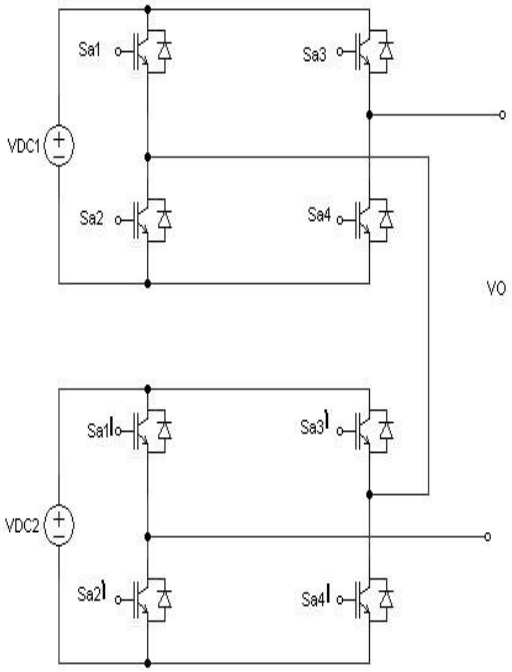

Figure 2. Structure of single phase three level cascaded multilevel inverter

II.A. Features Of Multilevel Inverters

- The series structure allows a scalable, modularized circuit layout and packaging since each bridge has the same structure.
- Requires the least number of components among all multilevel converters to achieve the same number of voltage levels without no extra clamping diodes or voltage balancing capacitors.
- Soft switching techniques can be implemented which reduces switching losses and device stresses.
- Potential of shock is reduced due to the separate DC sources.

II.B. Advantages

- The multi-level inverter is to synthesize a near sinusoidal voltage from several levels of dc voltages.
- As number of levels increases, the synthesized output waveform has more steps, which provides a staircase wave that approaches a desired waveform.
- Also, as steps are added to waveform, the harmonic distortion of the output wave decreases, approaching zero as the number of voltage levels increases.

III.PROPOSED MODEL

In proposed model using SHEPWM in flying capacitor type clamped inverter for non linear loads. The THD should reduce in nonlinear loads with the help of SHEPWM techniques; here the SHEPWM should be used to control the common mode voltage in closed loop. And it will be generate a pulse signal to flying capacitor multi level inverter here the THD should be calculated by LCL filtering method. For before filtering level the harmonics are generated and before filtering condition the THD should be reduced with the help of SHEPWM. Here loads are connected in series to non linear loads.

During proposed model using flying capacitor type clamped inverter .in this project the harmonics should be reduced by using less number of switches. This proposed inverter consists of less number of switches when compared to the other familiar topologies and initial cost also reduces due to the switch reduction. The flying-capacitor inverter does not require all the switches that are on (conducting) be in a consecutive series. Moreover, the flying-capacitor inverter has phase redundancies; whereas the diode-clamped inverter has only line-line redundancies. These redundancies allow a choice of charging/discharging specific capacitors and can be incorporated in the control system for balancing the voltages across the various levels.

A multilevel inverter not only achieves high power ratings, but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind, and fuel cells can be easily interfaced to a multilevel inverter system for a high power application. under this condition neutral point clamped multilevel inverter is presented in existing model, which has a simple structure and good performance .This topology effectively reduce the higher input dc voltage that each device must withstand. The main disadvantage still exists in this topology, which restricts the use of it to the high power range of operation. So the flying capacitor type clamped inverter should present in proposed model and also reduces harmonics in less number of switching devices.

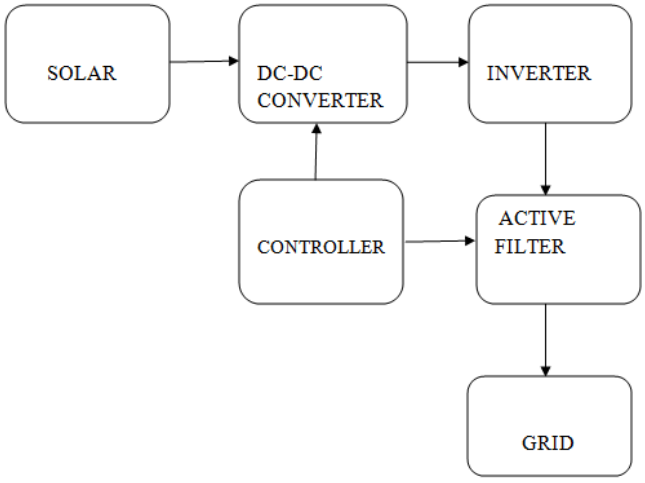

Fig 3. Bock Diagram Of Proposed Model

III.A) Dc Source

Here the DC power generated from photovoltaic cell. It will be produce a direct DC supply into boost converter, the individual dc source given into all converters. The purpose boost converter it's used to step up the DC voltage.

III.B) Boost Converter

The buck–boost converter is a type of DC-to-DC converter that has an output voltage magnitude that is either greater than or less than the input voltage magnitude. Two different topologies are called buck–boost converter. Both of them can produce a range of output voltages, from an output voltage much larger (in absolute magnitude) than the input voltage, down to almost zero.

III.C) Cascaded Multilevel Inverter

The single phase inverters find wide applications in low power applications. It is not an economical solution to use multilevel inverters for low power applications where square wave or quasi square wave inverters are preferred. To understand the operating principle of cascaded multilevel inverter different levels of single phase inverter is presented. There are three level of flying capacitor type clamped inverter connected series to non linear loads. It's taken an output pulse from SHEPWM and also reduces the THD with the help of LCL filtering method. The LCL filter should be used to reduce the THD in after filtering condition.

The three, five and seven levels of cascaded multi level inverters are modeled and simulated using MATLAB/SIMULINK model for different carrier frequencies and the corresponding values of total harmonic distortion were obtained and analyzed for magnitude and linearity. The carrier frequency with 5 kHz yields better results in terms of the output THD and it is fixed for all the levels. From the values of percentage total harmonic distortion it can be concluded that as the number of levels of the inverter increases the percentage of the output THD value decreases.

III. D) Pulse Width Modulation (PWM)

PWM technique is extensively used for eliminating harmful low-order harmonics in inverters. In PWM control, the inverter switches are turned ON and OFF several times during a half cycle and output voltage is controlled by varying the pulse width. Pulse-width modulation (PWM), as it applies to motor control, is a way of delivering energy through a succession of pulses rather than a continuously varying (analog) signal. By increasing or decreasing pulse width, the controller regulates energy flow to the motor shaft. The motor's own inductance acts like a filter, storing energy during the "on" cycle while releasing it at a rate corresponding to the input or reference signal. In other words, energy flows into the load not so much the switching frequency, but at the reference frequency. PWM is somewhat like pushing a

playground-style merry-go-round. The energy of each push is stored in the inertia of the heavy platform, which accelerates gradually with harder, more frequent, or longer-lasting pushes.

The riders receive the kinetic energy in a very different manner than how it's applied. PWM can be used to control the amount of power delivered to a load without incurring the losses that would result from linear power delivery by resistive means. Potential drawbacks to this technique are the pulsations defined by the duty cycle, switching frequency and properties of the load. With a sufficiently high switching frequency and, when necessary, using additional passive electronic, the pulse train can be smoothed and average analog waveform recovered. High frequency PWM power control systems are easily realizable with semiconductor switches. As explained above, almost no power is dissipated by the switch in either on or off state. However, during the transitions between on and off states, both voltage and current are nonzero and thus power is dissipated in the switches. By quickly changing the state between fully on and fully off (typically less than 100 nanoseconds), the power dissipation in the switches can be quite low compared to the power being delivered to the load.

In this paper using a Selective Harmonic PWM (SHEPWM) technique which will using closed loop module. There are many popular methods are used to reduce the harmonics in order to get an effective results. The popular methods for high switching frequency are Sinusoidal PWM and Space Vector PWM. For low switching frequency methods are space vector modulation and selective harmonic elimination. The SPWM technique has disadvantage that it cannot completely eliminate the low order harmonics. Due to this it cause loss and high filter requirement is needed. In Space Vector Modulation technique cannot be applied for unbalanced DC voltages. SHE PWM technique uses many mathematical methods to eliminate specific harmonics such as 5th, 7th, 11th, and 13th harmonics. The popular Selective Harmonic Elimination method is also called fundamental switching frequency based on harmonic elimination Theory.

Three types of pulse-width modulation (PWM) are possible:

1. The pulse centre may be fixed in the centre of the time window and both edges of the pulse moved to compress or expand the width.
2. The lead edge can be held at the lead edge of the window and the tail edge modulated.
3. The tail edge can be fixed and the lead edge modulated.

III.E) Non-Linear Load

A load is considered non-linear if its impedance changes with the applied voltage. The changing impedance means that the current drawn by the non-linear load will not be sinusoidal even when it is connected to a sinusoidal voltage. These loads are common in fluorescent lamps and electric welding machines. Large industries and electrical utilities are very concerned about the presence of nonlinear loads in their electrical power systems. It describes the causes of harmonics and their effects, as well as the means to improve power quality and to protect the equipment.

III.F) PI Controller

A proportional-integral-derivative controller (PID controller) is a generic control loop feedback mechanism (controller) widely used in industrial control systems. A PID controller calculates an "error" value as the difference between a measured process variable and a desired set point. The controller attempts to minimize the error by adjusting the process control outputs.

The PID controller algorithm involves three separate constant parameters, and is accordingly sometimes called three-term control: the proportional, the integral and derivative values, denoted *P*, *I*, and *D*. Simply put, these values can be interpreted in terms of time: *P* depends on the *present* error, *I* on the accumulation of *past* errors, and *D* is a prediction of *future* errors, based on current rate of change.

IV.SELECTIVE HARMONIC ELIMINATION (SHE) PWM

Selective Harmonic Elimination (SHE) has been a research topic since the early 1960's, first examined in and developed into a mature form in during the 1970's is a long established method of generating pulse width modulation (PWM) with low baseband distortion. Originally, it was useful mainly for inverters with naturally low switching frequency due to high power level or slow switching devices. The selective harmonic elimination method is also called fundamental switching frequency method based on the harmonic elimination theory.

There are many popular methods are used to reduce the harmonics in order to get an effective results. The popular methods for high switching frequency are Sinusoidal PWM and Space Vector PWM. For low switching frequency methods are space vector modulation and selective harmonic elimination. The SPWM technique has disadvantage that it cannot completely eliminate the low order harmonics. Due to this it cause loss and high filter requirement is needed. In Space Vector Modulation technique cannot be applied for unbalanced DC voltages. SHE PWM technique uses many mathematical methods to eliminate specific harmonics such as 5th, 7th, 11th, and 13th harmonics. The popular Selective Harmonic Elimination method is also called fundamental switching frequency based on harmonic elimination Theory.

IV.A) HARMONIC ELIMINATION THEORY

By applying Fourier series analysis, the output voltage can be obtained. Fourier series is an infinite sum of trigonometric functions that are economically related

$$f(t) = a_0 + \sum_{n=1}^{\infty} c_n \cos(2\pi n f_0 + \varphi_n) \quad (1)$$

Where

n= integer multiple,

φ_n = initial phase for nth harmonic

a_0 and c_n = Fourier co-efficients

The output voltage equation derived for different voltage sources is given below.

$$v(t) = \sum_{n=1,3,5}^{\infty} \frac{4V_{dc}}{n\pi}((v_1 \cos(n\varphi_1) + v_2 \cos(n\varphi_1) \dots v_s \cos(n\varphi_2))\sin(n\omega t)$$

(2)

Where

S = No. of dc sources connected per phase

V1, V2, V3 = level of Dc voltage $0 < \theta_1 < \theta_2 < \theta_3 \dots \dots < \theta_s < \frac{\pi}{2}$ = Switching angles

For the above Fundamental peak voltage v(t), it is required to determine the switching angles and some lower order harmonics of phase voltage are zero. Among no of switching angles one is used for fundamental voltage selection and remaining (s-1) switching angles are needed to eliminate lower order harmonics. For a balanced three phase system, triplen harmonics are eliminated automatically by using line-line voltages so only non-triplen odd harmonics are present. To minimize harmonic distortion and to achieve adjustable amplitude of the fundamental component, up to *s*-1 harmonic contents can be removed from the voltage waveform. To keep the number of eliminated harmonics at a constant level, all switching angles must satisfy the condition otherwise the total harmonic distortion (THD) increases dramatically.

This paper proposes a hybrid selective harmonic elimination pulse width modulation (SHEPWM) scheme for common mode voltage reduction in three-level neutral-point-clamped inverter-based induction motor drives. The scheme uses the conventional SHEPWM (C-SHEPWM) to control the inverter at high frequency ($\geq$ 0.9 motor rated frequency) and uses the modified SHEPWM (M-SHEPWM) to control the inverter at low frequency.

IV.B) Features of C-Shepwm and M-Shepwm

In an SHEPWM method the both CSHEPWM and MSHEPWM methods are used to control the Common Mode Voltage(CMV).Commonly used SHEPWM scheme, termed as C-SHEPWM reduces (6k±1)th (5th, 7th, 11th, 13th, . . .)harmonics, while keeping triplen harmonics in each inverter leg output voltage. This SHEPWM scheme takes advantage of the fact that the triplen harmonics, though existing in the inverter leg output voltage, will be cancelled in the line-to-line voltage of the motor. Another SHEPWM, termed as Modified SHEPWM or M-SHEPWM reduces (4k±1) th (3rd, 5th, 7th, 9th,.) harmonics. Since this SHEPWM scheme eliminates low-order triplen harmonics from each inverter leg output voltage, it reduces theTHD of the inverter.

Table 1.Features of C-SHEPWM&M-SHEPWM

	C-SHEPWM	M-SHEPWM
Harmonics eliminated	$6k\pm1$	$4k\pm1$
Maximum modulation index	1.15	1
Highest harmonic order eliminated	$3N$ - 2	$2N$ - 1

V. ACTIVE POWER FILTER

The increased severity of harmonic pollution in power networks has attracted the attention of power electronics and power system engineers to develop dynamic and adjustable solutions to the power quality problems. Such equipments, generally known as active filters [15], are also called active power line conditioners. To effectively compensate the line current harmonics, the active filter controller should be designed to meet the following three goals:

1. Extract harmonic currents and inject compensating Current
2. Maintain a constant dc capacitor voltage
3. Avoid generating or absorbing reactive power with Fundamental frequency components.

VI. NEURO-FUZZY CONTROLLER

Neuro fuzzy system gives the switching angles and frequency value. By using this value the harmonic contents present in the system are eliminated. The overall process takes place in proposed method is shown in Fig.4. Feedback controller used here is to calculate voltage error values in the system. This voltage error values is given as the input to neuro fuzzy system. In the feedback controller, the voltage values are calculated from the voltage waveform for different time values. From the reference waveform voltage values at different time values are taken as reference voltage value. Then for different time values, the voltage values are taken from the harmonics waveform and compared with the reference waveform.

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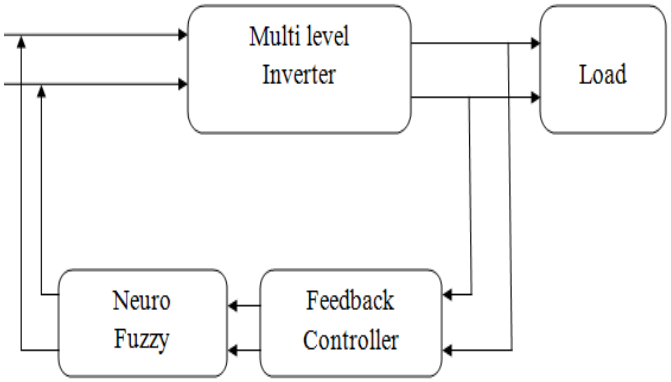

Fig 4.Block diagram of Neuro Fuzzy Controller

VII. NON-LINEAR LOAD

A nonlinear load in a power system is characterized by the introduction of a switching action and consequently current interruptions. This behaviour provides current with different components that are multiples of the fundamental frequency of the system. These components are called harmonics. For a fundamental power frequency of 60 Hz, the 2nd harmonic is 120 Hz; the 3rdharmonic is 180 Hz, and so on. The harmonic currents flow toward the power source through the path of least impedance.

Some examples of nonlinear loads that can generate harmonic currents are computers, fax machines, printers, PLCs, refrigerators, TVs and electronic lighting ballasts. Differently from the reactive power drawn by a linear load, the harmonic currents cannot be corrected by the use of capacitors and inductors, but by the use of Harmonic Mitigating Transformers.

Filters can be used when equipments are connected in a non-sinusoidal system. Nonlinear loads can be modelled, and these models can be used to evaluate the voltage and current harmonics in the loads.

VII.A) Difference between Linear& Non-Linear Loads

Table 2

LINEAR LOAD	NON LINEAR LOAD
Load current does not contain harmonics.	Load current contains all ODD harmonics.
Could be inductive or capacitive.	Can't be categorized. As leading or lagging Loads.
Resistive, Inductive or capacitive.	Usually an equipment with Diode and Capacitor.
May not demand high inrush currents while starting.	Essentially very high inrush current (20 time of I Normal)is drawn while starting for approx. One cycle.

VIII. SIMULATION RESULT ANALYSIS

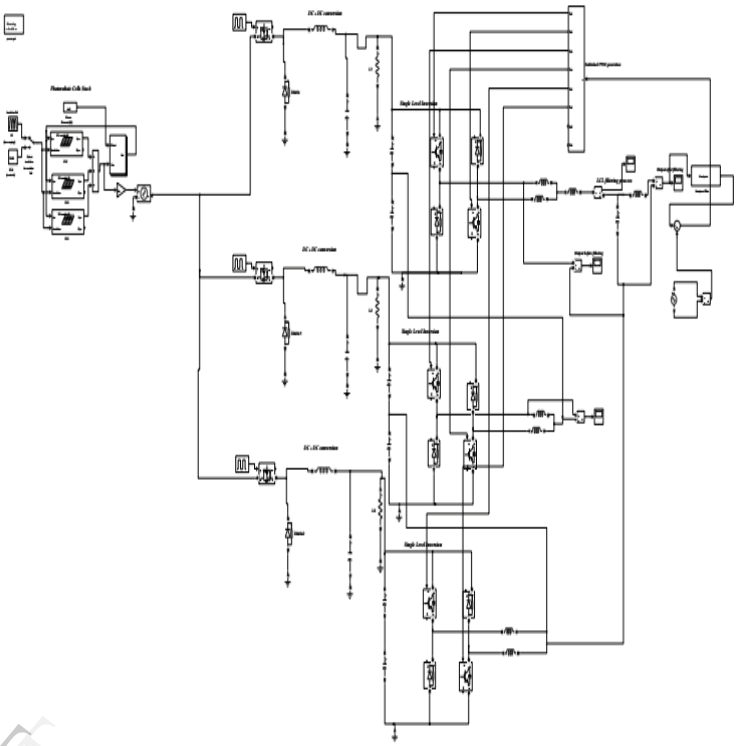

Fig 5.Simulation Diagram

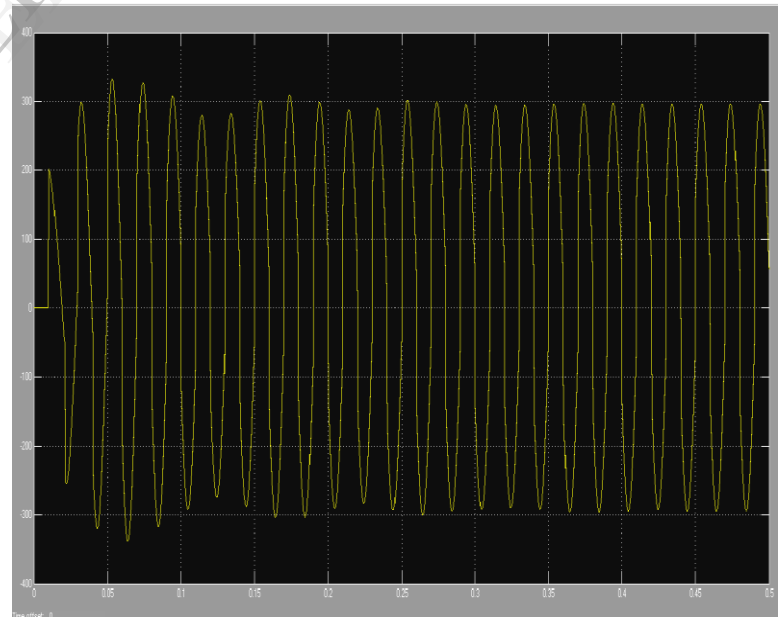

Fig 6. Shows the MATLAB simulation output voltage wave form of seven level cascaded multilevel inverter before filtering condition

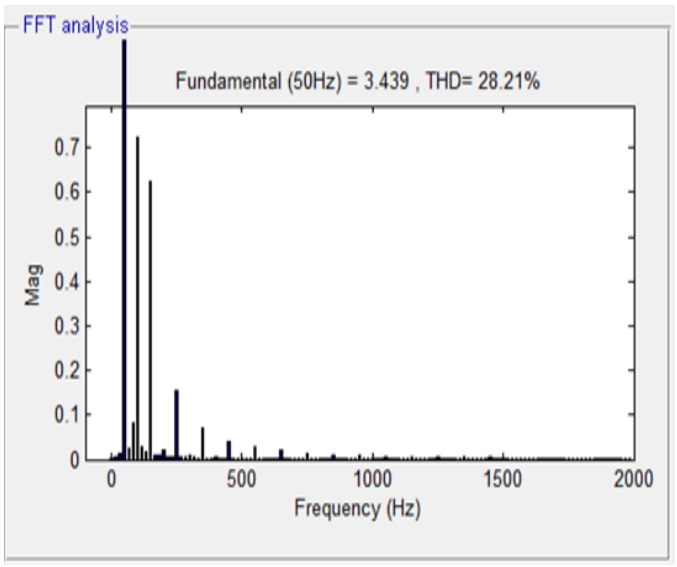

Fig 7. THD value of seven level inverter at before filtering is 19.75%.

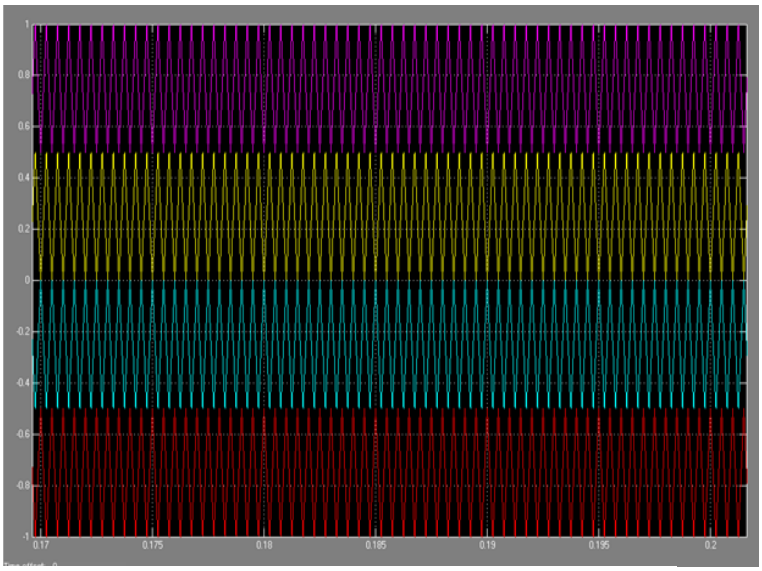

Fig 9.PWM Input Wave form

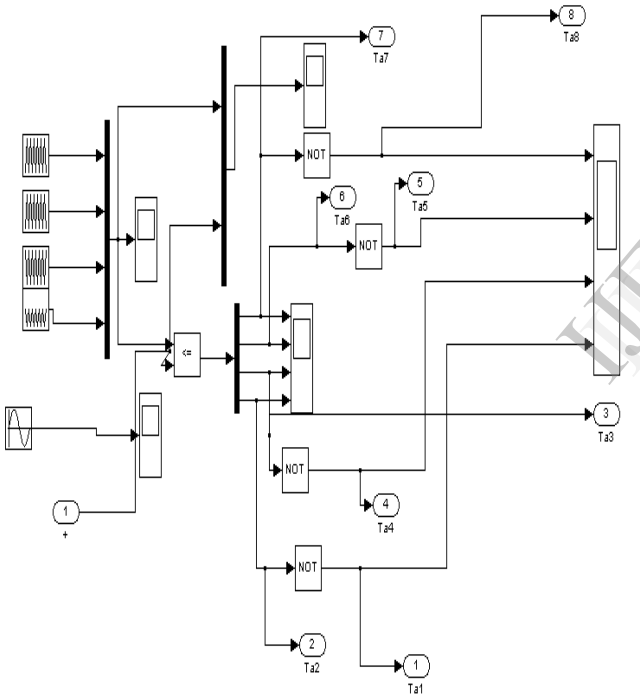

Fig 8.PWM Model

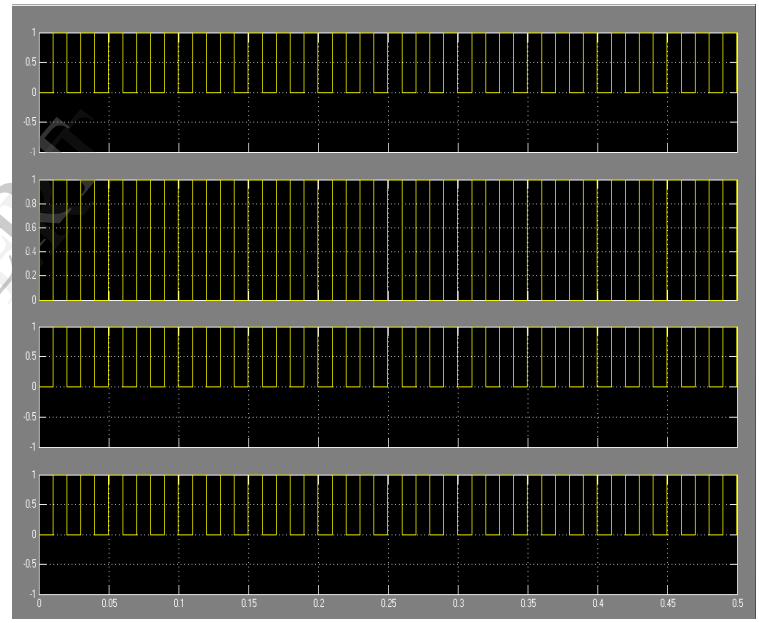

Fig 10.PWM Output Signal Waveform

Carrier frequency=20KHz Starting time=0.05sec

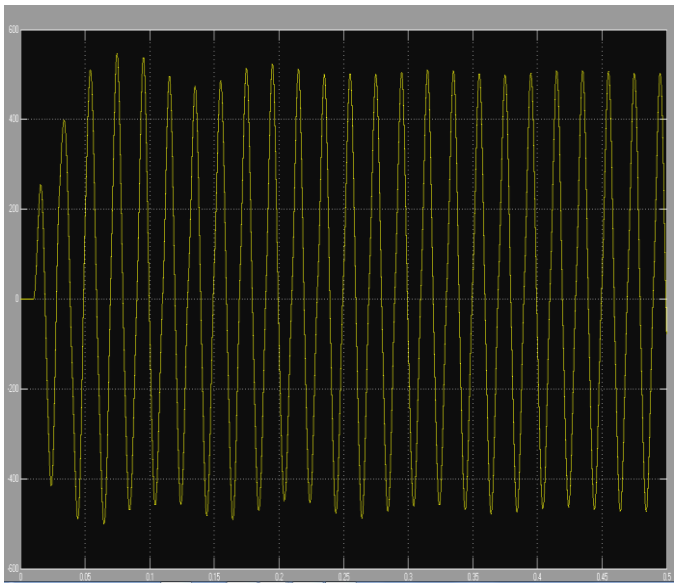

Fig 11. Shows the MATLAB simulation output voltage wave form of seven level cascaded multilevel inverter after filtering condition.

Fundamental frequency=50Hz
Number cycles=3
Starting time=0.3sec
THD rating=12.14%

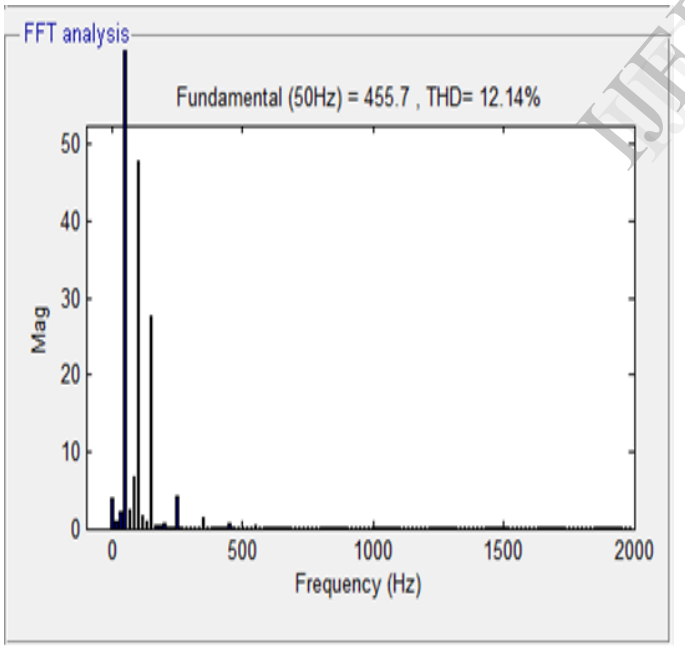

Fig 12. THD value of seven level inverter at after filtering is 12.14%.

IX. CONCLUSION

The simulation of the Three-level flying capacitor type clamped inverter is successfully done by using Selective Harmonic Elimination pulse width modulation technique. This proposed inverter consists of less number of switches when compared to the other familiar topologies. The initial cost reduces because of the switch reduction. From the simulation results THD value is calculated and compared the THD value of multilevel inverter with before and after filtering levels. Thus THD value is reduced using SHEPWM Technique. In this project the closed loop PWM techniques are used to reduce THD. Initially going to find a harmonics generation and it will be reduced by using LCL filtering condition.

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