Signal Processing and Display of LFMCW Radar on a Chip

Fathy M. Ahmed
Military Technical College, Cairo, Egypt

Abstract

The tremendous progress in embedded systems helped in the design and implementation of complex compact equipment. This progress may help in the idea of having radar on a chip. In this paper, a design and implementation of a signal processor and display algorithm for Linear Frequency Modulated Continuous Wave (LFMCW) radar on single Field Programmable Gate Array (FPGA) chip is proposed. The proposed algorithm is used for processing signals from radar receiver into information that can be interpreted easily. The signal processor based on calculating the Fast Fourier Transform (FFT) of the filtered, amplified, and digitally converted base band received signal to calculate target range. The B-scope radar display is designed to give target range and azimuth information. A simple Video graphic Adaptor (VGA) is designed to connect FPGA directly to a commercial Liquid Crystal Display (LCD). The proposed algorithm is cheap, simple, compact, and reliable. It can be considered as a first step to have complete radar on a chip.

Keywords: FPGA, LFMCW radar, and VGA.

1. Introduction

LFMCW radars are widely used to get the information of small size targets with high resolution which can be achieved by using wide-spectrum and narrow beam width [1-4]. This kind of radar, as shown in Figure 1, works by continuously transmitting linear frequency sweeps and mixing the delayed echoes from targets with a sample of the transmitted signal.

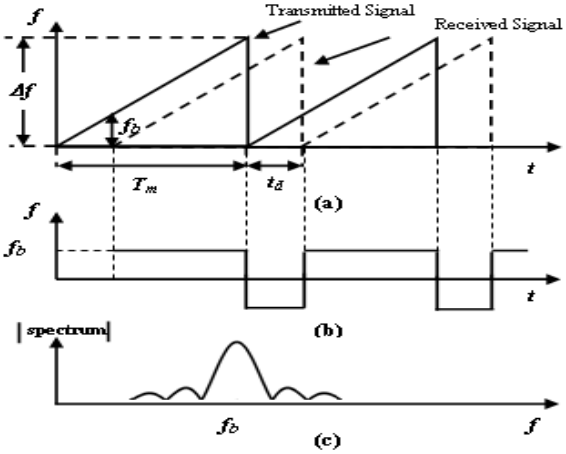


Figure 1 LFMCW radar signals ;(a) transmitted and received signals,(b) beat frequency, and (c) spectrum of mixed signal

Target range information is extracted from the spectrum of this mixed signal which is calculated by FFT algorithm [5]. This information is sent to the display part to be visualized on screens. One of the common radar displays used to monitor range azimuth information is the B-scope [1, 2]. Azimuth is represented as the horizontal axis, while range is represented in the vertical axis.

As technology is going up day after day, equipments are getting compact more and more. Based on this fact, the idea of having radar on a chip comes true. FPGA is one of the new developed digital hardware programmable components. By using these components, most of the digital logic circuits can be implemented in one or more chips. FPGA technology has the advantage of reducing size, cost, complexity, and leading to high reliability, maintainability and flexibility. These devices are programmed with special tools which indeed provide a kind of software generation. When this software is compiled and loaded into the device, it will be ready to implement the circuit of the specified application [6]. In the present paper, a design and implementation of a signal processor and display algorithm for LFMCW radar on single FPGA chip is proposed.

The rest of this paper is organized as follows; after the introduction, LFMCW radar theory is introduced in section 2. A description of the overall system design is presented in section 3. Finally, conclusion comes in section 4.

2. LFMCW Radar Theory

The general block diagram of LFMCW radar is shown in Figure 2 [1, 2]. The designed modules in the present work are shadowed in this figure.

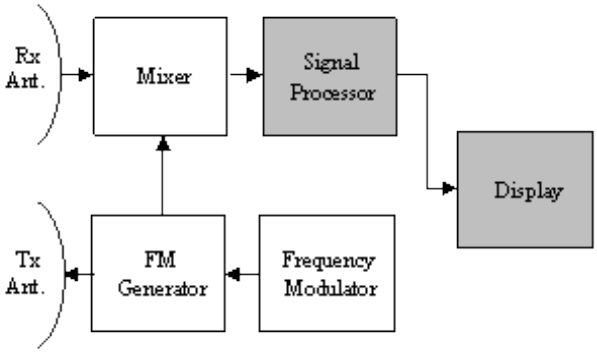


Figure 2 Block diagram of LFMCW radar

The range information of a fixed target can be obtained by [1, 2]:

$$R = \frac{f_b * T_m * C}{2 * \Delta f} \quad (1)$$

Where, f_b is the beat frequency, T_m is the modulation interval, C is the speed of light, and Δf is the difference between the maximum and minimum of the transmitted frequency.

The basic signal processing of LFMCW radar is to get the beat frequency. The target movement would cause the delay of the echo signal not to be constant, but if the delay change is slow enough, only the phase of the video signal would be changed (Doppler Frequency). So, the range and Doppler information can be extracted by the range-Doppler processing of the received signal. In the present work, for simplicity, only range information is considered. The common method of range processing is the FFT. Then this information is sent to the display part to be visualized on screens. The B-scope is a common radar display. Horizontal axis in this display represents the azimuth, while the vertical one represents the range. In the present work, a simple B-scope is designed to be screened on a commercial LCD. In the next section the overall description of the proposed design is presented.

3. Overall System Design

The proposed design for the signal processing and display of LFMCW radar, shown in Figure 3, consists of three sections; data acquisition, signal processing, and displaying.

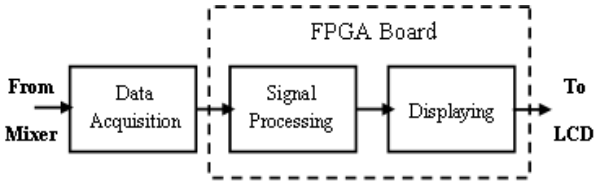


Figure 3 The proposed overall system design

Each of these sub-blocks is described in the following subsections. Design parameters of the used LFMCW radar is listed in Table 1.

Table 1 Design parameters of the used LFMCW radar

Parameter	Value
Modulation type	*Sawtooth*
Operating frequency	*2.4 GHz*
Scan type	*Sector (120^0)*
Max. range	*1200 m*
Max. beat frequency, f_{bmax}	*20 KHz*
Sampling frequency, f_s	*50 KHz*
FFT points	*128 samples*
Range resolution	*18.75 m*
Angle resolution	*2^0 degree*

3.1 Data Acquisition

Echoes reflected from objects, either the targets or the clutter, are received via a receiving antenna. The received carrier frequency waveform is converted into a base-band frequency waveform after the mixing process. Mixer is a nonlinear component, and its output consists of different harmonics. Only, the useful signal is the difference between its two inputs. So, a low pass filter with cut off frequency equals to the maximum beat frequency of 20 KHz is required. Also, this signal is very weak and requires some amplification. The next step is to convert this signal into digital form for processing inside FPGA. A sampling frequency of 50 KHz which satisfies Shannon theory is chosen [7]. A flash 6 bits Analog to Digital Converter (ADC) chip, CA3300, is used for conversion. The reference voltages of this ADC are 0 to 5 volts, so, an offset circuit is needed to shift the mixer output after filtering and amplification to be changed within 0 to 5 volt instead of -2.5 to 2.5 volt. However, the block diagram of the designed data acquisition circuit is shown in Figure 4. Simulation results to verify this circuit in time and frequency domains using OR-CAD are shown in Figure 5.

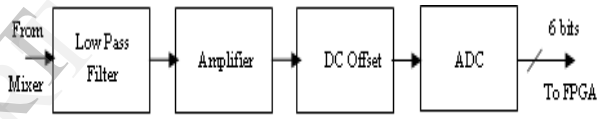
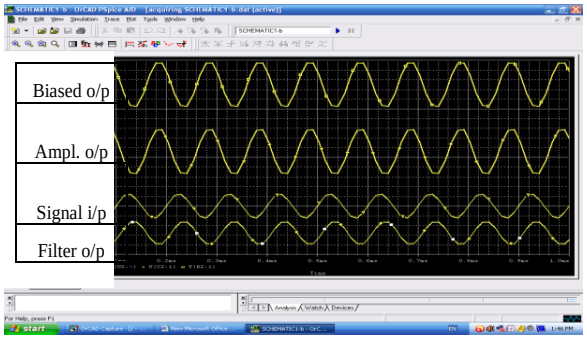
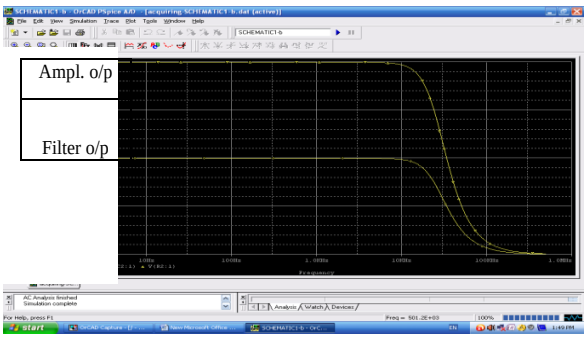


Figure 4 Block diagram of the data acquisition circuit



(a)



(b)

Figure 5 ORCAD simulation results of the data acquisition circuit; (a) time domain, and (b) frequency domain

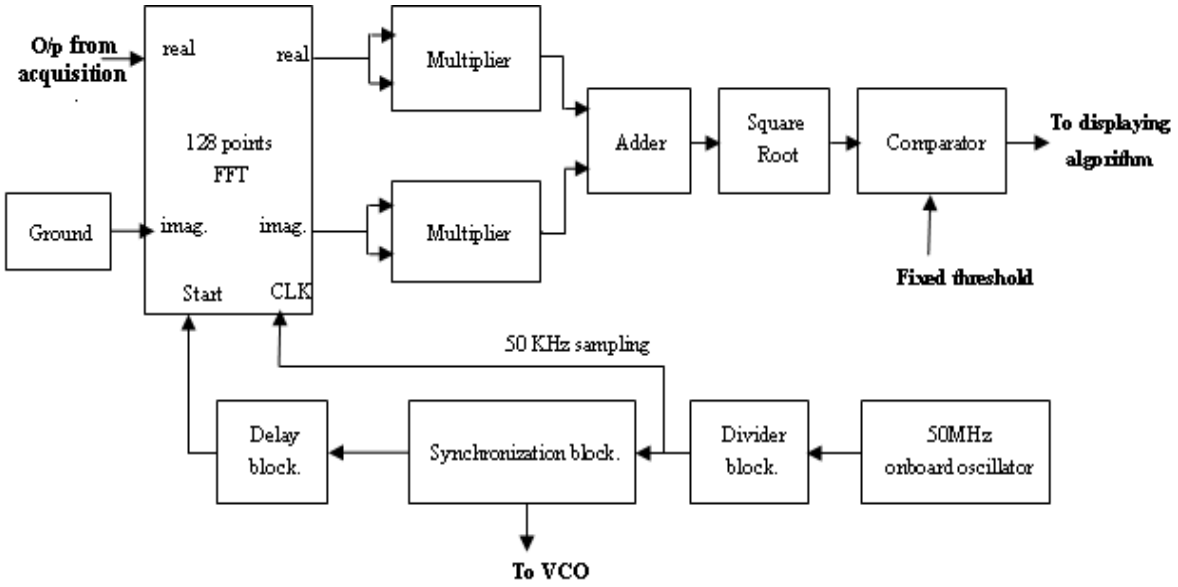


Figure 6 Block diagram of the designed signal processing circuit inside FPGA

3.2 Signal Processing

The output digital signal from the designed data acquisition circuit is fed to the used Spartan 3 FPGA starter kit (XC3S200FT256 chip) [8] for signal processing and displaying algorithm. The block diagram of the designed signal processing algorithm is shown in Figure 6. This block diagram is designed based on Xilinx ISE package.

Signal processing to get range information in LFMCW radar is simply an FFT operation of the received base-band signal. Since the received base-band signal is real, its spectrum is symmetric around $f_s/2$. So, the corresponding useful range pins out of the implemented 128 FFT pins is 64 which corresponds to the total designed range of 1200 m. So, the range resolution is 18.75 m. To achieve a sampling rate, f_s, of 50 KHz, a divider circuit is designed to get this sampling rate from the 50 MHz oscillator on the FPGA board.

A synchronization circuit is designed to trigger the Voltage Controlled Oscillator (VCO) control circuit for sawtooth sweeping. The start of signal processing is achieved by a designed triggering signal delayed from the synchronization signal by the maximum expected target delay of 8 us which corresponds to the maximum designed range of 1200 m. For safety, this delay is chosen to be one sampling period (20 us). Figure 7 shows the relation between these control signals.

The magnitude output of the FFT block is then compared with a fixed appropriate threshold value entered manually through digital switches on the FPGA board to decide the presence or absence of a target. The output decision is then fed to the displaying algorithm which is responsible of presenting range and azimuth information on the designed B-scope.

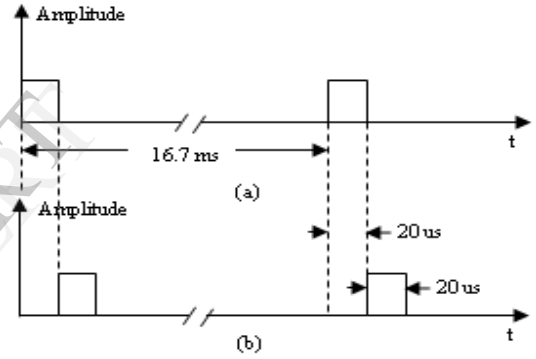


Figure 7 LFMCW radar control signals, (a) sawtooth triggering, and (b) signal processing start

3.3 Displaying Algorithm

The Spartan 3 starter kit board includes a VGA display port and DB15 connector. This port can be directly connected to most personal computer monitors or flat panel LCD displays using a standard monitor cable. The proposed displaying algorithm controls 5 VGA signals on the DB15 connector; Red (R), Green (G), Blue (B), Horizontal Sync (HS), and Vertical Sync (VS). These signals are responsible of operating and displaying the B-scope on the LCD monitor. A VGA standard resolution of 640x480 is chosen to be designed. Standard HS and VS signals parameters can be easily found [9], and a corresponding Very high speed integrated circuit Hardware Description Language (VHDL) code is written in the present work to get them. A general block diagram of the proposed displaying algorithm is shown in Figure 8.

The clock rates of each processing algorithm (sampling rate of 50 KHz) and the proposed displaying algorithm (pixel clock rate of 25 MHz) are different. So,

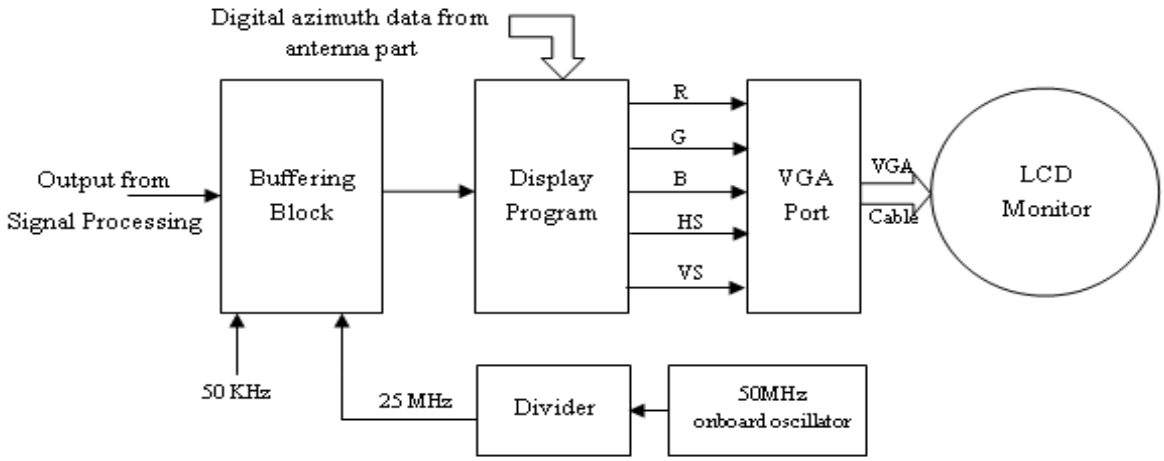


Figure 8 General block diagram of the designed displaying algorithm inside FPGA

a buffering algorithm, shown in Figure 9, between the signal processing part output and the displaying part input is designed. This buffering algorithm is responsible of storing the signal processing part output during one VCO sweep in range order controlled by an address generated from the FFT block with a rate of 50 KHz. During this sweep, the previously stored range data from the previous sweep is written to the displaying program with 25 MHz rate and controlled by a generated address for the pixel locations on the LCD display.

The azimuth data information is fed digitally to the proposed displaying algorithm from the antenna control circuits through the onboard FPGA connector. This azimuth data is in the form of 9 bits counting up and down corresponding to the direction of the scanned antenna sector. This data is used to plot the running time base of the B-scope.

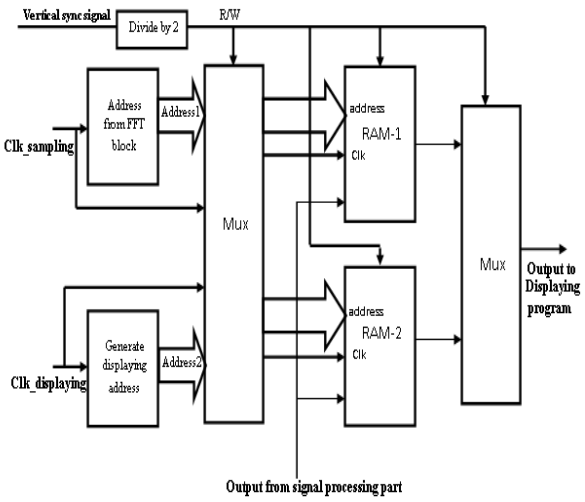


Figure 9 Block diagram for the buffering circuit between signal processor and display algorithms

For the purpose of clarity, the designed B-scope is divided into horizontal and vertical grids. Vertical grids represent the range resolution and only 32 range pins are plotted which is equivalent to 600 m. Horizontal grids represent the azimuth resolution. Also, 32 azimuth grids are plotted. By doing this, a detected target can be represented as a green square representing its range and azimuth on the designed B-Scope.

To add some demonstration on the designed B-scope, some writing representing the title, azimuth direction, range direction, a logo, and a range grid values are designed and presented. The way of designing these writing is achieved through generating an image of each phrase or logo. Then, this image is transformed using MATLAB into binary file. This file is stored in separate block memory inside the FPGA. Each block memory is addressed and enabled at certain instant and using certain address as required. However, the designed signal processing and displaying unit connected to a commercial LCD display is shown in Figure 10. The total implemented hardware occupied 84% of the total resources of the used FPGA chip. The maximum processing speed was found to be 81 MHz.

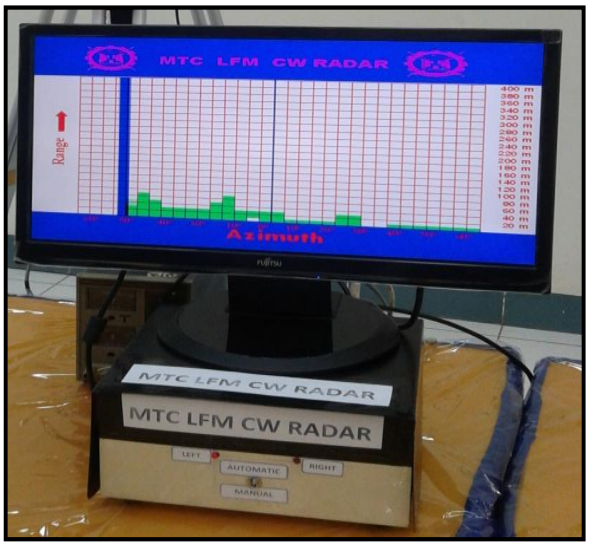


Figure 10 The designed signal processing and displaying unit connected to a commercial LCD display showing a radar B-scope

4. Conclusion

In this paper, a signal processing and displaying algorithm of simple sawtooth LFMCW radar, both implemented on a single Xilinx Spartan 3 FPGA chip (XC3S200FT256), has been proposed. Base-band received radar signal was filtered, amplified, and converted to digital form suitable for processing with FPGA. The proposed design and implementation relied completely on embedded system. This fact gives the system advantages of reliability, flexibility, compactness, and real time operation. Radar target range and azimuth were easily presented on a designed B-scope displayed on a commercial LCD. The proposed design consumed 84% of the used FPGA chip resources and achieved a maximum processing speed of 81 MHz for the obtained range resolution of 18.75 m. The proposed design is considered as a first step in building radar on a chip. More signal processing and enhanced target range resolution can be achieved by using large density FPGAs.

5. References

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