Simulation Analysis of a Novel Five-Level Diode Clamp Multilevel Inverter Topology for Industrial Application

Ms. Kavita Shrivastava
[1]PG Student S.D. College of Engineering, Selukate, Dist Wardha, India.

Mr. R.G. Shriwastava[2]
[2]Associate Professor & Head of Department of Electrical Engineering, B.D. College of Engineering, Sevagram, Dist Wardha, India

Mr. K. N. Sawalakhe[3]
[3]Head of Department (Electronics & Telecommunication)
S.D. College of Engineering, Selukate, Dist. Wardha, India.

***Abstract* --This paper presents a new five level diode clamped multilevel inverter topology which can be used for low-medium power industrial applications. In this work proposes single phase five level Diode Clamped Multilevel Inverter (DCMLI) topology using an auxiliary switch is presented, the number of power devices required to implement a five-level output. The topology is tested in the design of a 5 levels diode clamp multilevel inverter simplified; circuit operation is presented, Simulated and validated with experimental tests performed on a laboratory prototype. In this paper, the concept of a 5-level diode-clamp and modulate principle are implemented to control the output waveform approaching to the sine-wave as close as possible. The simulation result, the output voltage waveform presents better harmonics profile.**

Keywords*: *Space Vector Pulse Width Modulation (SVPWM), 5-Level DCMLI, Total harmonic distortion (THD).

I. INTRODUCTION

Recently, single-phase induction motor is widely used in buildings and industries because of its compact size, endurance and cheap price. However, industrial sector requires improving its efficiency by employing various controls to improve the efficiency and to save energy. In this paper, the concept of a 5-level diode-clamp and modulate principle are implemented to control the output waveform approaching to the sine-wave as close as possible. Therefore, controlling approach of voltage and frequency supplied to stator coil in order to control the motor speed efficiently according to actual operations which was developed by [1-2] is employed. In recent years, industry has begun to demand higher power equipment, which now reaches the megawatt level. Controlled AC drives in the megawatt range are usually connected to the medium voltage network. Today, it is hard to connect a single power semiconductor switch directly to medium voltage grids. For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels. The inverters with voltage level 3 or more are referred as multi level inverters. Multilevel inverters have become attractive recently particularly because of the increased power ratings, improved harmonic performance and reduced EMI emission that can be achieved with the multiple DC levels that are available for synthesis of the output voltage. New diode clamping multilevel inverter. Developed DC link capacitor voltage balancing in a three phase diode clamped inverter controlled by a direct space vector of line to line voltages. Simulations are performed using MATLAB-SIMULINK. Harmonics analysis and evaluation of performance measures for various modulation indices have been carried out and presented.

The proposed inverter can actively regulate the reactive power on individual feeder lines at a programmable output while providing the variable output power . The diode-clamp inverter type is used for experimentations in this article. Such inverter employs the technique of proportional stepping harmonic elimination type to control switching equipment in the circuit for providing appropriated waveform and increasing the efficiency at high loading. The diode-clamp and modulate principle are implemented to control the output waveform approaching to the sine-wave as close as possible.

II. LITERATURE REVIEW

José Rodríguez, Jih-Sheng Lai, and Fang Zheng Peng et.al [1] Presents the Multilevel inverter technology has emerged recently as a very important alternative in the area of high-power medium-voltage energy control. This paper presents the most important topologies like diode-clamped inverter (neutral-point clamped), capacitor-clamped (flying capacitor), and cascaded multicell with separate dc sources. Emerging topologies like asymmetric hybrid cells and soft-switched multilevel inverters are also discussed. This paper also presents the most relevant control and modulation methods.R.Dharmaprakash, Joseph Henry et.al [2]. This paper proposes a switching table based 2-level inverter and 3-level diode clamped multilevel inverter (DCMLI) for the purpose of direct torque control of induction motor. The proposed scheme determines the sector of reference vector and the voltage vector is selected from switching table to generate gating signals for the inverter. The 2-level inverter and 3-level DCMLI are used to explain this scheme. This can be extended to n-level inverter and to all major topologies.Manish V. Kurwale, Er.N.C.Amzare, Palak G. Sharma et.al [3] This paper presents a five level diode clamped multilevel inverter topology which can be used for low medium power industrial applications. The topology of five levels diode clamp multilevel inverter is tested using MATLAB. Circuit operation is presented, simulated & Total

Harmonic Distortion is analysed. A pulse to the inverter is provided using discontinuous PWM technique. Xu Zheng, Li Song and Pan Hongying et.al[4] This paper introduces five-level neutral point clamped inverter topology structure, characteristic and working principle. The voltage shifted modulation technology in PWM IPD, POD and APOD three arrangements and principle are described in detail.S.Shalini et. al [5] presents a 9-level diode Clamped inverter using Sinusoidal pulse width Modulation techniques as the control strategies. The algorithm has been developed within the carrier-based PWM framework to facilitate its implementation in diode clamped converters with three or more levels. A simulation model of 9-level DCMI has been designed and developed.

III. PROPOSED METHODOLOGY

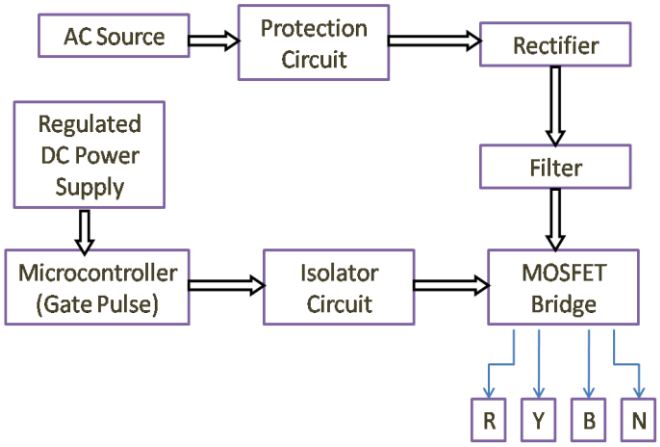

Fig.1 Block Diagram Of Proposed System

The general structure of the multilevel inverter is to synthesize a sinusoidal voltage from several levels of voltages typically obtained from capacitor voltage sources. Multilevel inverters are being considered for an increasing number of applications due to their high power capability associated with lower output harmonics and lower commutation losses. Multilevel inverters have become an effective and practical solution for increasing power and reducing harmonics of AC load.

The main multilevel topologies are classified into three categories:

- diode clamped inverters
- flying capacitor inverters
- cascaded inverters

In a three-phase inverter system, the number of main switches of each topology is equal. Comparing with the number of other components, for example, clamping diodes and dc-link capacitors having the same capacity per unit, diode clamped inverters have the least number of capacitors among the three types but require additional clamping diodes. Flying capacitor inverters need the most number of capacitors. But cascaded inverters are considered as having the simplest structure.

The diode-clamp inverter type is used for experimentations in this article. Such inverter employs the technique of proportional stepping harmonic elimination type to control switching equipment in the circuit for providing appropriated waveform and increasing the efficiency at high loading. The diode-clamp and modulate principle are implemented to control the output waveform approaching to the sine-wave as close as possible.

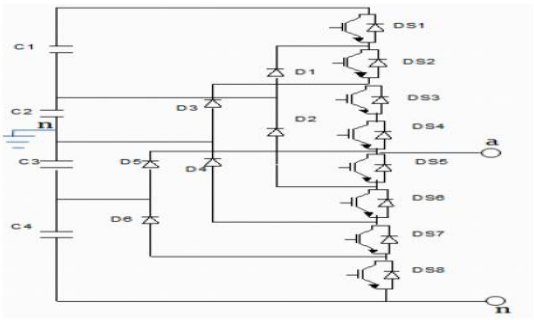

Fig.2 Diode Clamped Five Level Inverter

Number of DC bus capacitor in a multi level inverter is decided by (n-1), Number of switches in Multilevel inverter is decided by2*(n-1), Voltage source is decided by Vdc/ (n-1) & clamping diode is given by (n-1)*(n-2). Where 'n' is number of level of an inverter. For a five level inverter shown in "fig.1". In this circuit, the DC bus voltage is split up in to three levels as shown. Five-level diode-clamped converter in which the DC bus consist of four capacitor C1,C2,C3,C4 for DC bus voltage Vdc, the voltage across each capacitor is Vdc/4 & each device voltage stress will be limited to one capacitor voltage levels Vdc/4 through clamping diodes, For voltage levels Van= Vdc/2 turn on all upper switches S1-S4, For voltage level Van= Vdc/4, turn on three upper switches S2-S4 and lower switch S5,For voltage level Van=0, turn on two upper switches S3 and S4 and two lower switches S5 and S6, For voltage levels Van= -Vdc/4, turn on one upper switch S4 and three lower switches S5-S7, For voltage levels Van= -Vdc/2, turn on all lower switches S5-S8 NPC inverter which has been extensively used today in industrial drives, traction as well as FACT's system Based on concept of using diodes to limit power devices voltage stress Output phase voltage can assume any voltage level by selecting any of the nodes. DCMI is considered as a type of multiplexer that attaches the output to one of the available nodes Although main diodes have same voltage rating as main power devices, much lower current rating is allowable For three-phase DCMI, the capacitors need to filter only the high-order harmonics of the clamping diodes currents, low-order components intrinsically cancel each other Each power device block only a capacitor voltage Clamping diodes block reverse voltage

REDUCED SWITCHING TOPOLOGY

For practical implementation, the switching state needs to be converted into transistor signals. Once the transistor rsignals are established, general expressions for the a-phase line to ground voltage & the a-phase component of the DC currents can be written as

$V_{ao} = H_{an}V_{n0} + H_{an-1}V_{n-10} + \ldots + H_{a1}V_{10}$ (1)

$V_{bo} = H_{bn}V_{n0} + H_{bn-1}V_{n-10} + \ldots + H_{b1}V_{10}$ (2)

$V_{co} = H_{cn}V_{n0} + H_{cn}\text{-}1V_{n-10} + \ldots + H_{c1}V_{10}$ (3)

The Node Currents for the "n" level inverter are given by

$I_n = H_{an}I_a + H_{bn}I_b + H_{cn}I_c$

$I_{n-1} = (H_{an-1})I_a + (H_{bn-1})I_b + (H_{cn-1})I_c$

$I_1 = H_{a1}I_a + H_{b1}I_b + H_{c1}I_c$ (4)

The above relationships may be programmed into simulation software that simulates one phase of a diode clamped inverter. A number of blocks can be connected together for a multiphase system. For more simulation details, the transistor & diode KCL & KVL equations may be implemented. This allows inclusion of the device voltage drops & also the individual device voltages & currents. To express this relationship, consider the general N level diode clamped structure. Through the clamping action
of diodes, the blocking voltage of each transistor is the corresponding capacitor voltage in the series bank. Finally the capacitor junction currents may be expressed as the difference of two clamping diode currents. In case of a five level inverter, the expression reduces to

C1pVc1 = -Idc+Ha3Ia+Hb3Ib+Hc3Ic (5)

C1pVc2 = -(Idc+Ha1Ia+Hb1Ib+Hc1Ic) (6)

IV. SIMULATION MODEL AND RESULTS

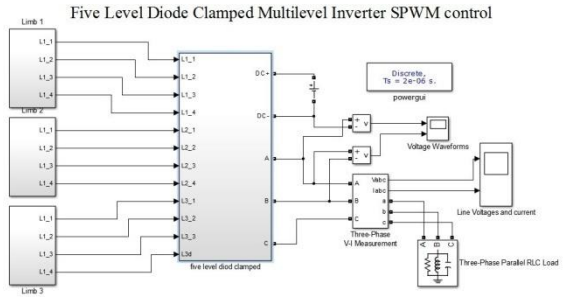

Fig.3 Simulink block diagram of Five Level Diode Clamped Inverter

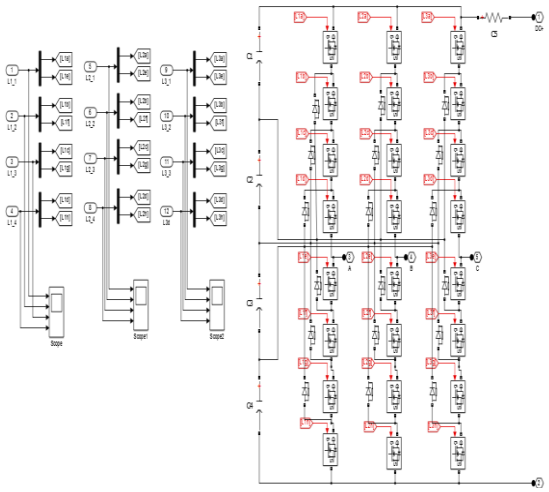

Fig.4 Sub system of Five Level Diode Clamped Inverter

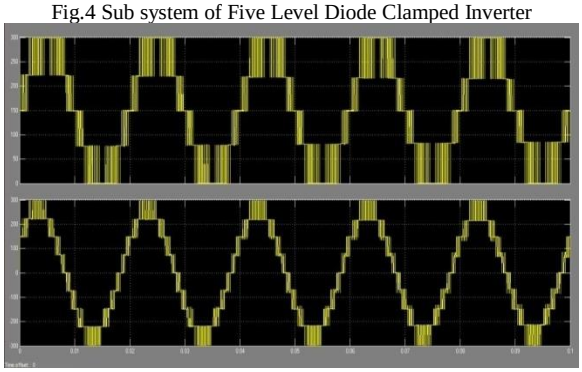

Fig.5 1- Phase to Neutral voltage

2-Line to Line voltage

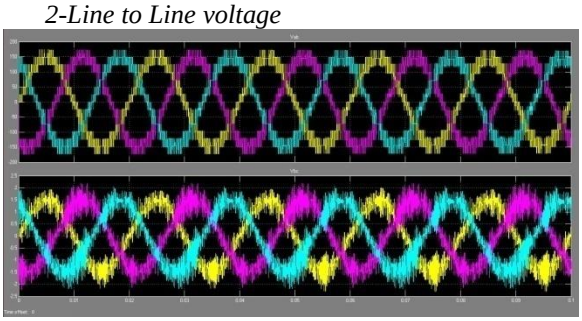

Fig.6 Three phase voltages

2-Three phase currents

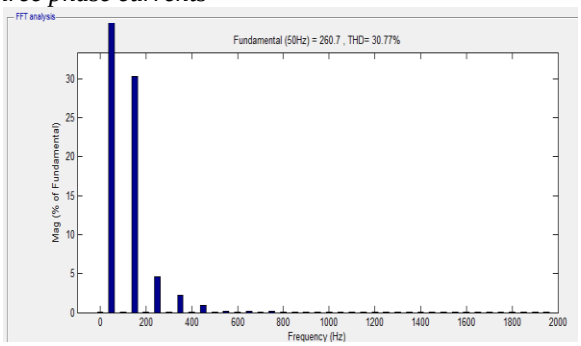

Fig. 7 THD magnitude (%)

V. RESULTS ANALYSIS AND DISCUSSION

DCMI is considered as a type of multiplexer that attaches the output to one of the available nodes Although main diodes have same voltage rating as main power devices, much lower current rating is allowable For three-phase DCMI, the capacitors need to filter only the high-order harmonics of the clamping diodes currents, low-order components intrinsically cancel each other Each power device block only a capacitor voltage Clamping diodes block reverse voltage.

VI. CONCLUSION

This paper had presented new topology for a diode clamped multilevel inverter. The main concept of this topology is to use power diode to limit power device voltage stress. The diode clamped multilevel inverter has an effective and practical solution for largest output levels and smallest Total Harmonic Distortion level. the simulation result the output voltage wavefom present better harmonic profile.

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AUTHORS BIOGRAPHY

Ms. Kavita Shrivastava obtained the B.E.Degree in Power Electronics Engineering from Nagpur University,India in 1997 & pursuing M.Tech. in Power Electroincs & power system from Suresh deshmukh college of Engineering,Wardha .

Mr. Rakesh Shriwastava obtained the B.E.Degree in Power Electronics Engineering from Nagpur University,India in 1994. He received the M.E.Degree in Control Engineering from Walchand college of Engineering,Sangli, (MS) India in 2007 & Pursuing the Ph.D.degree in Electrical Engineering from Nagpur University,Nagpur Since 2011 He is currently Working as Associate Professor & Head,in Electrical Engineering Department of Bapurao Deshmukh College of Engineering, Sewagram(Wardha).His research interests include analysis and control of electrical drives, particularly in hybrid and electric vehicle applications. He is a Life for Member of the Indian Society technical Education.

Mr. K.N.Sawalakhe obtained the B.E. Degree in Power Electronics Engineering from Nagpur University in 2004.& Masters Degree in Power System from PVG College of Engineering Pune in 2007.He is currently working as Head of Department in Suresh Deshmukh College of Engineering, Wardha. His area of interest for research is Power Electronics Drives.He is a Life member of the Indian Society technical Education.