Simulation and Analysis of Zero Voltage Switching PWM Full Bridge Converter

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Abstract— In the conventional zero voltage switching full bridge converter the introduction of a resonant inductance and clamping diodes are introduced the voltage oscillation across the rectifier diodes is eliminated and the load range for zero-voltage-switching (ZVS) achievement increases. When the clamping diode is conducting, the resonant inductance is shorted and its current keeps constant. So the clamping diode is hard turned-off, leading to reverse recovery loss if the output filter inductance is relatively larger. By introducing a reset winding in series with the resonant inductance to make the clamping diode current decay rapidly when it conducts this paper improves the full-bridge converter. The conduction losses are reduced by the use of reset winding. Also the clamping diodes naturally turn-off and avoids the reverse recovery. The proposed converter has been simulated for two different configurations and results have been compared. A 1 kW prototype converter is built to verify the operation principle and the experimental results are also demonstrated.

***Keywords*—**Clamping diodes, full bridge converter, reset winding, zero-voltage-switching (ZVS)**).**

1. Introduction

In medium-to-high power dc–dc conversions the full-bridge converter is widely used. It can achieve soft-switching without adding any auxiliary switches. The soft-switching techniques for PWM full bridge converter can be classified into two kinds: (i) zero-voltage-switching (ZVS) (ii) zero-voltage and zero-current-switching (ZVZCS) [1]. To achieve ZVS for switches the leakage inductance of the transformer and the intrinsic capacitors of the switches are used. The ZVS characteristics are load dependent and will be lost at light load [2]–[6]. In ZVZCS PWM full-bridge converters, one leg achieves ZVS, and the other leg achieves ZCS [7]–[13]. No matter ZVS or ZVZCS is realized for the switches there is serious voltage oscillation across the rectifier diodes caused by the reverse recovery By introducing a resonant inductance and two clamping diodes into the primary side of transformer this problem can be avoided [14]–[16]. The voltage ringing and overshoot, thus the voltage stress of the rectifier diodes is reduced without introducing losses or an additional controlled power device. The difference between the two locations of the resonant inductance and the transformer is analyzed and an optimal position is presented, [17].. No matter what the positions of the transformer and the resonant inductance are, the resonant inductance is clamped and its current keeps constant when the clamping diodes conduct. But the Transformer lead connection leads to more accurate results. The current ripple of output filter inductance should be sufficiently high to turn off the clamping diodes naturally. Because the forced turn off of clamping diodes results in serious reverse recovery., An auxiliary transformer winding has been introduced to the ZVS PWM full-bridge converter, in series with the resonant inductance. This winding makes the clamping diode current decay rapidly and reduces the primary side conduction losses. It also

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makes the current ripple of the output filter be smaller. Hence the output filter capacitor can be reduced. The experimental results are presented in Section IV to verify the validity of the proposed converter.

2. Operating Principle

The proposed ZVS PWM full-bridge converter with reset winding is shown in Fig. 1, where n_3 is the introduced reset winding. Phase-shifted control is used for the converter where $Q_1$and Q_3form the leading leg i.e the leg whose swiches operate first and Q_2 and Q_4 form the lagging leg. The converters in Fig. 1and (2) are defined as Tr_Lead type and Tr_Lag type, respectively. The primary winding n_1 is connected with the lagging leg and the leading leg, respectively. The operation principle of the two types is similar. The difference is that the clamping diodes conduct only once in type while conduct twice in type. The following description will be focused on the type.

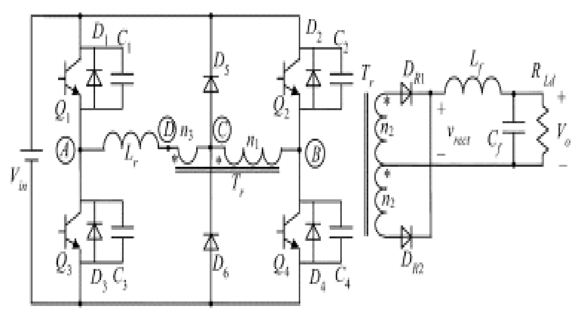


Fig: 1. Transformer-lag type ZVS PWM full bridge converter

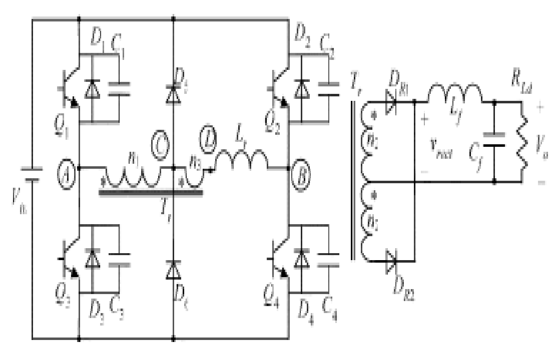
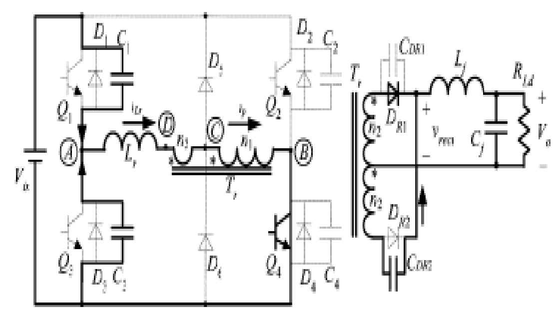


Fig: 2. Transformer-lead type ZVS PWM full bridge converter

Fig. 3 shows the equivalent circuits of the switching stages in a half period. The second half period is similar to the first half period.

1) *Stage 1* [Refer to Fig. (a)]

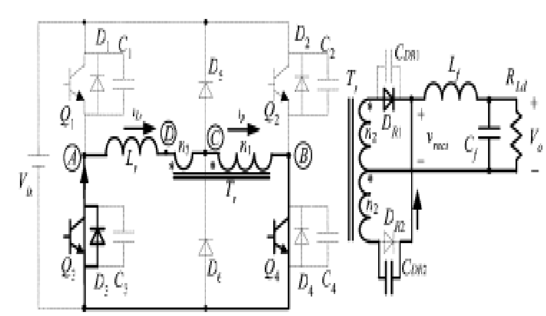
The power is transferred from the input source V_{in} to the load through Q_1, Q4 and DR_1. Q_1 is turned off at zero voltage due to C_1.C_3 limit the rising rate of the voltage across Q_1. The resonant inductance current i_{Lr} charges C_1 and discharges C_3, and the potential voltage of point A decays. In the meanwhile, the capacitor C_{DR2} is discharged. As the potential voltage of point C is greater than zero, D_6 is reverse biased. The voltage of C_3 decreases to zero and D3 conducts naturally.



(a)

1) *Stage 2* [Refer to Fig. (b)]

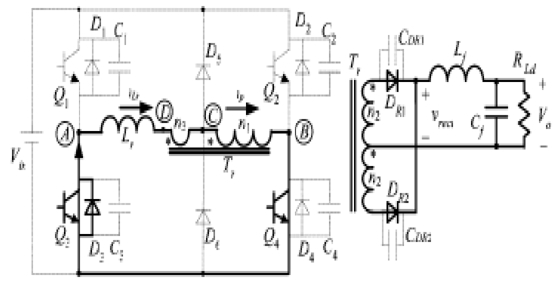
Q_3 can be turned on at zero voltage when D_3 conducts.C_{DR2} Continues to be discharged since the voltage of point C is still higher than zero. i_{Lr} and i_p continue decaying. This stage finishes when and the voltage of point C reduces to zero.



(b)

3) *Stage 3* [Refer to Fig. 3(c)]

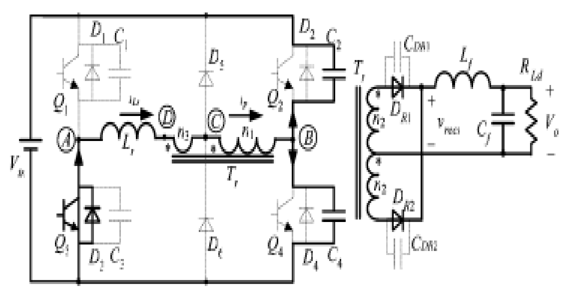
D_{R1} and D_{R2} conduct simultaneously, clamping the secondary voltage at zero. i_{Lr} is equal to i_p , and the. circuit operates in free-wheeling mode.



(c)

4) *Stage 4* [Refer to Fig. 3(d)]

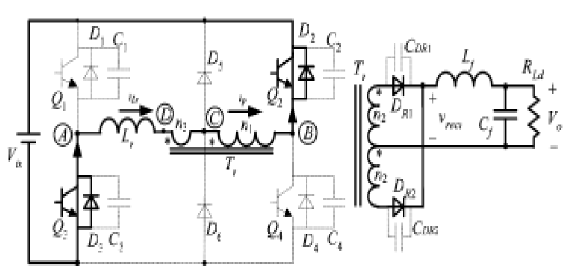
Q_4 is turned off at zero voltage at t_3, and is charged and C_2 is discharged in a resonant manner. This stage finishes when V_{C4} rises to V_{in} and V_{C2} falls to zero.



(d)

5) *Stage 5* [Refer to Fig. 3(e)]

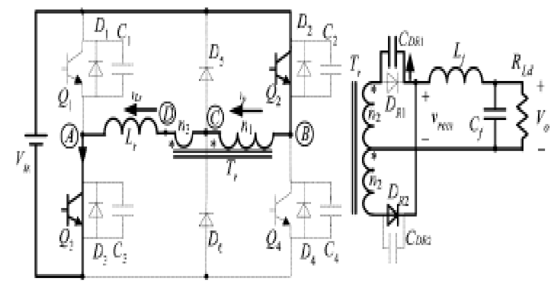
D_2 conducts naturally when V_{C2} decays to zero, and Q_2 can be turned on at zero voltage. Since i_{Lr} is equal to i_p, both of them decay linearly with the rate of V_{in}/ L_r. Now i_{Lr} and i_p crosses zero, and continue increasing linearly in the negative direction. The load current flows through both the rectifier diodes. As i_{Lr} and i_p reaches the reflected filter inductance current, D_{R1} turns off.



(e)

6) *Stage 6* [Refer to Fig. 3(f)]

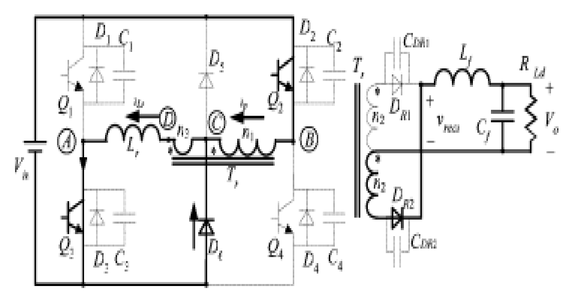
L_r resonates with C_{DR1}, and C_{DR1} is charged in a resonant manner. i_p and i_{Lr} continue increasing. The voltage of C_{DR1} rises to $2V_{in} .n_2/n_1$, and the primary voltage of the transformer, V_{BC} is V_{in}, the potential voltage of point C reduces to zero. So D_6 conducts, clamping V_{BC} at V_{in}, and the voltage of C_{DR1} is clamped at $2V_{in} .n_2 /n_1$.



(f)

7) ***Stage 7*** [Refer to Fig. 3(g)]

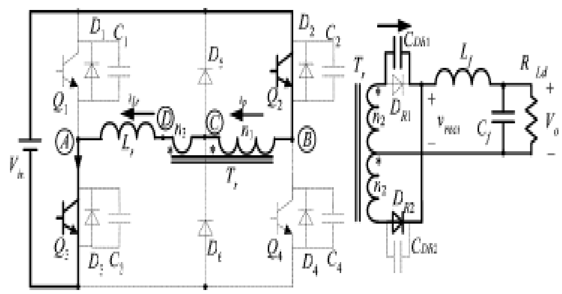
i_p declines downwards to the reflected filter inductance current when D_6 conducts, and increases in the negative direction. The voltage of the reset winding is $V_{in}.n_3/n_1$, which is applied to L_r, making i_{Lr} decrease quickly. Since i_{Lr} is greater than i_p, the current difference flows through D_6. This stage finishes when i_p equals i_{Lr}, and D_6 turns off naturally.



(g)

8) *Stage 8* [Refer to Fig. 3(h)]

The reset winding is in series with the primary winding after D_6 turns off. During this stage, L_r resonates with C_{DR1}.



(h)

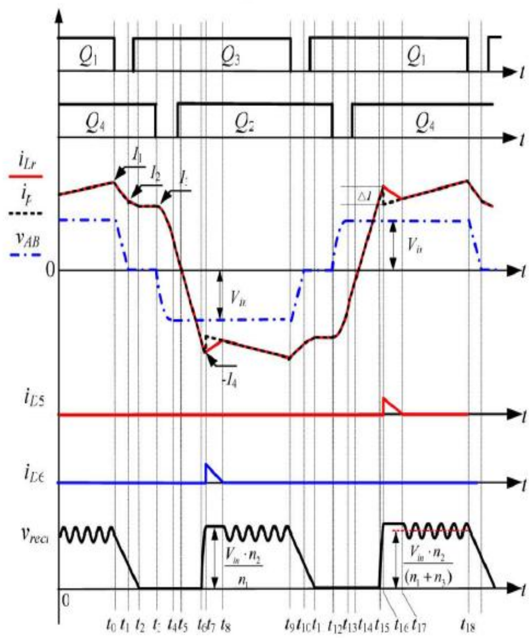


Fig: 4. Waveforms of ZVS PWM full-bridge converters with Reset Winding

3. Simulation Results

In order to observe the concrete comparisons, the computer simulation of ZVS PWM Full Bridge Converter has been carried out using a Mat lab simulink software package with the following parameters:

- Input voltage Vin : 290 VDC;
- Output voltage : 180 VDC;
- Maximum output current Io: 6 A;
- switching frequency fs: 100 kHz;
- Resonant inductance L_r : 8.5μH;
- Filter capacitance C_f : 100μF;
- Filter inductance L_f : 230μH;
- Load Resistor R_L: 30Ω;

Fig:6. Shows the generation of gate pulses fot Tr-Lag and Tr-Lag connection.

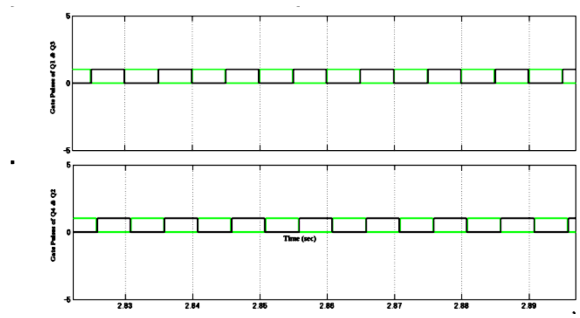


Fig:5. Gate pulse generated for both Transformer-lagging and leading circuits.

3.1Transformer Lag Connection

The transformer lag connection is so named because the primary winding of the transformer is connected to the lagging leg of the full bridge converter.

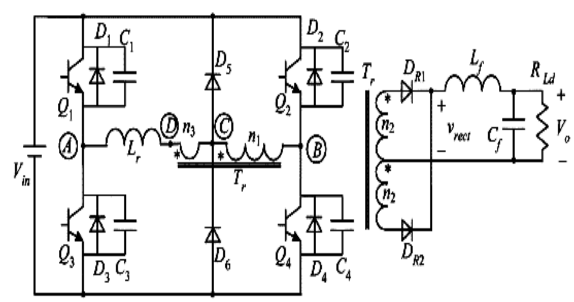


Fig:6. Tr-Lag type ZVS full bridge PWM full bridge converter

The simulation results of gate pulse generation input and output voltages, output current, inverter output voltage, current through the resonant inductor, voltage across the switch, zero voltage switching fot Tr-Lag connection performance are presented from fig: 7 to fig: 12

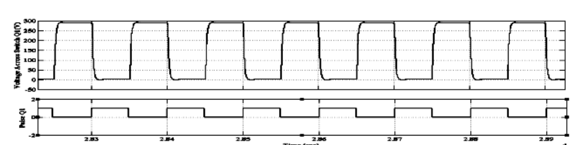


Fig:7. Voltage Across Switch Q1 (Tr-Lag)

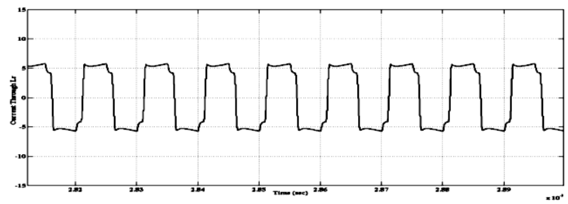


Fig:8. Current Through Lr (Tr-Lag)

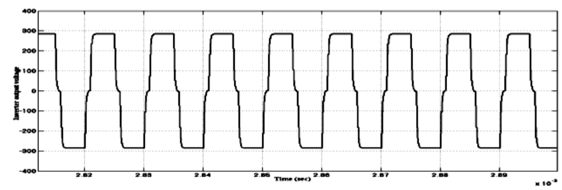


Fig9: Inverter output Voltage (Tr-Lag)

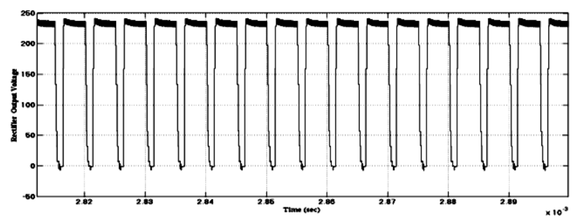


Fig:10. Rectifier Output Voltage (Tr-Lag)

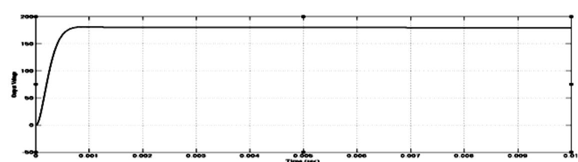


Fig:11. Output Voltage (Tr-Lag)

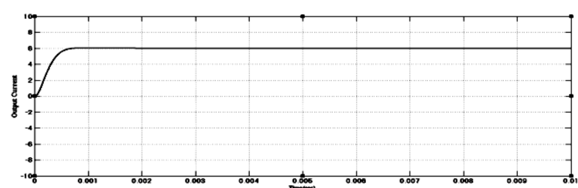


Fig:12.. Output Current (Tr-Lag)

3.2. Transformer Lead Connection

The transformer lead connection is so named because the primary winding of the transformer is connected to the leading leg of the full bridge converter. In this connection the clamping diode comes into action twice.

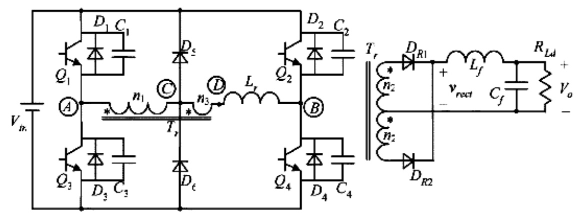


Fig:13. Tr-Lead type ZVS full bridge PWM full bridge converter

The simulation results of input and output voltages, output current, inverter output voltage, current through the resonant inductor, voltage across the switch, zero voltage switching fot Tr-Lead connection performance are presented from fig: 13 to fig: 19

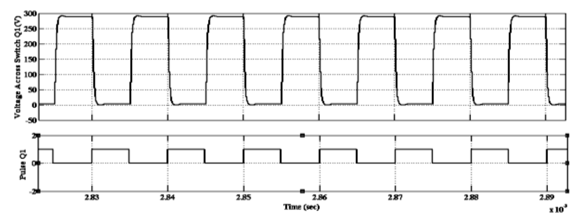


Fig:14. Voltage Across Switch Q1 (Tr-Lead)

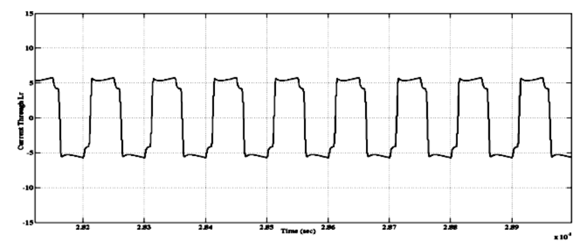


Fig:15. Current Through Lr (Tr-Lead)

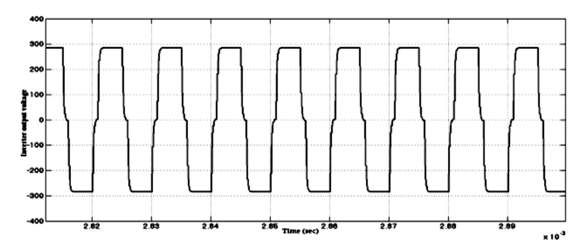


Fig16: Inverter output Voltage (Tr-Lead)

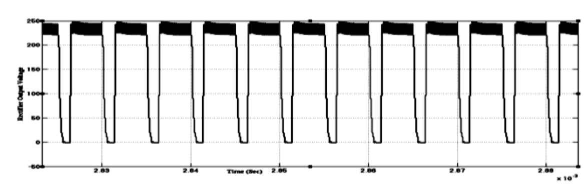


Fig:17. Rectifier Output Voltage (Tr-Lead)

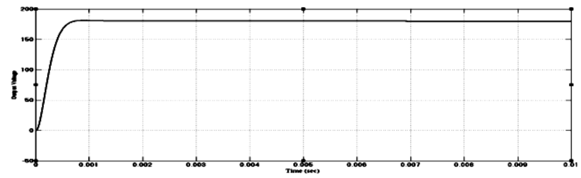


Fig:18. Output Voltage (Tr-Lead)

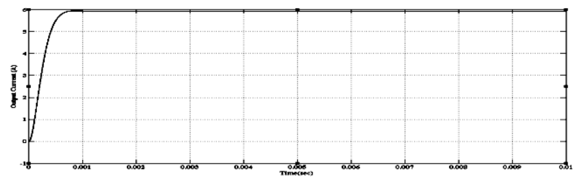


Fig:19.. Output Current (Tr-Lead)

4. Conclusion

A ZVS PWM full-bridge converter is proposed in this paper, it employs an additional reset winding to make the clamping diode current decay rapidly when the clamping diode conducts, thus the conduction losses of the clamping diodes. The reset winding removes the need of auxiliary switches and the resonant inductance is reduced. The use of reset winding removes the need of hard switching for clamping diodes so there will not be any power loss due to switching of clamping diodes and the conversion efficiency will increased. In the meanwhile, the clamping diodes can be turned off naturally without reverse recovery over the whole input voltage range, and the output filter inductance can be designed to be large to obtain small current ripple, leading to reduced filter capacitance. Compared with the traditional full bridge converter, the proposed circuit provides another simple and effective approach to avoid the reverse recovery of the clamping diodes. The structure and operation of the proposed ZVS PWM full-bridge converter with reset winding topology are described and two configurations have been studied i.e. Transformer-leading and Transformer-Lagging connections. We have studied the performance of both the configuration. If we compare the rectifier output in both the case we find that Tr-Lag connection produces less ripples. Transformer lagging configuration is advisable for more accurate results.

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