International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 4 Issue 12, December-2015

Simulation and Performance Analysis of Resistive Superconductor Surge Current Protection

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***Abstract* - Increase in power generation capacity of electrical power systems has lead to increase in the fault current level which can exceed the maximum designed short-circuit ratings of the switchgear. Many conventional protective devices like circuit breakers have been installed for protection of excessive fault current in electric power systems required to be tripped by over-current protection relay. In this paper, the simulation modelling and performance analysis of superconductor surge current protection is carried out. The modelling was carried out using Power System Analysis Toolbox while the simulation used matlab codes. The result showed that with the system faulted without the introduction of superconductor surge current protection the fault current was very high. The introduction of superconductor in the power system showed tremendous reduction in the fault current.**

Keywords: Circuit breaker, Fault current, Simulation, Resistive Superconductor Fault Current Limiters (RSFCL).

I. INTRODUCTION

problems especially transient stability. Hence, transient stability enhancement of a power system in the event of a short circuit will be of great importance. Employing Fault Current Limiters (FCL) is one of the useful methods to improve the transient stability of a power system. Fault Current Limiter (FCL) especially its resistive type, i.e. Resistive Fault Current Limiter reduces the fault current level of power systems **[1].** Limiting current allows the nominal and fault level ratings of equipment, such as converter switching devices or CBs, to be lower than without the SFCL. Current limiting may also limit the actual current density flowing through cables and other equipments, reducing the likelihood of approaching the critical current density of equipment. A properly designed FCL will have large impedance in fault conditions, quick appearance of impedance when fault occurs, provide rapid detection and initiation of limiting action within less than one cycle or 16ms and be capable of addressing two faults within a period of 15 seconds.

As a result of the reduction in fault current, the rating of the circuit breaker will be reduced as well as the weight and physical size of the CB. Using SFCLs with CBs may also increase the reliability of successful fault interruption because the SFCL, when operating as designed, will limit the fault current seen by the CB to its rated value [2].

Among the parameters of the FCL, the magnitude of the limiting impedance and its merits affects the current-limiting performance of the FCL much more than the other parameters. In other words, depending upon the kind of the FCL and its merits, the insertion of the FCL in to the power system can result in more severe interrupting problems. Therefore, it is important to study the interrupting behavior of circuit breakers in the presence of the kinds of FCLs. FCLs have large impedance in fault conditions and have very low impedance in normal conditions and also instantaneous recovery to zero impedance post fault clearance [3].

Most importantly, usage of FCLs is to reduce the fault current to withstanding level of existing circuit breakers. So, the existing equipments can still be used to protect the power system. Also after being limited by the FCL, the current is interrupted at its current zero by a circuit breaker. After the interruption of the fault current, a transient recovery voltage (TRV) appears across the contacts of the circuit breaker. To perform a successful interruption, the circuit breaker must withstand the TRV without re-establishment of the arc between the contacts [4].

II. SIMULATION OF THE NINE BUS SYSTEM WITH FAULT

The popular Western System Coordinated Council (WSCC) 3 machine, 9-bus system shown in Fig2.1 has been considered to be used for the modeling. In order to see the operation of power system circuits, two cases are considered. (1) Fault condition and (2) When a current limiter is inserted at the point of fault in series. Matlab simulation is used with NR and GS method of iterations and this Matlab simulation is programmed to plot the graphs for each of these conditions with a PSAT simulator.

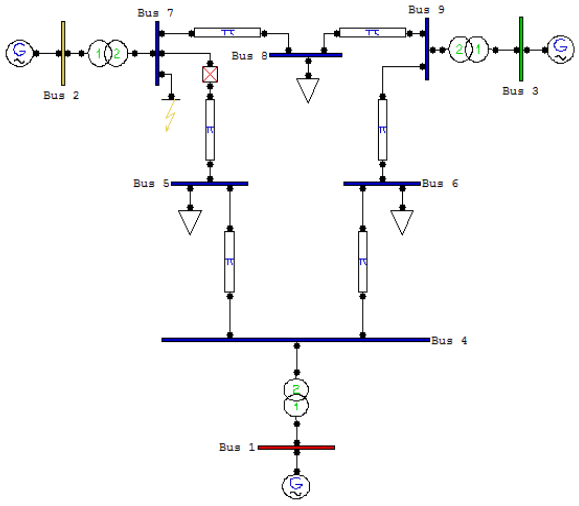

Fig. 1 Shows the 9 bus and 3 machine network with fault on bus 7[5]

For test system, bus 1 is chosen as slack bus which is used to compensate loses in the system, bus 2 and 3 are taken as the voltage control bus and other buses 5, 6 and 8 are the load buses as shown in fig.1

The network above consists of three generators, nine transmission lines, three transformers, and three loads. Generator 1 has its generating voltge at 16.5 KV, 2 has a generating voltage of 18KV and 3 has a generating voltage of 13.5KV. Transformers are connected between buses and synchronous generators for steping up the voltages at their respective generating voltages to 230KV. A circuit breaker is connected between bus 7 and bus 8. The base MVA is 100, and the system frequency is 50 Hz. In the above network (fig.1) simulation is run to see the behaviour of the network when the system is with fault) and the plots for the transformers and the power flow of the system is presented. The summary of the electrical parameters is shown in tab.1 below.

Table 1. Summary of Test System Steady-State Parameters [5]

S/NO	Parameter Description	Value	Unit
1	Base power	100	MVA
2	System Voltage	230	KVA
3	Substation Transformer 1	16.5/230	KVA
4	Substation Transformer 2	18/230	KVA
5	Substation Transformer 3	13.8/230	KVA
6	Generator 1-3	100 each	MVA
7	Nominal Frequency	50	Hz
8	Source Short-Circuit Power	400	MVA
9	Fault Impedance Z_F	0.4	Ω
10	Source/Internal Impedance	2	Ω
11	Limiter Impedance Z_{FCL}	20% of source impedance	Ω

On applying fault at bus 7, as shown in fig .1 above the current in bus 2 plotted as shown in fig 1.2 below. The fault time is 1second and the fault clearing time is 1.09 seconds. The first intervention of the circuit breaker 1.09seconds and the second intervention time, which is the reclosing time of the circuit breaker, is 2.1 seconds. From fig 1.2, it can be seen that the power at the buses are not constant after 1second. It shows that there is a lot of disturbance between the time one second and four seconds. Even though the circuit breaker recloses at 2.11 seconds, due to synchronous generator at these buses, the time taken to come back to normal operation is longer than the power flow in transmission line.

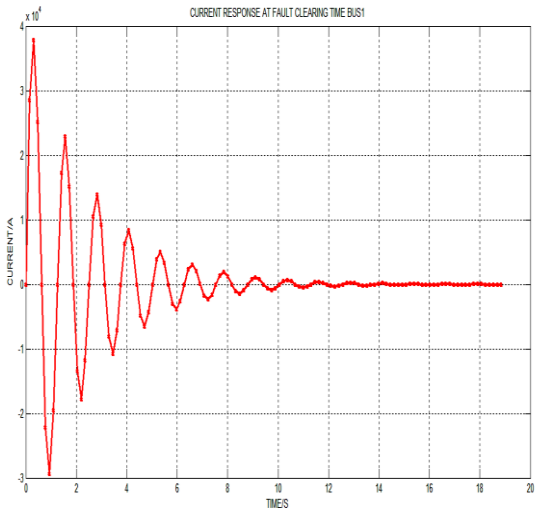

Fig 1.1 current response at bus 1

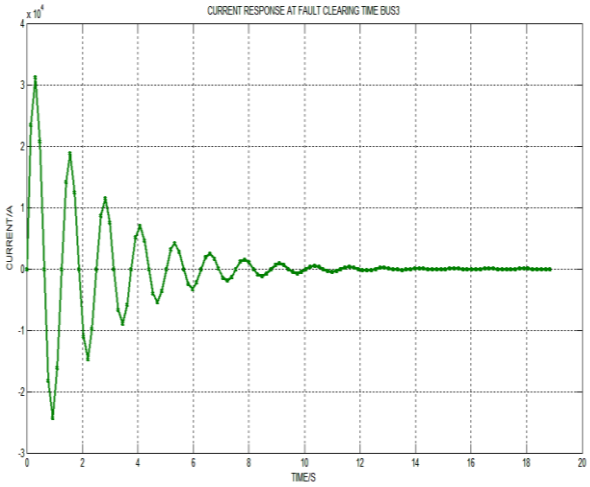

Figure 1.2 current response at bus 2

II. RESULTS DURING FAULT IN THE SYSTEM

From fig 1.1 to fig 1.3 it is seen that the current in the network during fault is increased to a very high value, which is called fault current. This means that voltges at the buses decreases to a very low value during fault and once the fault is cleared the voltage returns to its normal value. It is observed that the fault current is highest on the bus 2, because this buse is close to the fault position, which is at bus 7. However there is also some disturbance at time 1.9seconds because circuit breaker recloses then and the generators have to supply more power. When all the three generators come in synchronism with each other, the current returns to its normal value at time 10seconds.

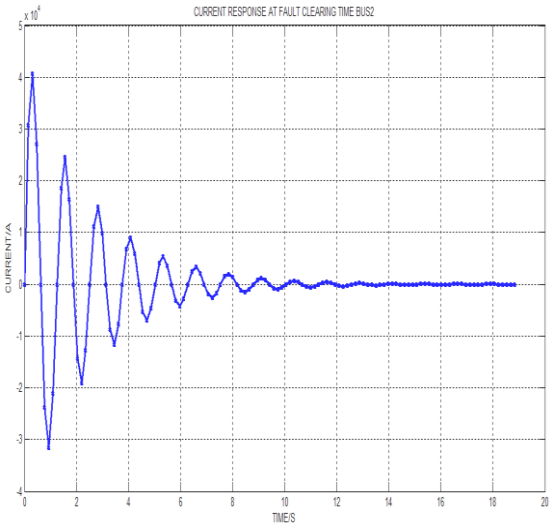

Figure 1.3 current response at bus 3

IV. SIMULATION OF THE NINE BUS SYSTEM WITH RSFCL

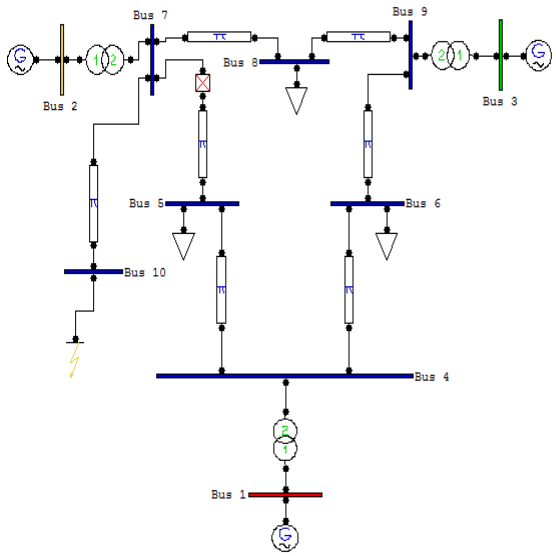

fig .2 Shows the 9 bus and 3 machine network with fault and rsfcl

On inserting RSFCL in series with the fault at bus 7, as shown in fig 2 above the current in bus 1, 2, and 3are plotted as shown in fig 2.1 to fig 1.3 below.

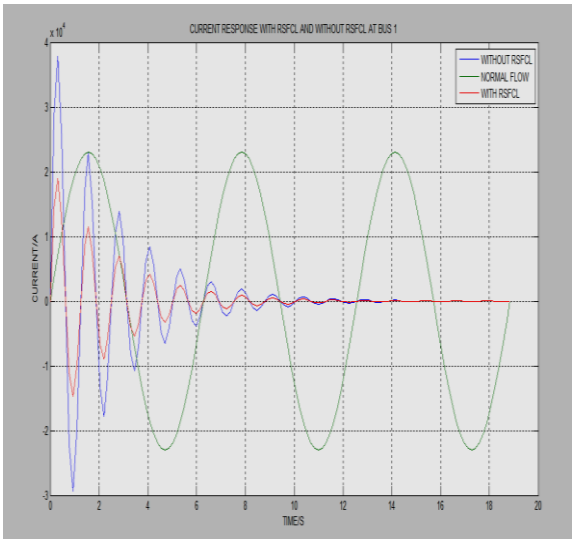

Figure 2.1 Current Response with and without RSFCL at bus 1

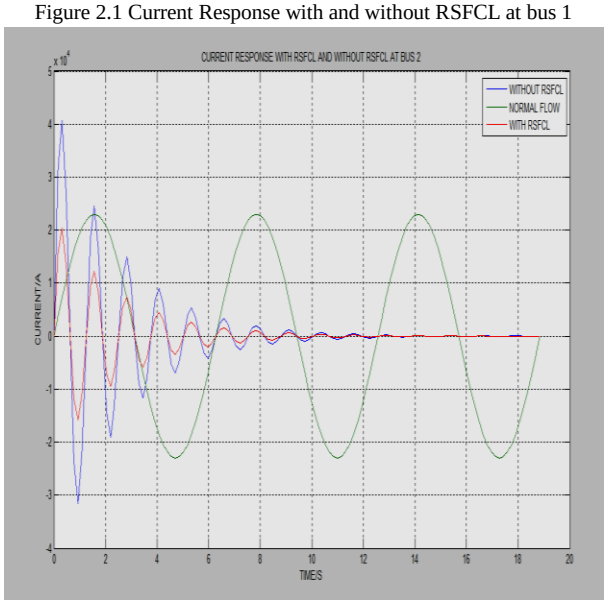

Figure 2.2 Current Response with and without RSFCL at bus 2

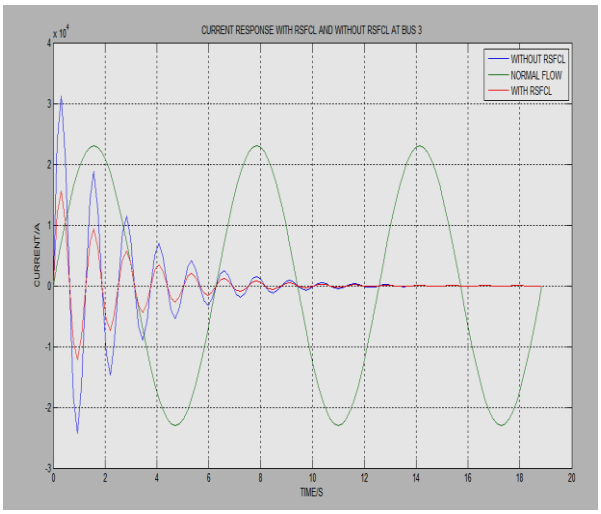

Fig 2.3 Current Response with and without RSFCL at bus 3

V. RESULTS OF RSFCL IN SERIES WITH FAULT IN THE SYSTEM

Based on the principle of fault current limiter, the impedance of FCL increases during fault, which limits the current during fault. To show the effect of the increases in impedance during fault, a dummy line is added between bus 7 and fault, which is bus 10 (fig .2). This is because PSAT does not allow fault to be connected to the transmission line.

Increasing the impedance of the dummy transmission line, (the line between fault and bus 7), the current during fault is considerably reduced to a lower value as shown in fig 2.1 to fig 2.3 above. The fault time is 0.1 second and the fault clearing time is 1.9 seconds. The current during this period was very high before the increase in the impedance between the fault and the bus 7. The fault current on bus 2 is $3.9x10^4$A, which is very high to damage the equipment installed in the system because the current during normal operation is $2.1x10^4$ on bus 2. From fig 2.1, it can be seen that the fault current is considerably reduced to a lower value close to its value during normal operation. Similarly the faults currents are reduced at other buses as well. The summary of the fault currents with and without Resistive Superconductor Fault Current Limiter at each bus is shown below in tab .2

Table.2 Line current with and without RSFCL

Bus	Current Values without RSFCL (A)	Current Values with RSFCL (A)
1	$3.9x10^4$	$1.95x10^4$
2	$4.05x10^4$	$2.0x10^4$
3	$3.1x10^4$	$1.55x10^4$
4	$5.7x10^5$	$2.85x10^5$
5	$5.0x10^5$	$2.5x10^5$
6	$5.1x10^5$	$2.55x10^5$
7	$5.7x10^5$	$2.85x10^5$
8	$5.7x10^5$	$2.855x10^5$
9	$5.8x10^5$	$2.9x10^4$

From tab 2 above, it shows that during the presence of RSFCL the fault current is reduced to almost half of the fault current value without RSFCL.
The comparison results are shown in Fig .3 above.

From Fig .3 it is see that the fault current is limited by a maximum of 50% for the specified RSFCL impedance. So if the Limiter impedance is further increased, the current limitation effectiveness is reduced.

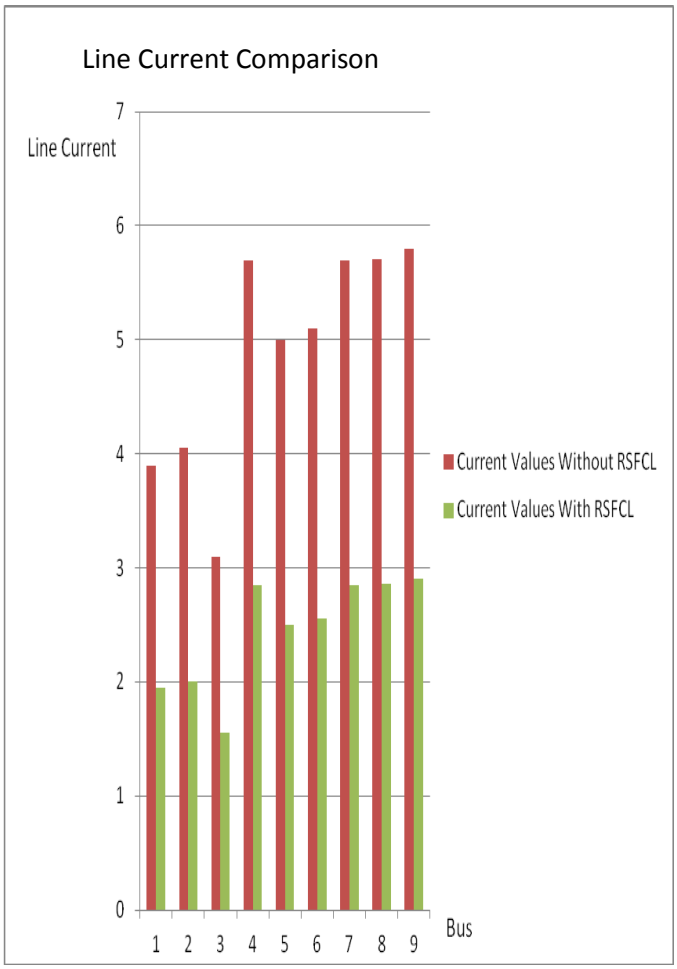

Figure.3 Line Current Comparisons with and without RSFCL

VI. CONCLUSION

The purpose of this work is to analyse the effect of resistive superconductor fault current limiter when implemented in a power system. Several methods are explained in literature review. From this work, simulation modelling was carried out on superconductor surge current protection. The simulation result from MATLAB/PSAT application showed that this method can reduce losses and improve power quality in test system. The performance of the power system with and without RSFCL also have been analyzed and found that implementation of RSFCL gives good effect to the performance of the system. The proposed model reduces the large fault currents to a lower managerial level, during steady state the voltage drop in the system is zero. The device detects fault current within the first cycle of fault. In conclusion, as the Fault Current is reduced, the lower rating circuit breakers can be used in the power system.

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